PIN Limiter Diodes in Receiver Protectors

Introduction

Radio and radar receivers must be capable of processing very small signals, necessitating the use of very sensitive circuit blocks that can contain fragile semiconductors. Many of these systems must also be capable of surviving very large incident signals, without damage to the sensitive components they contain. The receiver protection limiter, most often referred to simply as a limiter, can protect the receiver from large input signals and also allow the receiver to function normally when these large signals are not present.

Limiters are most often employed in radar transceivers, whose transmitters and receivers are tuned to the same frequency. The transmitter produces a signal, the peak level of which is in most systems in the kilowatts or megawatts order of magnitude, which is applied to an antenna that is typically also utilized by the receiver. The receiver must be capable of reliably detecting and processing very weak reflected signals, so it has a sensitive, low noise amplifier (LNA) at its input, although some receivers apply the received signal directly to the input of a downconverter mixer. Both of these circuit blocks employ sensitive semiconductor components that will very likely be damaged by even a small portion of the transmitter signal that might be coupled to the receiver input, either by reflection from the antenna or by other means. A limiter can protect these components.
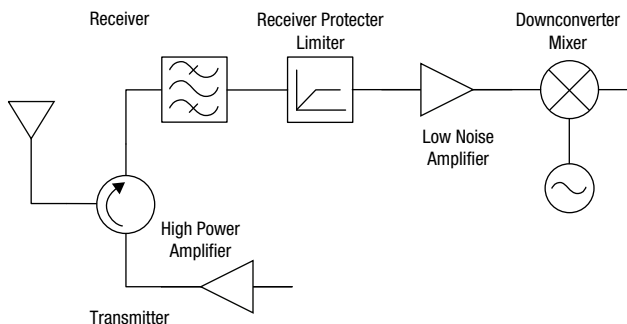

Figure 1. Simplified Radar Transceiver with a Receiver Protector Limiter

A Simple Limiter Circuit

A simple, passive receiver protection limiter is shown in Figure 2. In its most fundamental form, this circuit consists of a PIN diode and an RF choke inductor, both of which are in shunt with the main signal path. In most limiter circuits, DC blocking capacitors are included at the input and the output of the circuit. A single-stage limiter can typically reduce the amplitude of a large input signal by 20–30 dB.
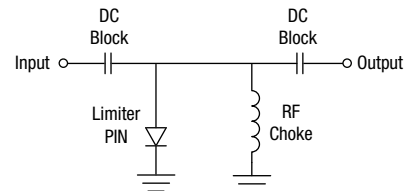

Figure 2. A Single-Stage Limiter

The PIN limiter diode can be described as an incident power-controlled, variable resistor. In the case when no large input signal is present, the impedance of the limiter diode is at its maximum, thereby producing minimum insertion loss, typically less than 0.5 dB. The presence of a large input signal temporarily forces the impedance of the diode to a much lower value, producing an impedance mismatch which reflects the majority of the input signal power back towards its source. A nominal transfer curve for a limiter stage is shown in Figure 3.

When the large input signal is no longer present, the impedance of the diode reverts from a very low value to its maximum value after a brief delay elapses. The limiter diode and its environment determine the duration of this delay.

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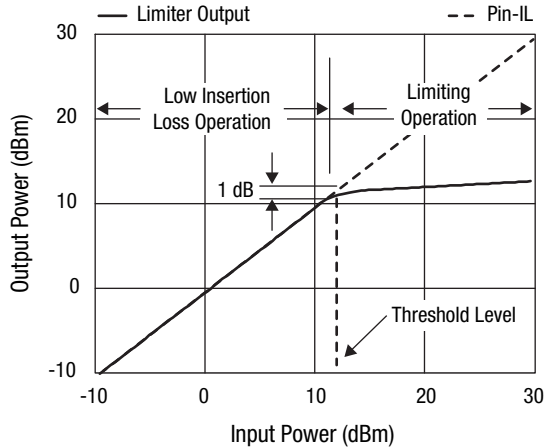
**Figure 3. Output Power vs. Input Power for a
Single-Stage Limiter**

It is important to note that when a large input signal is present, the limiter diode reflects rather than dissipates the majority of the input signal power. In a properly designed circuit, a limiter diode that is capable of safely dissipating only a few hundred milliwatts is also capable of protecting a receiver from signals many orders of magnitude larger, without damage to the limiter diode. Of course, this is based upon the assumption that the reflected signal is either re-radiated from the system antenna, or is directed by a non-reciprocal device, such as a circulator or an isolator, to a resistive load that can dissipate the reflected signal power.

Clipper (Limiter) Circuit

Note that the PIN limiter circuit operates differently from another class of limiter, known as a "clipper," an example of which is shown in Figure 4. In that type of circuit, two rectifying diodes (which could be Schottky or PN junction diodes) are utilized to limit the peak voltage of the positive and negative signal alternations, either referenced to ground or to some arbitrarily selected DC level. This circuit, in this case with the rectifier diodes connected to ground, allows signals whose amplitudes are less than the cut-in voltage of the rectifier diodes to pass unchanged. Signals whose voltage amplitudes are larger than the cut-in voltage of the rectifying junction will force the diode into conduction. In this case, the voltage drop across the diode is approximately 0.7 V for a Si PN diode, so the peak voltage of the alternation that forward biases the diode is clamped to within a forward voltage drop of the potential to which the diode is connected. Note that the output signal is no longer purely sinusoidal—plentiful harmonics of the input signal can be generated by clipper circuits.
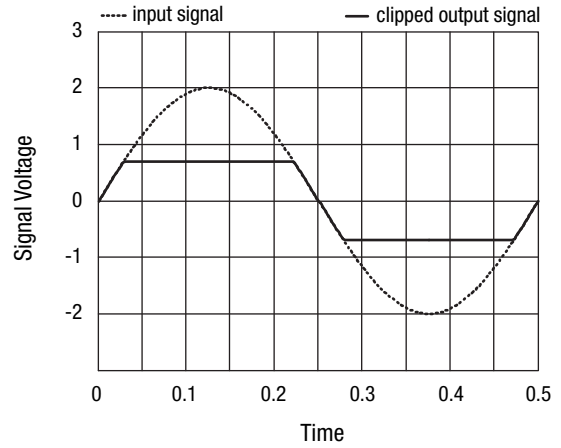

**Figure 4. Clipper Circuit and Large Signal
Input/Output Waveforms**

Clipper circuits are typically used for low frequency applications, nominally at VHF and below, since the stored charge of the rectifier diodes limits rectification efficiency at higher frequencies. This type of limiting circuit is often found in frequency modulation or phase modulation receiver IF amplifier sections.

In the "grey area" where the frequency of a signal is at the higher end of the range where clippers are useful, but at the lower end of the range where a PIN limiter circuit (as shown in Figure 2) is utilized, an antiparallel pair of PIN diodes, such as SMP1330-005[1], can be used in the clipper circuit shown in Figure 4. In the lower UHF band, this circuit will act as a hybrid of the clipper and the incident-power-controlled, variable resistor limiter.

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Description of the PIN Limiter Diode

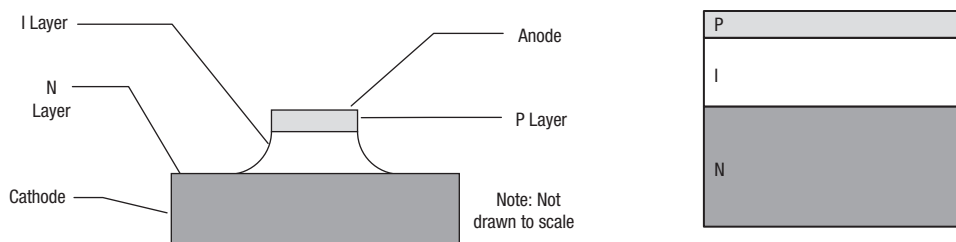The cross-sectional diagram of a typical mesa PIN limiter diode die is shown in Figure 5.

Figure 5. Cross-Sectional Views of a Limiter PIN Diode Die (Left) and Its Cylindrical Section Approximation (Right)

When a large input signal is incident upon the limiter PIN diode, the electric field of the signal temporarily forces positive charge carriers (holes) from the diode P layer and negative charge carriers (electrons) from the diode N layer into the nominally undoped, high impedance I layer, causing the impedance of the diode to be temporarily reduced to a much lower value.

The minimum and maximum impedances of the limiter PIN diode are determined by the geometry of the diode as well as the resistivity of the diode's I layer. In the simplest approximation, the PIN diode can be modeled as a right cylindrical section with three separate layers: the P layer, the I layer and the N layer, where the resistance of each layer is given by

$$R_{LAYER} = \frac{p_{LAYER} \times Thickness_{LAYER}}{Area_{LAYER}}$$

where p_{LAYER} is the resistivity of the layer.

P Layer

The P layer is heavily doped with p-type acceptor impurities. It is typically quite thin, so its resistance is sufficiently small (of the order of a few mΩ) that it is ignored in most analyses.

N Layer

The N layer is sometimes called the N$^+$ layer because it is very heavily doped with n-type donor impurities. Its thickness is generally the largest of the three diode layers, so while its resistivity is small, its resistance is large enough that it should not be ignored. The resistance of this layer is most often of the order of tenths of an ohm. The electrical resistance of this layer is a major constituent of the minimum impedance of the limiter PIN diode. The N layer is also a significant element of the diode thermal impedance.

I Layer

The I layer that is sandwiched between the P and the N layers is "where the action is" for a PIN diode. This layer is nominally undoped ("I" stands for "intrinsic"), but in actual practice it is very lightly doped with n-type donor impurities. In the state when no external forward bias is applied to the diode, the resistivity of this layer is of the order of a few hundred Ω-cm or more, so the resistance it produces can be in the many hundreds to few thousands of ohms.

The resistance of the I layer can be modulated by forcing charge carriers into it from the P and N layers, simply by applying a forward bias voltage or current to the diode. The resistance of the I layer is exponentially indirectly proportional to the current flowing through the diode, that is, it can be described by

$$R_{ILAYER} = k \times I^{-\alpha} + R_{BULK}$$

where

R_{ILAYER}	is the series resistance of the I layer of the diode
k	is a constant, which is equal to the R_{ILAYER} of the diode when I = 1 mA, assuming I is also expressed in mA
I	is the current through the diode, expressed in mA, assuming k is also expressed in mA
α	is a curve fitting factor which is related to the slope of the R_{ILAYER} vs. I curve for the diode. For a typical PIN diode, $0.84 \leq \alpha \leq 0.9$
R_{BULK}	Saturated resistance of the I layer

It is also possible to express the resistance of the I layer in terms of its physical properties and bias current:

$$R_{I\text{-}LAYER} = \frac{w^2}{2* I_F * \mu_A * T_L}$$

where

R_{ILayer}	is the series resistance of the I layer of the diode
w	is the thickness of the I layer
I_F	is the bias current through the diode
μ_A	is ambipolar carrier mobility, $\mu_A = (\mu_N + \mu_P)/2$, where μ_N and μ_P are the carrier mobilities of electrons and holes, respectively
T_L	is the minority carrier lifetime

From this we can see that I layer resistance and minority carrier lifetime are indirectly proportional to each other.

The shape and resistivity of this layer determine the minority carrier lifetime of the diode. The thickness and doping concentration of the I layer determine reverse breakdown voltage and the threshold level of the diode; more about these important parameters later.

Total PIN Diode Resistance, R_S

The total resistance of a PIN diode is equal to the sum of the resistances of the P, I and N layers, since they are electrically in series. The resistances of the P and N layers are constants. For non-zero bias current, the total series resistance of a PIN diode is

$$R_S = R_{I\text{-}LAYER} + R_{P\text{-}LAYER} + R_{N\text{-}LAYER} = K \times I^{-\alpha} + R_{SAT}$$

The three constant terms, R_{BULK}, $R_{P\text{-}LAYER}$ and $R_{N\text{-}LAYER}$, are typically lumped together and referred to as R_{SAT}.

Power Dissipation

The power dissipated by a PIN diode in conduction is the sum of a DC and an AC term: the product of the DC current and the DC forward voltage; and, the product of the square of the RF current and series resistance of the diode. Since the DC component of the dissipated power is typically quite small (of the order of a few mW), it is often ignored. The RF currents in a limiter PIN diode can be large, so the AC term dominates the total power dissipation.

$$P_{DISS} = I_{DC} \times V_{DC} + I^2_{RF} \times R_S \approx I^2_{RF} \times R_S \quad \text{(conducting state)}$$

The PIN diode can also dissipate power when it is not conducting. In this state, dissipated power is given by

$$P_{DISS} = \frac{V^2_{RF}}{R_S} \quad \text{(non-conducting state)}$$

Since a passive limiter PIN diode is not in conduction when very small RF voltages are present, R_S remains large while V_{RF} is small; power dissipation in this state is negligible.

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NOTE: *This may not be the case for a PIN diode used as a switch for high power signals.*

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Threshold Level

The threshold level for a limiter PIN diode is defined as the input signal level at which the diode is 1 dB into compression. That is, the input signal level at which the insertion loss, due to the reduction of the diode's impedance resulting from the presence of a large RF signal, is 1 dB greater than that when a very small signal is incident upon the diode. The threshold level is primarily determined by the thickness of the I layer of the diode: they are directly proportional to each other. The thinnest practical limiter PIN diode has a nominal I layer thickness of 1 µm. Such a diode has a threshold level of approximately 7–10 dBm in a 50 Ω system. The thickest commercially available PIN limiter diodes have I layer thickness around 7 to 10 µm, with threshold levels of around 20–23 dBm. Limiter PIN diodes with I layer thicknesses between these values are available, with corresponding threshold levels.

Minority Carrier Lifetime

Minority carrier lifetime, T_L, is defined as the mean time that a free charge carrier exists before recombination occurs. It is also determined by characteristics of the I layer of a PIN diode: it is directly proportional to the volume of the I layer, but is slightly reduced by larger ratios of the I layer outer surface to I layer volume, and is directly proportional to the resistivity of the I layer. Small minority carrier lifetime of a limiter PIN diode is generally desirable because it is proportional to the brief delay between the cessation of a large RF signal across the diode and the reversion of the diode's impedance to its maximum value. The I layer of a limiter PIN diode is doped with gold atoms to establish charge trapping sites, thereby substantially reducing minority carrier lifetime, which is desirable for radar receiver protectors and other applications such as EW receivers. But, we have already seen that the minority carrier lifetime and series resistance of a PIN diode are indirectly proportional to each other; these two characteristics must be balanced against each other for optimal limiter performance.

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Minority carrier lifetime is related to limiter recovery time, which is a very important characteristic of a limiter that will be discussed in more detail later.

Junction Capacitance

The capacitance of the PIN limiter diode affects the small signal insertion loss of the diode. Capacitance is given by the familiar equation

$$C_J = \frac{\varepsilon \times A}{d}$$

where

C_J is the junction capacitance of the diode

ε is the dielectric constant of the I layer, where $\varepsilon = \varepsilon_0\varepsilon_R$, the product of the dielectric constant of free space and the relative dielectric constant of the material comprising the I layer

A is the area of the junction of the diode

d is the thickness of the depletion layer

So, it is clear from the discussions of threshold level, resistance, capacitance and minority carrier lifetime that the design of a PIN limiter diode is an exercise in tradeoffs: adjusting I layer thickness and junction area to determine junction capacitance and series resistance, while maintaining I layer thickness to meet requirements for a given threshold level; and looking at I layer volume, shape and doping to minimize minority carrier lifetime without deleteriously affecting series resistance and junction capacitance.

Avalanche Breakdown Voltage

Avalanche breakdown voltage is the reverse bias voltage at which "a breakdown is caused by the cumulative multiplication of charge carriers through field-induced impact ionization"[2]. For RF and microwave diodes, reverse breakdown voltage is most often defined to be the voltage required to force 10 µA of current to flow in the reverse-bias direction. The minimum rated breakdown voltage can be considered to be the absolute maximum reverse voltage that should be applied to the diode, unless otherwise noted in the manufacturer's specifications.

Direct measurement of the avalanche breakdown voltage of a PIN diode is not recommended. The avalanche breakdown condition can very easily cause catastrophic damage to a PIN diode. Under reverse bias, the resistivity of the I layer is maximum, so driving a

charge carrier through this region requires a very large electric field, typically of the order of 10 to 20 V per µm of thickness. Since the crystal structure of this region inevitably has discontinuities (remember the Au doping and the fact that during wafer processing the Si has been subjected to many processing steps, many of which can induce strain in the semiconductor crystal), when avalanche breakdown starts to occur, the current density through the I layer is not distributed equally but is concentrated in some regions, which are referred to as "filaments." The current densities in these filaments can be so large that the localized heating raises the temperature in these volumes to the point that diffusion of the p-type and n-type dopants from the P and N layers, respectively, into the I layer occurs. These filaments of dopants can extend through the entire thickness of the I layer, forming permanent short circuits. This process happens slowly enough, on a tenths-of-a-second scale, that it can be observed on a curve tracer. The diode will briefly produce the well-known diode I-V curve until filamentary diffusion shorts the I layer so that the curve shown on the curve tracer snaps to one that looks very much like that of a small-value resistor.

Thermal Impedance

The thermal impedance of a limiter diode is quite important, since it is well known that the serviceable life of a semiconductor is reduced exponentially as operating junction temperature increases. Even though in normal operation a limiter diode will dissipate only a small portion of the RF power incident upon it, that small portion can be appreciable. This power is converted from electrical energy to heat in the diode by Joule heating, primarily in the diode's I and N layers, since that is where the majority of the resistance of the diode resides.

Thermal Resistance

It is well known that there are three means by which heat can flow from a region of high temperature to regions of lower temperature: convection, radiation and conduction. Convection and radiation of heat from a diode die are negligible and are typically assumed to not contribute to the removal of heat from the diode.

Conduction of the heat generated in the I layer and at the pn junction (the interface between the heavily doped, p-type P layer and the lightly doped, n-type I layer) is through the cathode layer, which is typically the thickest layer of the diode. The electrical connection to the anode of the diode is made using a circular-cross-section wire (typically 0.0007 inches [17.8 µm] diameter) or a rectangular-cross-section ribbon (typically 0.00025 x 0.003 inches [6.35 µm x 76.2 µm]). The cross-sectional area of each of these conductors is sufficiently small that conduction of heat through this path is also considered to be negligible[3].

2. *"IEEE Standard Dictionary of Electrical and Electronics Terms,"* IEEE, Second Edition, 1977, p. 45.
3. A. W. Davis, *"Microwave Semiconductor Circuit Design,"* Van Nostrand Reinhold Co., 1984, p. 160.
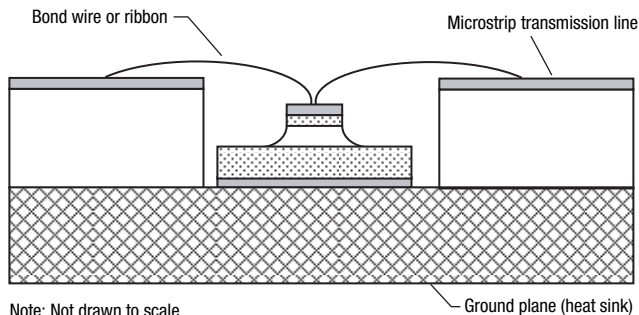
Note: Not drawn to scale

Figure 6. Cross Section of a Shunt PIN Limiter Diode in a Microstrip System

Rigorous calculation of thermal impedance for a diode can be quite involved. However, if we make some simplifying assumptions, we can reduce this calculation to a more manageable problem. Heat flows from a point source in conical section whose major angle is roughly 60°. If we assume nominal dimensions for a limiter PIN diode with a mesa, and that the heat is generated at the interface between the P and I layers, as long as a 60° conical section whose minor diameter is the circumference of the P-I interface is completely contained within the diode, then we simplify the analysis to assume that all heat flows from the diode through a right cylindrical section whose diameter is also equal to the diameter of the P-I interface as shown in Figure 6. This assumption is valid for virtually all commercially available limiter diodes. This analysis will predict a thermal resistance somewhat larger than that which is actually produced by the entire volume of the conic section, but this over-estimation of thermal resistance is often offset by overly optimistic assumptions about other thermal impedances within the system.
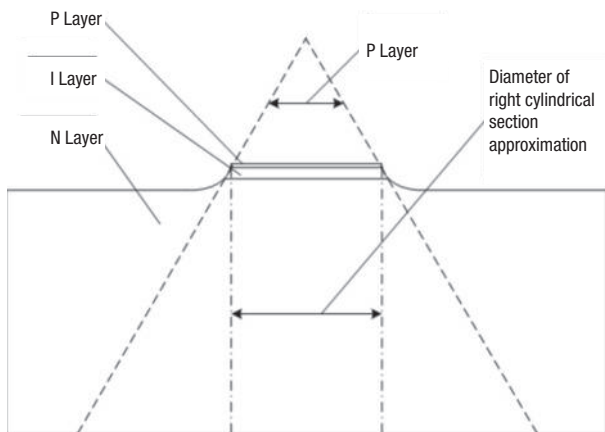
Figure 7. Cross Section of a Shunt PIN Limiter Diode in a Microstrip System

The thermal resistance from junction to heat sink, θ_{JC}, is given by

$$\theta_{JC} = \frac{L}{G_{THERMAL} \times A}$$

where

θ_{JC} = Thermal resistance from junction to heat sink

L = Length of thermal conduction path (approximately the combined thickness of the I and N layers of a limiter PIN diode)

$G_{THERMAL}$ = Thermal conductivity of the material in the thermal path (for Si, 0.84 W/(cm°C))[4]

A = Cross-sectional area of the right cylindrical section assumed to be path for heat flow

Thermal Capacitance

A finite period of time is required for heat to flow out of the diode. During this time, the temperature of the diode increases as the heat propagates from the junction to the die attach interface to the heatsink. Thermal capacitance, $C_{THERMAL}$, also known as heat capacity, is defined as the amount of energy required to raise the temperature of the diode I layer by 1 °C, in the absence of heat flow from the diode[5]. Thermal capacitance is given by

$$C_{THERMAL} = \frac{(Specific\_Heat \times Density)}{Volume}$$

where

$C_{THERMAL}$ = Thermal capacitance
Specific Heat = Specific heat of Si = 0.176 cal/(g °C)
Density = Density of Si = 2.43 g/cm^3
Volume = I & N layer volumes = $(\pi \times radius_{ILAYER}^2)/(thickness_{ILAYER} + thickness_{N\ LAYER})$

Thermal Time Constant

The thermal time constant of a limiter diode can be used to understand how the junction temperature of a limiter diode changes over time. It is important since the diode will not reach its final, steady state temperature until approximately 6 thermal time constants, $\tau_{THERMAL}$, have elapsed, assuming a constant amplitude input signal. For signal bursts of briefer duration, junction temperature may reach a peak value less than that it would reach for much longer bursts.

4. *"Reference Data for Radio Engineers,"* Howard W. Sams & Co., Sixth Edition, 1975, p. 4-13.
5. J. F. White, *"Microwave Semiconductor Engineering,"* J. F. White Publications, 1995, p. 106.

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Thermal time constant is the analog of electrical time constant. It is the product of thermal resistance and thermal capacitance.

$$\tau_{THERMAL} = \theta_{JC} \times C_{THERMAL}$$

The junction temperature of a limiter diode versus time is given by

$$T_J = T_{HEATSINK} + \Delta T_J$$

where

$$\Delta T_J = P_{DISSIPATED} \times \theta_{JC} \left(1 - e^{\frac{-t}{\tau_{THERMAL}}}\right)$$

Since the heat sink in a typical system is not infinite, rigorous analysis should include the thermal resistances and capacitances of the remainder of the system, such as that of the die attach medium, system ground plane, system housing, etc.

T_J vs. Time

Consider a series of RF bursts incident upon a typical limiter diode, such as CLA4606-000. The thermal resistance of the diode is 80 °C/W, the diode's P layer diameter is 63.5 µm, its I layer is 2.5 µm thick and its N layer is 100 µm thick. Also assume that the peak dissipated power in the diode is 2 W, the duration of each RF burst (sometimes called the "pulse width") is 25 µs at 2.5% duty cycle and the die attach surface is maintained at 40 °C.

If the input signal were continuous wave (CW), the junction temperature would seriously exceed the maximum rated temperature, and the diode would consequently be destroyed. The thermal capacitance of this diode is 57.6 µJ/°C, so the thermal time constant is $\tau_{THERMAL}$= 46 µs. Since 6 * $\tau_{THERMAL}$ is substantially longer than the burst duration, we can expect that the junction temperature of diode will not reach the maximum possible temperature. The simulated junction temperature versus time for this set of conditions is shown in Figure 8.
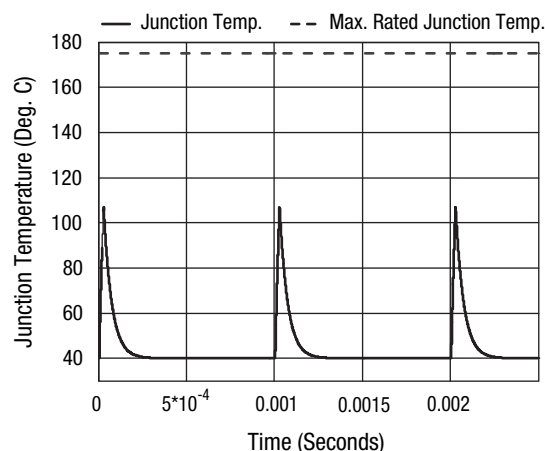
Figure 8. Diode Junction Temperature vs. Time, Duty Cycle = 10%

We can see in Figure 8 that the peak diode temperature is approximately 107 °C, which is well under the rated maximum junction temperature of 175 °C. Notice that after each RF burst there is ample time for the T_J to recover to the die attach surface temperature before the next burst occurs. Under these signal conditions, the diode is not subjected to overstress.

Assume the duty cycle increases to 40% and the burst duration increases to 50 µs. In this case, the diode is capable of handling peak power dissipation of only 2 W, in which case the peak T_J climbs alarmingly close to that maximum rated temperature. We can see in Figure 9 that the junction temperature does not recover to the temperature of the die attach surface before the start of the next burst, so the T_J for the diode follows a stair-step-like curve, until the peak T_J finally reaches its steady state value of approximately 172 °C at the end of the third RF burst. At that point, the average T_J is approximately 120 °C.
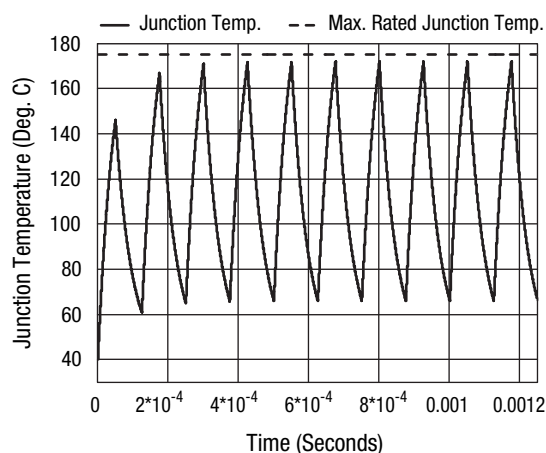

Figure 9. Diode Junction Temperature vs. Time, Duty Cycle = 50%

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Finally, consider the case where the RF burst duration is longer than $6\tau_{THERMAL}$. The plot in Figure 10 shows the junction temperature versus time for an input RF burst duration of 1.5 ms and 10% duty cycle, but with the diode dissipating 750 mW peak. Notice that the diode reaches its peak junction temperature and remains there for a substantial interval, so the fact that the signal is bursted rather than CW is not significant. The analysis of the thermal conditions for this case must be performed as if the input signal were CW, rather than a sequence of bursts.

In summary, the physical properties of the diode determine its thermal time constant (product of thermal resistance and thermal capacitance), which must be compared against the duration of the pulse which heats the diode in order to determine how much power the diode can safely dissipate without overheating.
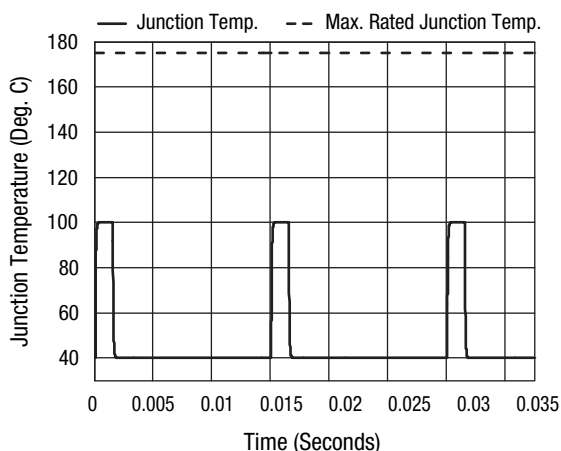
Figure 10. Diode Junction Temperature vs. Time, Burst Width = 1.5 ms, Duty Cycle = 10%

The Limiter Circuit

A typical, single-stage limiter circuit is shown in Figure 11. When a small signal, such as the input signal to a receiver, is incident upon the diode, the electric field of this signal is not large enough to force carriers into the I layer of the diode so its resistance remains high. The insertion loss of the diode in this state is primarily the mismatch loss produced by the capacitive reactance of the diode's junction capacitance. The inductor, which is present to complete the required DC circuit path, is chosen to have a sufficiently large reactance and out-of-band series resonance so that it also produces negligible in-band reflection loss.
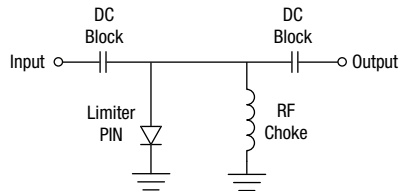
Figure 11. A Single-Stage Limiter

The Leading Edge of an RF Signal Burst

Consider what happens at the leading edge of a large signal RF burst incident upon the diode. The electric fields produced by this signal will force charge carriers into the I layer of the diode, reducing its series resistance. The series resistance of the I layer changes from its maximum value to its minimum value, assuming the amplitude of the input RF signal is sufficiently large. The low impedance of the limiter diode causes a large impedance mismatch to the transmission line, thereby reflecting almost all of the input signal power back towards the source.

Initially, when the diode is still in its high impedance state, virtually all of the input signal power passes by the diode limiter, only attenuated by the small mismatch loss from the diode's capacitance. After sufficient time has passed for the impedance of the diode to reduce to its minimum, which is approximately the carrier transit time across the I layer, the input power is attenuated by the isolation produced by the diode's low impedance. The isolation produced by

$$\text{Isolation} = 20 \log \left(\frac{Z_0}{2 \times R} \right)$$

The maximum output power from the diode is called "spike leakage." The power level out of the diode after it has changed to its low impedance is called "flat leakage." It is important to select a limiter diode such that the energy that propagates past the limiter during the output spike is sufficiently small that no damage to the following receiver stages will occur.
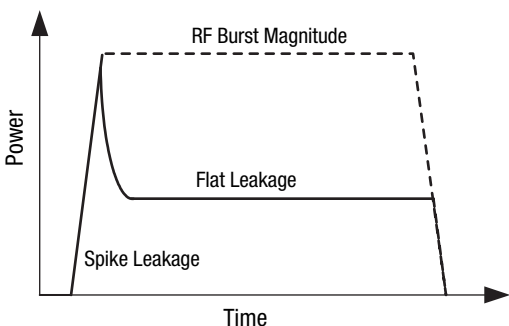
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Figure 12. Limiter Input and Output Power vs. Time

Figure 13. The Transfer Function for a Single-Stage Limiter

As implied above, even after the limiter diode has reached its low impedance state a small portion of the input signal is not reflected back to its source. Some of this energy propagates past the limiter stage to the limiter circuit's load. The balance of the input energy is dissipated by the diode, due to the Joule heating produced by the RF signal voltage across the diode's resistance. The amount of power that propagates to the load is typically 2–4 dB larger than the threshold level of the diode, again assuming the incident signal is much larger than the input threshold level. This is the case for increasing RF signal levels, until the series resistance of the limiter PIN reaches its minimum value.

If the input signal amplitude increases further, then the output power from the limiter will also increase on a dB-for-dB basis, since the finite, non-zero minimum impedance of the diode remains fixed at approximately R_{SAT}. Consequently, the reflection loss caused by the impedance mismatch also remains constant. The transfer function for a single-stage limiter is shown in Figure 13. For a practical limiter, the RF currents in the limiter diode when it is operating in its saturated mode can approach or exceed the value which will cause damage to the diode, so care should be taken to avoid operating with input signal levels that force the diode to operate well into its saturated mode region.

After the RF Signal Burst—Recovery Time

At the end of the RF input signal burst and for a brief period thereafter, there are still free charge carriers present in the diode I layer, so its resistance remains low. During this interval, the limiter is still operating in its isolation state. In a radar transceiver this means that the receiver is essentially "blind" during this interval, even though the transmitter is no longer producing its high power RF burst. The sensitivity of the receiver is temporarily degraded during this interval, since reflected signals that might arrive from a target during this interval would be attenuated by the mismatch loss of the diode's very low impedance. Clearly, the operators of radar systems would like to see the duration of this condition to be as short as possible.

After completion of the RF burst there is no externally applied electric field to force these charge carriers to be conducted out of the I layer, so the primary mechanism to eliminate them and thereby allow the diode to revert to its high impedance, low insertion loss state is recombination of the negatively charged electrons with the positively charged holes. The time that this process takes is proportional to the minority carrier lifetime of the diode, so limiter PIN diodes are treated during wafer fabrication to reduce minority carrier lifetime, without adjusting I layer thickness or junction area. In most cases, this treatment consists of the addition of gold (Au) doping to the I layer by thermal diffusion[6]. The minority carrier lifetime of an Au-doped limiter diode with a 2 µm thick I layer and a junction capacitance of 0.1 pF is approximately 5 ns. The same diode without Au doping would have minority carrier lifetime of 20 to 40 ns.

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6. Platinum (Pt) has also been used as the I layer dopant, rather than gold, but this is generally not done in modern RF/microwave limiter diode fabrication.

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Multistage Limiters

We have seen how the electrical characteristics of a limiter PIN diode are determined by the diode's geometry and by the composition of its layers. The single-stage limiter can typically produce 20–30 dB of isolation, depending on the input signal frequency and the characteristics of the diode. In most cases, much more isolation is required to protect sensitive receiver components. Multistage limiters are used for such applications.

A two-stage limiter circuit is shown in Figure 14. The limiter PIN diode at the output, commonly referred to as the "clean-up stage," is the diode with thinner I layer, selected so that the threshold level of the circuit is low enough to protect the remainder of the receiver components.
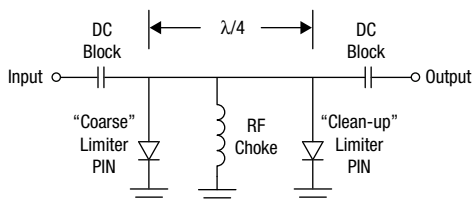
Figure 14. Two-stage limiter

The limiter diode at the input, often called the "coarse limiter," has a thicker I layer for several reasons. The P layer diameter can be larger for a diode with a thicker I layer while maintaining a capacitance value that produces low insertion loss under small input signal conditions. This produces a diode series resistance that is often smaller than that of the clean-up diode, so the isolation of the coarse limiter can be larger than that of the clean-up stage. Thermal resistance of diodes typically used as coarse limiters can also be lower than that of clean-up-type diodes.

The placement of these stages with respect to each other is important. The coarse limiter is normally placed one-quarter wavelength ($\lambda/4$), or an odd multiple of one-quarter wavelength, from the clean-up stage towards the signal source.
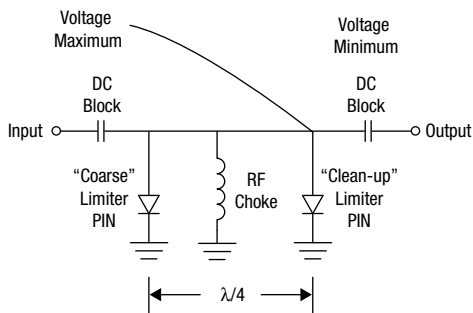
Figure 15. The Standing Wave in a Two-Stage Limiter

Under small signal conditions, both diodes are in their high impedance states, so the total insertion loss produced is a result of each diode's capacitance and the small mismatch loss they create.

At the leading edge of a large RF signal burst, both diodes are initially in their high impedance state. Consequently, for a very brief period, the entire input signal amplitude, less the small insertion loss, propagates past the limiter. The impedance of clean-up stage changes first, since the carrier transit time across its thinner I layer is less than that of the coarse diode. This establishes a standing wave on the transmission line, with a voltage minimum at the low-impedance clean-up stage. Since the coarse limiter stage is spaced $\lambda/4$ away, a voltage maximum occurs across it. This large voltage forces charge carriers into the coarse limiter I layer, thereby reducing its impedance. Consequently, the lower impedance of the coarse diode ultimately produces the majority of the overall limiting that takes place, while the clean-up stage determines the threshold level and spike leakage of the circuit.

For example, this circuit could be implemented with a 1.5 µm clean-up diode, such as CLA4603-000, and a 7 µm coarse limiter, such as CLA4607-000. The capacitance for each of these diodes is 0.2 pF maximum, and the maximum resistance specified with 10 mA forward bias current is 2 Ω. Since the coarse diode has a substantially thicker I layer, it can have a junction diameter twice that of the clean-up stage and still maintain low capacitance. This results in a much lower thermal resistance for the coarse stage (40 °C/W) than for the clean-up stage (100 °C/W), allowing it to handle larger input signals.

If the limiter is required to handle very large input signals, a third stage may be added at the limiter input, spaced another $\lambda/4$ from the second diode, which now becomes known as the "intermediate limiter." The new coarse limiter diode has an even thicker I layer diode than the intermediate stage limiter. The spike and flat leakage remain functions of the clean-up limiter I layer thickness, and the power handling and overall isolation a function of the characteristics of the three-diode cascade. More stages with increasingly thick I layers, spaced at $\lambda/4$, can be added at the input of the limiter as is required to handle extremely large signals, but most practical limiters are designed with 3 stages or less.

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Detector Limiters

The threshold level for the thinnest I layer diode available is approximately 7 dBm. Some extremely sensitive receiver components may be damaged by the spike leakage energy even at this level. The threshold level of the limiter circuit can be lowered arbitrarily by adding a Schottky detector diode and some passive components to the circuit, as shown in Figure 16.
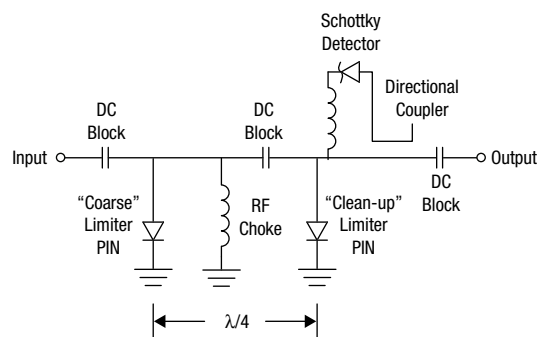

Figure 16. A Two-Stage Detector Limiter

The Schottky diode is used as a peak (envelope) detector. It is coupled to the output of the limiter circuit, often via a directional coupler. The current produced by the Schottky detector is applied as a bias current to the clean-up stage, via an RF choke. The combination of the coupling factor of the directional coupler and the barrier height of the Schottky diode determines the threshold level of this circuit, which is typically in the 0 dBm range for most practical implementations.

Conclusion

A limiter PIN diode is a three-layer device whose middle I layer is doped with Au to reduce minority carrier lifetime. The design of the diode, specifically I layer thickness, I layer resistivity and P-to-I-layer junction area is an exercise in trade-offs to produce the desired resistance, capacitance, recovery time and threshold level. The diode can be used as an input-power-controlled RF variable resistance to produce attenuation that is a function of the diode characteristics as well as the incident signal amplitude. The limiter circuit can consist of a single diode or multiple cascaded diodes separated by $\lambda/4$. Adding a directional coupler and Schottky detector diode to the system can lower threshold level.

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