

# Power MOSFET

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A **power MOSFET** is a specific type of metal oxide semiconductor field-effect transistor (MOSFET) designed to handle significant power levels. Compared to the other power semiconductor devices, for example IGBT, Thyristor, its main advantages are high commutation speed and good efficiency at low voltages. It shares with the IGBT an isolated gate that makes it easy to drive.

It was made possible by the evolution of CMOS technology, developed for manufacturing Integrated circuits in the late 1970s. The power MOSFET shares its operating principle with its low-power counterpart, the lateral MOSFET.

The power MOSFET is the most widely used low-voltage (that is, less than 200 V) switch. It can be found in most power supplies, DC to DC converters, and low voltage motor controllers.



Two power MOSFETs in the surface-mount package D2PAK. Each of these components can sustain a blocking voltage of 120 volts and a continuous current of 30 amperes.

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## Basic structure

Several structures had been explored at the beginning of the 1980s, when the first Power MOSFETs were introduced. However, most of them have been abandoned (at least until recently) in favour of the Vertical Diffused MOS (VDMOS) structure (also called Double-Diffused MOS or simply DMOS).

The cross section of a VDMOS (see figure 1) shows the "verticality" of the device: It can be seen that the source electrode is placed over the drain, resulting in a current mainly vertical when the transistor is in the on-state. The "diffusion" in VDMOS refers to the manufacturing process: the P wells (see figure 1) are obtained by a diffusion process (actually a double diffusion process to get the P and N<sup>+</sup> regions, hence the name double diffused).

Power MOSFETs have a different structure than the lateral MOSFET: as with most power devices, their structure is vertical and not planar. In a planar structure, the current and breakdown voltage ratings are both functions of the channel dimensions (respectively width and length of the channel), resulting in inefficient use of the "silicon estate". With a vertical structure, the voltage rating of the transistor is a function of the doping and thickness of the N epitaxial layer (see cross section), while the current rating is a function of the channel width. This makes possible for the transistor to sustain both high blocking voltage and high current within a compact piece of silicon.

It is worth noting that power MOSFETs with lateral structure exist. They are mainly used in high-end audio amplifiers. Their advantage is a better behaviour in the saturated region (corresponding to the linear region of a bipolar transistor) than the vertical MOSFETs. Vertical MOSFETs are designed for switching applications, so they are only used in On or Off states.

### On-state resistance

When the power MOSFET is in the on-state (see MOSFET for a discussion on operation modes), it exhibits a resistive behaviour between the drain and source terminals. It can be seen in figure 2 that this resistance (called  $R_{DS(on)}$  for "drain to source resistance in on-state") is the sum of many elementary contributions:

- $R_S$  is the source resistance. It represents all resistances between the source terminal of the package to the channel of the MOSFET: resistance of the wire bonds, of the source metallisation, and of the N<sup>+</sup> wells;
- $R_{ch}$ . This is the channel resistance. It is inversely proportional to the channel width, and for a given die size, to the channel density. The channel resistance is one of the main contributors to the  $R_{DS(on)}$  of low-voltage MOSFETs, and intensive work has been carried out to reduce their cell size in order to increase the channel density;
- $R_a$  is the access resistance. It represents the resistance of the epitaxial zone directly under the gate electrode, where the direction of the current changes from horizontal (in the channel) to vertical (to the drain contact);
- $R_{JFET}$  is the detrimental effect of the cell size reduction mentioned above: the P implantations (see figure 1) form the gates of a parasitic JFET transistor that tend to reduce the width of the current flow;
- $R_n$  is the resistance of the epitaxial layer. As the role of this layer is to sustain the blocking voltage,  $R_n$  is directly related to the voltage rating of the device. A high voltage MOSFET requires a thick, low-doped layer (i.e. highly resistive), whereas a low-voltage transistor only requires a thin layer with a higher doping level (i.e. less resistive). As a result,  $R_n$  is the main factor responsible for the resistance of high-voltage MOSFETs;

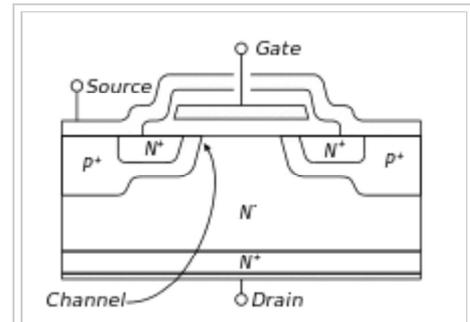


Fig. 1: Cross section of a VDMOS, showing an elementary cell. Note that a cell is very small (some micrometres to some tens of micrometres wide), and that a power MOSFET is composed of several thousand of them.

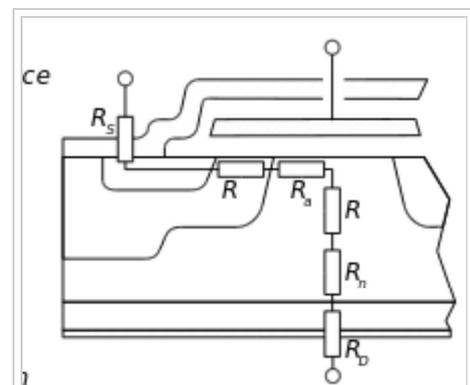


Fig.2: Contribution of the different parts of the MOSFET to the on-state resistance.

- $R_D$  is the equivalent of  $R_S$  for the drain. It represents the resistance of the transistor substrate (note that the cross section in figure 1 is not at scale, the bottom  $N^+$  layer is actually the thickest) and of the package connections.

### Breakdown voltage/on-state resistance trade-off

When in the OFF-state, the power MOSFET is equivalent to a PIN diode (constituted by the  $P^+$  diffusion, the  $N^-$  epitaxial layer and the  $N^+$  substrate). When this highly non-symmetrical structure is reverse-biased, the space-charge region extends principally on the light-doped side, i.e. over the  $N^-$  layer. This means that this layer has to withstand most of the MOSFET's OFF-state drain-to-source voltage.

However, when the MOSFET is in the ON-state, this  $N^-$  layer has no function. Furthermore, as it is a lightly doped region, its intrinsic resistivity is non-negligible and adds to the MOSFET's ON-state Drain-to-Source Resistance ( $R_{DS(on)}$ ) (this is the  $R_n$  resistance in figure 2).

Two main parameters govern both the breakdown voltage and the  $R_{DS(on)}$  of the transistor: the doping level and the thickness of the  $N^-$  epitaxial layer. The thicker the layer and the lower its doping level, the higher the breakdown voltage. On the contrary, the thinner the layer and the higher the doping level, the lower the  $R_{DS(on)}$  (and therefore the lower the conduction losses of the MOSFET). Therefore, it can be seen that there is a trade-off in the design of a MOSFET, between its voltage rating and its ON-state resistance. This is demonstrated by the plot in figure 3.

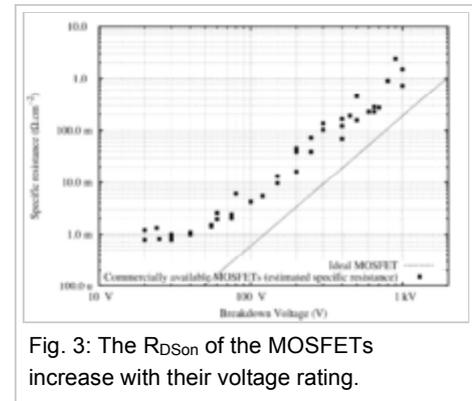


Fig. 3: The  $R_{DS(on)}$  of the MOSFETs increase with their voltage rating.

### Body diode

It can be seen in figure 1 that the source metallization connects both the  $N^+$  and  $P$  implantations, although the operating principle of the MOSFET only requires the source to be connected to the  $N^+$  zone. However, if it were, this would result in a floating  $P$  zone between the  $N$ -doped source and drain, which is equivalent to a NPN transistor with a non-connected base. Under certain conditions (under high drain current, when the on-state drain to source voltage is in the order of some volts), this parasitic NPN transistor would be triggered, making the MOSFET uncontrollable. The connection of the  $P$  implantation to the source metallization shorts the base of the parasitic transistor to its emitter (the source of the MOSFET) and thus prevents spurious latching.

This solution, however, creates a diode between the drain (cathode) and the source (anode) of the MOSFET, making it able to block current in only one direction.

Body diodes may be utilized as freewheeling diodes for inductive loads in configurations such as H-bridge or half bridge. While these diodes usually have rather high forward voltage drop, they can handle large currents and are sufficient in many applications, reducing part count, and thus, device cost and board space.

### Switching operation

Because of their unipolar nature, the power MOSFET can switch at very high speed. Indeed, there is no need to remove minority carriers as with bipolar devices.

The only intrinsic limitation in commutation speed is due to the internal capacitances of the MOSFET (see figure 4). These capacitances must be charged or discharged when the transistor switches. This can be a relatively slow process because the current that flows through the gate capacitances is limited by the external driver circuit. This circuit will actually dictate the commutation speed of the transistor (assuming the power circuit has sufficiently low inductance).

### Capacitances

In the MOSFETs datasheets, the capacitances are often named  $C_{iss}$  (input capacitance, drain and source terminal shorted),  $C_{oss}$  (output capacitance, gate and source shorted), and  $C_{rss}$  (reverse transfer capacitance, gate and source shorted). The relationship between these capacitances and those described below is:

$$C_{iss} = C_{GS} + C_{GD}$$

$$C_{oss} = C_{GD} + C_{DS}$$

$$C_{rss} = C_{GD}$$

Where  $C_{GS}$ ,  $C_{GD}$  and  $C_{DS}$  are respectively the gate-to-source, gate-to-drain and drain-to-source capacitances (see below). Manufacturers prefer to quote  $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$  because they can be directly measured on the transistor. However, as  $C_{GS}$ ,  $C_{GD}$  and  $C_{DS}$  are closer to the physical meaning, they will be used in the remaining of this article.

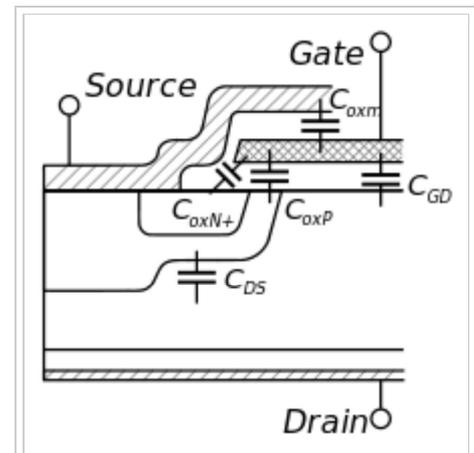


Fig. 4: Location of the intrinsic capacitances of a power MOSFET.

### Gate to source capacitance

The  $C_{GS}$  capacitance is constituted by the parallel connection of  $C_{oxN+}$ ,  $C_{oxP}$  and  $C_{oxm}$  (see figure 4). As the  $N^+$  and  $P$  regions are highly doped, the two former capacitances can be considered as constant.  $C_{oxm}$  is the capacitance between the (polysilicon) gate and the (metal) source electrode, so it is also constant. Therefore, it is common practice to consider  $C_{GS}$  as a constant capacitance, i.e. its value does not depend on the transistor state.

### Gate to drain capacitance

The  $C_{GD}$  capacitance can be seen as the connection in series of two elementary capacitances. The first one is the oxide capacitance ( $C_{oxD}$ ), constituted by the gate electrode, the silicon dioxide and the top of the  $N$  epitaxial layer. It has a constant value. The second capacitance ( $C_{GDj}$ ) is caused by the extension of the space-charge zone when the MOSFET is in off-state (see the section Blocking Voltage). Therefore, it is dependent upon the drain to source voltage. From this, the value of  $C_{GD}$  is:

$$C_{GD} = \frac{C_{oxD} \times C_{GDj}(V_{GD})}{C_{oxD} + C_{GDj}(V_{GD})}$$

The width of the space-charge region is given by <sup>[1]</sup>

$$w_{GDj} = \sqrt{\frac{2\epsilon_{Si}V_{GD}}{qN}}$$

where  $\epsilon_{Si}$  is the permittivity of the Silicon,  $q$  is the electron charge, and  $N$  is the doping level. The value of  $C_{GDj}$  can be approximated using the expression of the plane capacitor:

$$C_{GDj} = A_{GD} \frac{\epsilon_{Si}}{w_{GDj}}$$

Where  $A_{GD}$  is the surface area of the gate-drain overlap. Therefore, it comes:

$$C_{GDj}(V_{GD}) = A_{GD} \sqrt{\frac{q\epsilon_{Si}N}{2V_{GD}}}$$

It can be seen that  $C_{GDj}$  (and thus  $C_{GD}$ ) is a capacitance which value is dependent upon the gate to drain voltage. As this voltage increases, the capacitance decreases. When the MOSFET is in on-state,  $C_{GDj}$  is shunted, so the gate to drain capacitance remains equal to  $C_{oxD}$ , a constant value.

### Drain to source capacitance

As the source metallization overlaps the P-wells (see figure 1), the drain and source terminals are separated by a P-N junction. Therefore,  $C_{DS}$  is the junction capacitance. This is a non-linear capacitance, and its value can be calculated using the same equation as for  $C_{GD}$ .

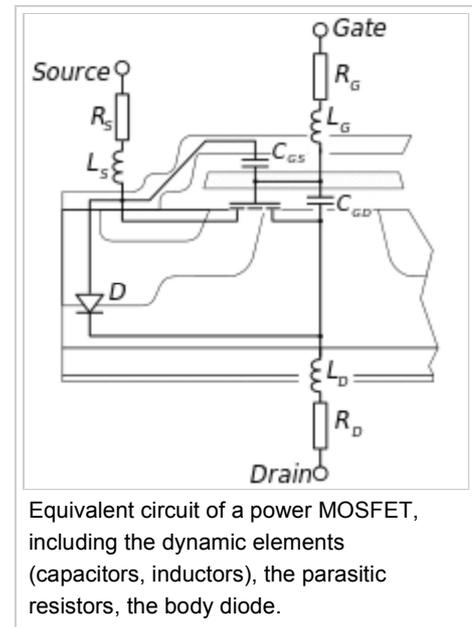
## Other dynamic elements

### Packaging inductances

To operate, the MOSFET must be connected to the external circuit, most of the time using wire bonding (although alternative techniques are investigated). These connections exhibit a parasitic inductance, which is in no way specific to the MOSFET technology, but has important effects because of the high commutation speeds. Parasitic inductances tend to maintain their current constant and generate overvoltage during the transistor turn off, resulting in increasing commutation losses.

A parasitic inductance can be associated with each terminal of the MOSFET. They have different effects:

- the gate inductance has little influence (assuming it is lower than some hundreds of nanohenries), because the current gradients on the gate are relatively slow. In some cases, however, the gate inductance and the input capacitance of the transistor can constitute an oscillator. This must be avoided as it results in very high commutation losses (up to the destruction of the device). On a typical design, parasitic inductances are kept low enough to prevent this phenomenon;
- the drain inductance tends to reduce the drain voltage when the MOSFET turns on, so it reduces turn on losses. However, as it creates an overvoltage during turn-off, it increases turn-off losses;
- the source parasitic inductance has the same behaviour as the drain inductance, plus a feedback effect that makes commutation last longer, thus increasing commutation losses.
  - at the beginning of a fast turn-on, due to the source inductance, the voltage at the source (on the die) will be able to jump up as well as the gate voltage; the internal  $V_{GS}$  voltage will remain low for a longer time, therefore delaying turn-on.
  - at the beginning of a fast turn-off, as current through the source inductance decreases sharply, the resulting voltage across it goes negative (with respect to the lead outside the package) raising the internal  $V_{GS}$  voltage, keeping the MOSFET on, and therefore delaying turn-off.



## Limits of operation

### Gate oxide breakdown

The gate oxide is very thin (100 nm or less), so it can only sustain a limited voltage. In the datasheets, manufacturers often state a maximum gate to source voltage, around 20 V, and exceeding this limit can result in destruction of the component. Furthermore, a high gate to source voltage reduces significantly the lifetime of the MOSFET, with little to no advantage on  $R_{DSon}$  reduction.

### Maximum drain to source voltage

Power MOSFETs have a maximum specified drain to source voltage (when turned off), beyond which breakdown may occur. Exceeding the breakdown voltage causes the device to conduct, potentially damaging it and other circuit elements due to excessive power dissipation.

### Maximum drain current

The drain current must generally stay below a certain specified value (maximum continuous drain current). It can reach higher values for very short durations of time (maximum pulsed drain current, sometimes specified for various pulse durations). The drain current is limited by heating due to resistive losses in internal components such as bond wires, and other phenomena such as electromigration in the metal layer.

## Maximum temperature

The junction temperature ( $T_J$ ) of the MOSFET must stay under a specified maximum value for the device to function reliably, determined by MOSFET die layout and packaging materials. The packaging often limits the maximum junction temperature, due to the molding compound and (where used) epoxy characteristics.

The maximum operating ambient temperature is determined by the power dissipation and thermal resistance. The junction-to-case thermal resistance is intrinsic to the device and package; the case-to-ambient thermal resistance is largely dependent on the board/mounting layout, heatsinking area and air/fluid flow.

The type of power dissipation, whether continuous or pulsed, affects the maximum operating temperature, due to thermal capacitance characteristics; in general, the lower the frequency of pulses for a given power dissipation, the higher maximum operating ambient temperature, due to allowing a longer interval for the device to cool down. Models, such as a Foster Network, can be used to analyze temperature dynamics from power transients.

## Safe operating area

The safe operating area defines the combined ranges of drain current and drain to source voltage the power MOSFET is able to handle without damage. It is represented graphically as an area in the plane defined by these two parameters. Both drain current and drain to source voltage must stay below their respective maximum values, but their product must also stay below the maximum power dissipation the device is able to handle. Thus the device cannot be operated at both its specified maximum drain current and maximum drain to source voltage. <sup>[2]</sup>

## Latch-up (LU)

The equivalent circuit for a MOSFET consist of one MOSFET in parallel with a parasitic BJT (Bipolar Junction Transistor). If the BJT turns ON, it cannot be turned off since the gate has no control over it. This phenomenon is known as 'latch-up', which can lead to device destruction. The BJT can be turned on due to a voltage drop across the p-type body region. To avoid latch-up, the body and the source are typically short circuited within the device package.

## Technology

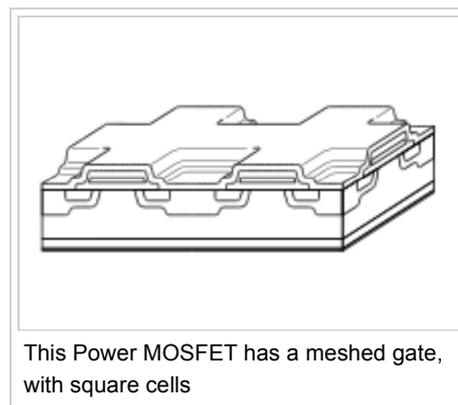
### Layout

#### Cellular structure

As described above, the current handling capability of a power MOSFET is determined by its gate channel width. The gate channel width is the third (Z-axis) dimension of the cross-sections pictured.

To minimize cost and size, it is valuable to keep the transistor's die area size as small as possible. Therefore, optimizations have been developed to increase the width of the channel surface area (i.e. increase the "channel density"). They mainly consist of creating cellular structures repeated over the whole area of the MOSFET die. Several shapes have been proposed for these cells, the most famous being the International Rectifier's "Hexfet" (hexagonal shape).

Another way to increase the channel density is to reduce the size of the elementary structure. This allows for more cells in a given surface area, and therefore more channel width. However, as the cell size shrinks, it becomes more difficult to ensure proper contact of every cell. To overcome this, a "strip" structure is often used (see figure). It is less efficient than a cellular structure of equivalent resolution in terms of channel density, but can cope with smaller pitch.



This Power MOSFET has a meshed gate, with square cells

## Structures

### P-substrate power MOSFET

A P-substrate MOSFET (often referred to as PMOS) is a MOSFET with opposite doping types (N instead of P and P instead of N in the cross-section in figure 1). This MOSFET is made using a P-type substrate, with a P<sup>-</sup> epitaxy. As the channel sits in a N-region, this transistor is turned on by a negative gate to source voltage. This makes it desirable in a buck converter, where one of the terminals of the switch is connected to the high side of the input voltage: with a N-MOSFET, this configuration requires to apply to the gate a voltage equal to  $V_{in} + V_{GS}$ , whereas no voltage over  $V_{in}$  is required with a P-MOSFET.

The main disadvantage of this type of MOSFET is the poor on-state performance: it uses holes as charge carriers, which have a much lower mobility than electrons. As resistivity is directly related to mobility, a given PMOS will have a  $R_{DSon}$  three times higher than a N-MOSFET with the same dimensions.

### VMOS

This structure has a V-groove at the gate region and was used for the first commercial devices.<sup>[3]</sup>

### UMOS (also called Trench-MOS)

In this Power MOSFET structure, the gate electrode is buried in a trench etched in the silicon. This results in a vertical channel. The main interest of the structure is the absence of the JFET effect. The name of the structure comes from the U-shape of the trench.

### Super Junction

Especially for voltages beyond 500 V some manufacturers, most notably Infineon Technologies with its CoolMOS™ products, have begun to use a charge compensation principle. Thus the resistance in the epitaxial layer as biggest contributor in high voltage MOSFETs can be reduced by a factor of greater than 5.

### Super Junction Deep-Trench Technology

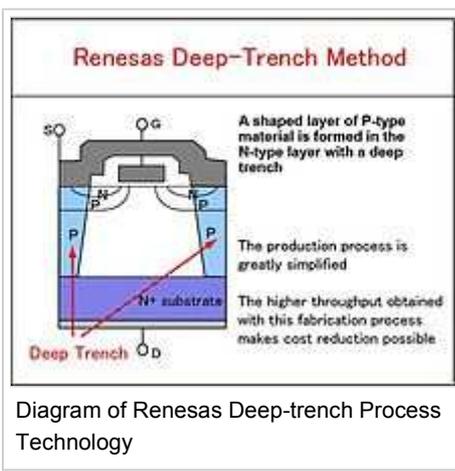
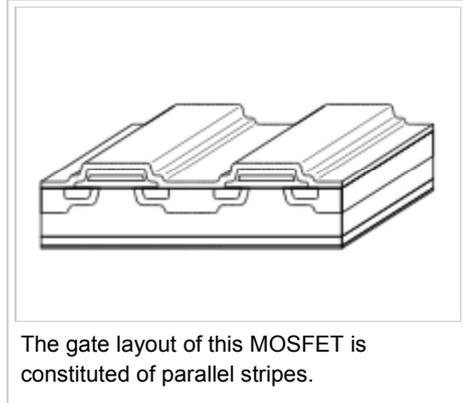
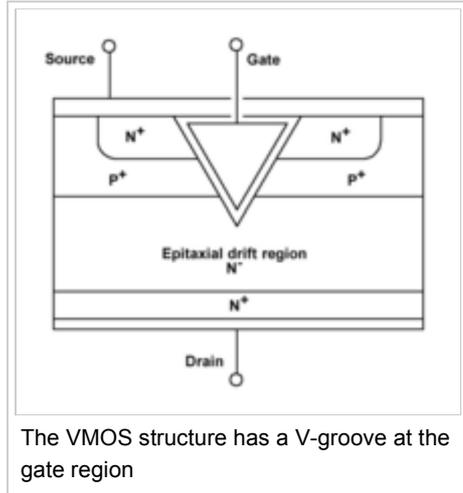


Diagram of Renesas Deep-trench Process Technology

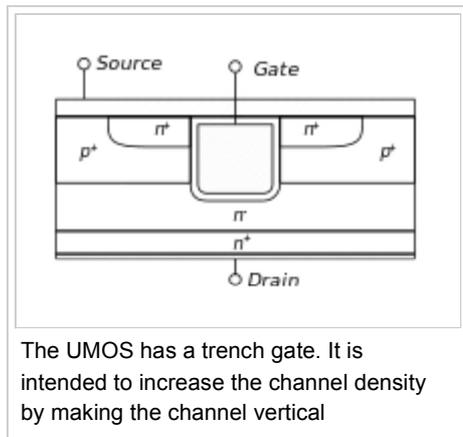
Seeking to improve the manufacturing efficiency and reliability of Super Junction MOSFETs, Renesas Electronics developed a super junction structure with a deep-trench process technique. This proprietary technology entails etching trenches in the low-impurity N-type material to form P-type regions. The Renesas process overcame problems inherent to the multi-level epitaxial growth approach and resulted in both economic benefits from manufacturing efficiency and also improved circuit design benefits of extremely low on-resistance and reduced internal capacitance. Renesas announced it's deep-trench technology in 2011.<sup>[4]</sup>



The gate layout of this MOSFET is constituted of parallel stripes.



The VMOS structure has a V-groove at the gate region



The UMOS has a trench gate. It is intended to increase the channel density by making the channel vertical

## See also

- Power electronics

## References

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## Further reading

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