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| **UČNI NAČRT PREDMETA / COURSE SYLLABUS** | | | | | | | | | | | | | | | | | |
| **Predmet:** | | | **Načrtovanje digitalnih elektronskih sistemov** | | | | | | | | | | | | | | |
| **Course title:** | | | **Digital electronic systems design** | | | | | | | | | | | | | | |
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| **Študijski program in stopnja**  **Study programme and level** | | | | | **Študijska smer**  **Study field** | | | | | | | | **Letnik**  **Academic year** | | **Semester**  **Semester** | | |
| doktorski študijski program tretje stopnje Elektrotehnika | | | | | Ni smeri | | | | | | | | 1 | |  | | |
| 3rd cycle: doctoral study programme Electrical Engineering | | | | |  | | | | | | | |  | |  | | |
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| **Vrsta predmeta / Course type** | | | | | | | | | | | | Izbirni/Elective | | | | | |
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| **Univerzitetna koda predmeta / University course code:** | | | | | | | | | | | | 64816 | | | | | |
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| **Predavanja**  **Lectures** | **Seminar**  **Seminar** | | | **Vaje**  **Tutorial** | | | **Klinične vaje**  **work** | | | | **Druge oblike študija** | | | **Samost. delo**  **Individ. work** | |  | **ECTS** |
| **30** | **20** | | |  | | |  | | | |  | | | **75** | |  | **5** |
|  | | | | | | | | | | | | | | | | | |
| **Nosilec predmeta / Lecturer:** | | | | | Andrej Žemva | | | | | | | | | | | | |
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| **Jeziki /**  **Languages:** | | **Predavanja / Lectures:** | | | | **Slovene, English** | | | | | | | | | | | |
| **Vaje / Tutorial:** | | | | **Slovene, English** | | | | | | | | | | | |
| **Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:** | | | | | | | | |  | **Prerequisits:** | | | | | | | |
| Vpis v letnik | | | | | | | | |  | Enrollment in the study year | | | | | | | |
| **Vsebina:** | | | | | | | |  | | **Content (Syllabus outline):** | | | | | | | |
| Sistemi v integriranem vezju. Tehnologija in gradniki vezij. Potek načrtovanje digitalnih elektronskih sistemov. Načrtovanje v jeziku VHDL (Very High-Speed Integrated Circuits Description Language). VHDL podatkovni tipi in modeli RTL (Register Transfer Level). Komponente, podprogrami in paketi VHDL. Komunikacijski vmesniki in vodila. Vmesniki. Predstavitev vgrajenih jeder IP (Intellectual Property) jeder: procesorji, pomnilniki, komunikacijske enote. Uporaba mehkih procesorskih jeder v programirljivih vezjih.  Hkratno načrtovanje strojne in programske opreme in modeliranje funkcionalnosti v višjenivojskih jezikih: SystemC, SpecC. Analiza zmogljivosti in delitev na strojni in programski del. Optimizacija načrtovalskega postopka strojne in programske opreme.  Testiranje digitalnih elektronskih sistemov. Modeliranje napak, simulacija vezij z napakami, avtomatsko generiranje testnih vzorcev. Načrtovanje vezij za obrobno in vgrajeno testiranje. Možnost optimizacije vezij z upoštevanjem testiranja. | | | | | | | |  | | Systems in the integrated circuit. Technology and circuit entities. Design flowchart of digital electronic systems. VHDL (Very High-Speed Integrated Circuits Description Language) systems design. VHDL data types and RTL (Register Transfer Level) models. VHDL components, subprograms and packages. Communication interfaces and buses. Interfaces. Embedded IP (Intellectual Property) cores: processors, memories, communication units. Applications of soft processor cores in programmable devices.  Hardware/Software co-design and system modeling using high-level languages: SystemC, SpecC, UML. Feasibility analysis and systems partitioning to hardware and software. Optimization of hardware and software system parts.  Testing of digital electronic systems. Fault modelling, fault simulation and automatic test pattern generation. Circuit design for boundary and built-in test. Circuit optimization exploiting testing. | | | | | | | |

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| **Temeljni literatura in viri / Readings:** | | | | | |
| [1] Tocci R, Widmer N, Moss G (2011), Digital Systems: Principles and Applications. Prentice  Hall, New Jersey  [2] Ciletti M D (2011), Advanced Digital Design with the Verilog HDL. Prentice Hall, New Jersey  [3] Mano M M (2013) Digital Design, Prentice Hall, New Jersey  [4] Tokheim R (2014), Digital Electronis: Principles and Application. McGraw-Hilll, New York  [5] A. Trost (2015), Načrtovanje digitalnih vezij v jeziku VHDL, Založba FE UL, Ljubljana | | | | | |
| **Cilji in kompetence:** | |  | | **Objectives and competences:** | |
| Posredovati temeljne raziskovalne in razvojne segmente na področju snovanja kompleksnih digitalnih elektronskih sistemov. | |  | | To present state-of-the-art research and development activity in the design of the complex digital electronic systems. | |
| **Predvideni študijski rezultati:** | | |  | **Intended learning outcomes:** | |
| Študent bo usvojil analizo in sintezo kompleksnih digitalnih elektronskih sistemov.  Na različnih načrtovalskih nivojih in z različnimi jeziki za opis vezij bo sposoben zasnovati in izdelati digitalni elektronski sistem. | | |  | Student will master analysis and design of complex digital electronic systems. They will be able to design digital system at different design levels and with different hardware description design languages. | |
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| **Metode poučevanja in učenja:** | | |  | **Learning and teaching methods:** | |
| Predavanja in vaje. | | |  | Lectures and tutorials. | |
| **Načini ocenjevanja:** | Delež (v %) /  Weight (in %) | | | | **Assessment:** |
| Poročilo in zaključen opis projekta, ustni izpit. | 50, 50 | | | | Complete design project, oral exam. |
| **Reference nosilca / Lecturer's references:** | | | | | |
| Nahtigal T, Puhar P, Žemva A (2012) A systematic approach to configurable functional verification of HW IP blocks at transaction level. Comp and Elec Eng 38:1513-1523  Trost A, Žemva A (2012) Teaching design of video processing circuits. Int Jour Elec Eng Edu 49:170-178  Nahtigal T, Žemva A (2012) Block-wise authentication method for digital images. Jour Elec Eng 63:289-295  Trost A, Žemva A (2012) Design of custom processors for the FPGA devices. Elektr Vest 79:55-60  Močnik J, Finc M, Žemva A (2013) Power consumption optimization in the smart home. Elec World 119:20-22. | | | | | |