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| **UČNI NAČRT PREDMETA / COURSE SYLLABUS** | | | | | | | | | | | | | | | | |
| **Predmet:** | | | Digitalne strukture | | | | | | | | | | | | | |
| **Course title:** | | | Digital Structures | | | | | | | | | | | | | |
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| **Študijski program in stopnja**  **Study programme and level** | | | | | **Študijska smer**  **Study field** | | | | | | | **Letnik**  **Academic year** | | **Semester**  **Semester** | | |
| Univerzitetni študijski program prve stopnje Elektrotehnika | | | | | Vse smeri | | | | | | | 2. | | zimski | | |
| 1st cycle academic study programme Electrical Engineering | | | | | All fields | | | | | | | 2. | | winter | | |
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| **Vrsta predmeta / Course type** | | | | | | | | | | | Obvezni – strokovni/ Compulsory professional | | | | | |
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| **Univerzitetna koda predmeta / University course code:** | | | | | | | | | | | 64113 | | | | | |
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| **Predavanja**  **Lectures** | **Seminar**  **Seminar** | | | **Vaje**  **Tutorial** | | | **Klinične vaje**  **work** | | | **Druge oblike študija** | | | **Samost. delo**  **Individ. work** | |  | **ECTS** |
| **45** |  | | | **45** | | |  | | |  | | | **85** | |  | **7** |
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| **Nosilec predmeta / Lecturer:** | | | | | Tadej Kotnik | | | | | | | | | | | |
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| **Jeziki /**  **Languages:** | | **Predavanja / Lectures:** | | | | slovenski / Slovenian | | | | | | | | | | |
| **Vaje / Tutorial:** | | | | slovenski / Slovenian | | | | | | | | | | |
| **Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:** | | | | | | | |  | **Prerequisites:** | | | | | | | |
| Vpis v letnik. | | | | | | | |  | Enrolment in the year of the course. | | | | | | | |

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| **Vsebina:** |  | **Content (Syllabus outline):** |
| **Številski sistemi in kode:** številski sistemi, kode in kodiranje, odkrivanje in odpravljanje napak.  **Booleova algebra:** izjave in Booleove spremen­ljivke, operacije z izjavami, aksiomi in teoremi, načini dokazovanja teoremov.  **Preklopne funkcije in logična vrata:** oblike funkcij, metode poenostavljanja in pretvorbe med oblikami, Karnaughov diagram in pravilnostna tabela, funkcijsko polni sistemi, logična vrata in vezja, hazard v logičnih vezjih, tehnološke izvedbe logičnih vezij in njihove lastnosti, tehnologija CMOS.  **Kombinacijska vezja:** kodirniki in dekodirniki, multipleksorji in demultipleksorji, primerjalniki enakosti in velikosti, seštevalniki, množilniki, aritmetično-logična enota.  **Računalniško podprto načrtovanje digitalnih struktur:** minimizatorji, urejevalniki shemat-skih prikazov, simulatorji vezij, strojno opisni jeziki, sintetizatorji geometrije tiskanih vezij.  **Sekvenčna vezja:** spominske celice, pravilnostna in vzbujalna tabela, stabilizatorji preklopnikov, registri, števci, pomikalni registri, krožni števci, vzbujalne enačbe, tabela in diagram stanj, analiza in sinteza sekvenčnih vezij.  **Tristanjski izravnalniki in vodila:** izravnalnik, izravnalnik s histerezo, tristanjski izravnalniki in serijska vodila, tristanjski vmesniki in paralelna vodila.  **Programirljiva vezja:** pomnilna mreža, ROM, PROM, EPROM, EEPROM, Flash, PLA, PAL, GAL, SRAM, DRAM, CPLD, FPGA. Uporaba strojno opisnega jezika za realizacijo kombina­cijskih in sekvenčnih vezij s CPLD in FPGA.  **Dodatne vsebine (podane v primeru razpoložljivega časa, a ne sodijo v izpitno snov):** mikrokrmilniki, mikroprocesorji, analog-no-digitalni in digitalno-analogni pretvorniki, generatorji takta in urinih pulzov. |  | **Number systems and codes:** number systems, codes, encoding, error detection and correction.  **Boolean algebra:** propositional logic, Boolean variables, basic operations, derived operations, axioms and theorems, proofs of theorems.  **Boolean functions and logic gates:** representa-tions, methods of simplification and conversion, Karnaugh map and truth table, logic gates and circuits, functionally complete sets of operations, timing hazards, logic families and technologies and their characteristics, CMOS technology.  **Combinational logic circuits:** encoders and decoders, multiplexers and demultiplexers, comparators, adders, multipliers, arithmetic-and-logic units.  **Computer-aided digital design:** minimizers, schematic editors, circuit simulators, hardware description languages, PCB layout designers,  IC layout designers.  **Sequential logic circuits:** latches and flip-flops, truth table and excitation table, switch debouncers, registers, counters, shift registers, ring counters, excitation equations, state table and state diagram, analysis and synthesis of sequential logic circuits.  **Three-state buffers and buses:** buffer, Schmitt-trigger buffers, three-state buffers, serial buses, parallel buses.  **Programmable logic circuits:** storage matrix, ROM, PROM, EPROM, EEPROM, Flash, PLA, PAL, GAL, SRAM, DRAM, CPLD, FPGA. Use of hardware description languages for implementation of combinational and sequential logic in CPLD and FPGA circuits  **Additional topics (in case of spare time, but not required in exams):** microcontrollers, microprocessors, analog-digital and digital-analog converters, clock generators. |

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| **Temeljni literatura in viri / Readings:** | | | |
| 1. J. F. Wakerly. Digital Design: Principles and Practices, 4th ed. Pearson/Prentice Hall, 2006. 2. M. Morris Mano, M. D. Ciletti. Digital Design, 4th ed. Pearson/Prentice Hall, 2007. 3. W. Kleitz. Digital Electronics, 9th ed. Pearson, 2012. 4. C. Maxfield. Bebop to the Boolean Boogie, 3rd ed. Newnes, 2009. 5. G. Pucihar, T. Kotnik. Digitalne strukture: Zbirka rešenih nalog. Založba FE in FRI, 2011. | | | |
| **Cilji in kompetence:** |  | | **Objectives and competences:** |
| Spoznati teoretične osnove logičnega odločanja in pomnjenja v digitalnih strukturah. Pridobiti znanje za praktično načrtovanje, izdelavo in preizkušanje digitalnih struktur. |  | | To gain the basic theoretical understanding of functioning of digital structures. To acquire the knowledge and basic experience of practical design, implementation and testing of digital structures. |
| **Predvideni študijski rezultati:** | |  | **Intended learning outcomes:** |
| **Znanje in razumevanje:** Študent bo razumel osnove delovanja kombinacijskih in sekvenčnih digitalnih struktur. Znal bo analizirati njihovo delovanje, ga opisati v enem od strojno opisnih jezikov in izvesti načrtovanje, abstraktno in strukturno sintezo ter preizkušanje digitalnih struktur. Pridobil bo tudi osnovno znanje za praktično izdelavo digitalnih vezij s sodobnimi računalniško podprtimi metodami.  **Uporaba:** Samostojna analiza, načrtovanje, abstraktna in strukturna sinteza, preizkušanje in izdelava digitalnih struktur s klasičnimi in sodobnimi metodami.  **Refleksija:** Študent bo sposoben oceniti in izbrati najugodnejšo izvedbo digitalne strukture glede na funkcionalno obsežnost, ekonomičnost in zanesljivost delovanja načrtovanega sistema.  **Prenosljive spretnosti:** Sposobnost samostojne analize delovanja digitalnih struktur; sposobnost samostojnega načrtovanja, abstraktne in strukturne sinteze ter preizkušanja prototipov digitalnih struktur; poznavanje in osnovne izkušnje z uporabo sodobnih računalniško podprtih metod za načrtovanje, analizo in simulacijo delovanja digitalnih struktur. | |  | **Knowledge and understanding:** The students will gain the basic understanding of the functioning of combinational and sequential digital logic. They will be able to analyze their operations, describe them in one of the hardware description languages, design logic circuits and test them. They will also gain the basic knowledge of digital design with modern computer-aided methods.  **Application:** Independent analysis, design, abstract and structural synthesis, testing and construction of digital structures using classical and modern methods and tools.  **Reflection:** The students will be able to evaluate and choose the most suitable technology and design of a digital logic system with regard to the requirements of complexity, cost efficiency, and reliability.  **Transferrable skills:** Ability to individually analyze functioning of digital logic systems; ability to individually design, synthesize on the abstract and structural level, as well as test prototypes of digital systems; knowledge and basic experience with modern computer-aided methods for design, analysis and simulation of digital logic systems |

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| **Metode poučevanja in učenja:** | |  | **Learning and teaching methods:** | |
| Predavanja z vključenimi primeri reševanja nalog za poglabljanje razumevanja teoretičnih osnov, laboratorijske vaje za pridobivanje sa-mostojnih praktičnih izkušenj z načrtovanjem, realizacijo in preizkušanjem digitalnih vezij. | |  | Lecture classes with examples of problem solving to illustrate the theoretical concepts, laboratory work for acquisition of practical skills in design, implementation and testing of digital logic circuits. | |
| **Načini ocenjevanja:** | Delež (v %) /  Weight (in %) | | | **Assessment:** |
| Pogoj za opravljanje izpita je pozitivna ocena laboratorijskih vaj (50 ≤ L ≤ 100), pisni izpit pa študent opravi, če zbere vsaj polovico točk (50 ≤ P ≤ 100). V tem primeru se določi izhodišče za končno oceno (I), I = (2P + L)/3, iz katerega sledi predlog končne ocene pri predmetu (K):  • 90 < I ≤ 100: K = 10  • 80 ≤ I ≤ 90: K = 9  • 70 ≤ I < 80: K = 8  • 60 ≤ I < 70: K = 7  • 50 ≤ I < 60: K = 6  Pri 50 ≤ P < 67 je obvezen ustni zagovor izpita, študent pa z uspešnim zagovorom potrdi oceno K. Pri 67 ≤ P ≤ 100 študent izbira med vpisom predlagane ocene K in ustnim zagovorom, s slednjim pa lahko končno oceno tako izboljša kot poslabša. | ocena vaj 33.33%;  ocena izpita 66.67%;  ustni zagovor lahko oceno potrdi, izboljša ali poslabša  /  lab work gra-de contributes 1/3, and exam grade 2/3 to the final grade; verbal exam can result in confirmation, reduction or increase of the grade | | | The necessary condition for entering the written examination is a positive grade in lab work (50 ≤ L ≤ 100), and written exam is passed if half or more points are gained (50 ≤ P ≤ 100). If these require-ments are met, a tentative basis for the final grade (K) is determined as follows:  I = (2P + L)/3,  • 90 < I ≤ 100: K = 10  • 80 ≤ I ≤ 90: K = 9  • 70 ≤ I < 80: K = 8  • 60 ≤ I < 70: K = 7  • 50 ≤ I < 60: K = 6  For 50 ≤ P < 67, the written exam is follo-wed by a verbal one, and with adequate understanding demonstrated, the stu-dent gets the grade K. For 67 ≤ P ≤ 100, the student chooses between accepting grade K and attending the verbal exam, where based on the adequacy of demonstrated understanding, grade K can be confirmed, reduced or increased. |
| **Reference nosilca / Lecturer's references:** | | | | |
| 1. **KOTNIK, Tadej**, MIKLAVČIČ, Damijan. Second-order model of membrane electric field induced by alternating external electric fields. *IEEE transactions on bio-medical engineering*, 2000, vol. 47, no. 8, str. 1074-1081.  2. FLISAR, Karel, PUC, Marko, **KOTNIK, Tadej**, MIKLAVČIČ, Damijan. Cell membrane electroper-meabilization with arbitrary pulse waveforms. *IEEE engineering in medicine and biology magazine*,2003, vol. 22, no. 1, str. 77-81.  3. REBERŠEK, Matej, MARJANOVIČ, Igor, BEGUŠ, Samo, PILLET, Flavien, ROLS, Marie-Pierre, MIKLAVČIČ, Damijan, **KOTNIK, Tadej**. Generator and setup for emulating exposures of biological samples to lightning strokes. *IEEE transactions on bio-medical engineering*, 2015, vol. 62, no. 10, str. 2535-2543.  4. **KOTNIK, Tadej***. Digitalne strukture: Učno gradivo s predavanj*. Ljubljana: Fakulteta za elektro-tehniko, 2010. (http://lbk.fe.uni-lj.si/pdfs/DS-Predavanja.pdf)  5. PUCIHAR, Gorazd, **KOTNIK, Tadej**. *Digitalne strukture: Zbirka rešenih nalog*. Ljubljana: Založba FE in FRI, 185 str., 2011. | | | | |