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| **UČNI NAČRT PREDMETA / COURSE SYLLABUS** | | | | | | | | | | | | | | | | | |
| **Predmet:** | | | Preizkušanje elektronskih vezij | | | | | | | | | | | | | | |
| **Course title:** | | | Testing of electronic circuits | | | | | | | | | | | | | | |
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| **Študijski program in stopnja**  **Study programme and level** | | | | | **Študijska smer**  **Study field** | | | | | | | | **Letnik**  **Academic year** | | **Semester**  **Semester** | | |
| Univerzitetni študijski program druge stopnje Elektrotehnika | | | | | vse smeri, Elektronika | | | | | | | | 1. | | poletni | | |
| 2nd cycle master study programme Electrical Engineering | | | | | All fields, Electronics | | | | | | | | 1. | | summer | | |
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| **Vrsta predmeta / Course type** | | | | | | | | | | | | izbirni modul D, strokovni  elective module D, professional | | | | | |
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| **Univerzitetna koda predmeta / University course code:** | | | | | | | | | | | | 059 | | | | | |
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| **Predavanja**  **Lectures** | **Seminar**  **Seminar** | | | **Vaje**  **Tutorial** | | | **Klinične vaje**  **work** | | | | **Druge oblike študija** | | | **Samost. delo**  **Individ. work** | |  | **ECTS** |
| **45** |  | | | **30 (0A+30L)** | | |  | | | |  | | | **75** | |  | **6** |
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| **Nosilec predmeta / Lecturer:** | | | | | Prof. dr. Andrej Žemva | | | | | | | | | | | | |
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| **Jeziki /**  **Languages:** | | **Predavanja / Lectures:** | | | | Slovenski / Slovene  (English possible) | | | | | | | | | | | |
| **Vaje / Tutorial:** | | | | Slovenski / Slovene  (English possible) | | | | | | | | | | | |
| **Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:** | | | | | | | | |  | **Prerequisits:** | | | | | | | |
| Vpis v prvi letnik podiplomskega magistrskega študijskega programa Elektrotehnika druge stopnje, poznavanje elektronskih vezij. | | | | | | | | |  | Enrolment in the 1st year of 2nd cycle master study programme in Electrical Engineering, basic knowledge of electronic circuits. | | | | | | | |
| **Vsebina:** | | | | | | | |  | | **Content (Syllabus outline):** | | | | | | | |
| UVOD:  Pomen in vloga testiranja, testiranje digitalnih, analognih in mešanih vezij, vpliv tehnologije izdelave vezij VLSI na testiranje.  TESTNI POSTOPKI ZA VEZJA VLSI IN TESTNA OPREMA:  Kako testiramo integrirana vezja? Vrste testiranja. Oprema za avtomtasko testiranje.  EKONOMIJA TESTIRANJA IN KAKOVOST VEZIJ:  Gospodarski vidik testiranja, strošek testiranja, izplen, delež napak, ocena deleža napak.  MODELIRANJE NAPAK:  Vrste napak, funkcijsko in strukturno testiranje, model enojnih in večkratnih napak,  modeliranje stika med povezavami.  LOGIČNA SIMULACIJA IN SIMULACIJA NAPAK:  Modeliranje vezij za logično simulacijo na različnih stopnjah, algoritmi za logično simulacijo, algoritmi za simulacijo napak.  AVTOMATSKA GENERACIJA TESTNIH VEKTORJEV:  Definicija generacije testnih vektorjev, identifikacija redundantnih napak, sistemi za avtomatsko generacijo testnih vektorjev, testiranje sinhronih in asinhronih sekvenčnih vezij.  TESTIRANJE POMNILNIŠKIH VEZIJ:  Analiza možnih napak, metode testiranja pomnilniških vezij.  TESTIRANJE ANALOGNIH IN MEŠANIH VEZIJ:  Funkcijsko DSP-testiranje, metode testiranja ADC in DAC gradnikov, modelno testiranje.  TESTIRANJE ZAKASNITEV:  Problem testiranja zakasnitev, pristopi k testiranju in ugotavljanju zakasnitev v vezjih.  TEST IDDQ:  Princip testiranja IDDQ in pregled metod, učinkovitost in omejitve testiranja IDDQ.  NAČRTOVANJE TESTIRANJA:  Metode in pravila za načrtovanja vezij z upoštevanjem testiranja, delni-scan načrt vezja, izvedbe scan-vezij.  VGRAJENI TESTI:  Stroški vgrajenega testa, generiranje testnih vektorjev za vgrajeni test, vstavljanje testnih točk, vgrajeno testiranje pomniških vezij.  STANDARD ZA OBROBNO TESTIRANJE:  Namen standarda, konfiguracija vezja za obrobno testiranje po standardu IEEE 1149.1 (JTAG), vodilo ATP (Analog Test Bus), ciljne napake v analognih vezjih, obrobno testiranje analognih vezij.  TESTIRANJE SISTEMOV  Sistemsko testiranje, funkcijsko in diagnostično testiranje (slovar napak, diagnostično drevo, primer sistemskega testa mikroprocesorja), testna arhitektura za sisteme v čipu. | | | | | | | |  | | INTRODUCTION:  Role of testing, digital, analog and mixed signal test, VLSI technology trends affecting testing.  VLSI TESTING PROCESS AND TEST EQUIPMENT:  How to test chips? Types of testing, automatic test equipment.  TEST ECONOMICS AND PRODUCT QUALITY:  Test economics, costs of testing, yield, defect level, defect level estimation.  FAULT MODELING:  Types of defects, faults and errors, functional and structural testing, single stuck-at and multiple faults model, bridging fault model.  LOGIC AND FAULT SIMULATION:  Circuit modelling for logic simulation at different levels, algorithms for logic simulation, algorithms for fault simulation.  AUTOMATIC TEST-PATTER GENERATION:  Definition of test-pattern generator, redundancy identification, systems for automatic test pattern generation, testing of synchronous and asynchronous sequential circuits.  MEMORY TEST:  Failure analysis, test methods of memory devices.  ANALOG AND MIXED-SIGNAL TEST:  Functional DSP-based testing, test methods of ADC and DAC devices, model-based testing.  DELAY TEST:  Delay test problem, delay test methodologies, practical considerations in delay testing.  TEST IDDQ:  IDDQ test principle and survey of IDDQ methods, effectiveness and limitations of IDDQ test.  DESIGN FOR TESTABILITY:  DFT methods and DFT rules, scan design rules, scan and partial-scan design, variations of scan designs.  BUILT-IN SELF-TEST (BIST):  The economic case of BIST, test-pattern generation for BIST, test points insertion, memory BIST.  BOUNDARY SCAN STANDARD:  Purpose of standard, circuit configuration with boundary standard IEEE 1149.1 (JTAG), analog test bus (ATB), targeted analog faults, boundary scan in analog circuits.  SYSTEM TEST  System test and core based design, functional and diagnostic test (fault dictionary, diagnostic tree, a microprocessor system test example), test architecture for system-on-a-chip (SOC). | | | | | | | |

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| **Temeljni literatura in viri / Readings:** | | | | | |
| 1. GIZOPOULOS, Dimitris (Ed.). Advances in Electronic Testing: Challenges and Methodologies, Springer, 2006.  2. WUNDERLICH, Hans-Joachim. Models in Hardware Testing, Springer Verlag, 2010.  3. BUSHNELL, Michael, AGRAWAL, Wishwani. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Springer Publishing Company, 2013.  4. NAVABI, Zainalabedi. Digital System Test and Testable Design: Using HDL Models and Architectures, Springer, 2011. | | | | | |
| **Cilji in kompetence:** | |  | | **Objectives and competences:** | |
| * osvojiti znanje o možnih vzrokih napak v elektronskih vezjih, njihovem odkrivanju in diagnozi, * seznanitev z modeliranjem napak pri zasnovi in izdelavi vezja, * poznavanje algoritmov za simulacijo napak in avtomatsko generacijo testnih vzorcev, * poznavanje algoritmov in metod za odkrivanje zakasnitev, * obvladovanje tehnik za načrtovanje vezij z upoštevanjem testiranja, * praktični pristopi k načrtovanju in testiranju elektronskih vezij. | |  | | * to acquire the knowledge of reasons for circuit defects, errors and faults, their detection and diagnosis, * knowledge on fault modelling for various design errors and circuit implementation defects, * knowledge of fault simulation and automatic test-pattern generation algorithms, * knowledge of algorithms and methods for delay testing, * to master techniques for circuit design for testability, * practical approaches of design and test of electronic circuits. | |
| **Predvideni študijski rezultati:** | | |  | **Intended learning outcomes:** | |
| * temeljno znanje o testiranju vezij, * razumevanje pomena testiranja pri načrtovanju in izdelavi elektronskih vezij, * samostojnost pri izbiri testne metode in sposobnost testiranja in diagnoze napak, * znanje za načrtovanje elektronski vezij z upoštevanjem testiranja, * znanje za nadaljnji študij na področju snovanja in testiranja elektronskih vezij. | | |  | * fundamental knowledge of circuit testing, * understanding of testing role in design and implementation of electronic circuits, * self-dependence by selecting the proper testing method and ability to test and fault diagnosis, * knowledge of design for testability, * knowledge of further studies on advanced circuit design and test. | |
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| **Metode poučevanja in učenja:** | | |  | **Learning and teaching methods:** | |
| * predavanja (prosojnice v kombinaciji s tablo), * laboratorijske vaje (praktično delo z ugotavljanjem napak in diagnozo napak v digitalnih analognih in mešanih integriranih vezjih. | | |  | * lectures (slides and blackboard) * laboratory assignments (hands on fault detection and fault diagnosis in digital, analog and mixed-signal integratedcircuits. | |
| **Načini ocenjevanja:** | Delež (v %) /  Weight (in %) | | | | **Assessment:** |
| Način: laboratorijske vaje, pisni izpit, ustni izpit.  Ocene od 1 do vključno 5 so negativne, ocene od vključno 6 do 10 so pozitivne.  Pozitivna ocena laboratorijskih vaj je pogoj za pristop k izpitu.  Prispevki k oceni:  laboratorijske vaje  pisni izpit  ustni izpit | 50%  25%  25% | | | | Type: laboratory exercises, written exam, oral exam.  Negative grades: from 1 to 5, positive grades: from 6 to 10.  Positive evaluation of laboratory exercises is a prerequisite for the exam.  Contributions to final grade:  laboratory exercises  written exam  oral examination |
| **Reference nosilca / Lecturer's references:** | | | | | |
| 1. MOČNIK, Jure, ŽEMVA, Andrej. Controlling voltage profile in smart grids with remotely controlled switches. *IET generation, transmission & distribution*, 2014, vol. 8, no. 8, str. 1499-1508.  2. TOMAŽIČ Jure, ŽEMVA, Andrej. Efficient and lightweight battery management system contributes to victory in the Green Flight Challenge 2011. *Electric power systems research*, 2013, vol. 98, no. 5, str. 70-76.  3. MOČNIK, Jure, HUMAR, Janez, ŽEMVA, Andrej. A non-conventional intrument transformer. *Measurement*, 2013, vol. 46, no 10, str. 4114-4120.  4. SLUGA, Janez, ZALETELJ, Viktor, ŽEMVA, Andrej. Agent control for reconfigurable open kinematic chain manipulators. *International journal of advanced robotic systems*, 2013, vol. 10, no. 353, str. 1-13.5. BAŠA, Kristjan, ŽEMVA, Andrej.Simulation and verification of a dynamic model of the electric forklift truck. *Intelligent automation and soft computing*, 2011, vol. 17, no. 1, str. 13-30.  5. BAŠA, Kristjan, ŽEMVA, Andrej. Simulation and verification of a dynamic model of the electric forklift truck. *Intelligent automation and soft computing*, 2011, vol. 17, no. 1, str. 13-30. | | | | | |