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| **UČNI NAČRT PREDMETA / COURSE SYLLABUS** | | | | | | | | | | | | | | | | | |
| **Predmet:** | | | Analogna integrirana vezja in sistemi | | | | | | | | | | | | | | |
| **Course title:** | | | Analogue Integrated Circuits and Systems Design | | | | | | | | | | | | | | |
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| **Študijski program in stopnja**  **Study programme and level** | | | | | **Študijska smer**  **Study field** | | | | | | | | **Letnik**  **Academic year** | | **Semester**  **Semester** | | |
| Podiplomski magistrski študijski program druge stopnje Elektrotehnika | | | | | Elektronika | | | | | | | | 1 | | 2 | | |
| 2nd cycle masters study programme in Electrical Engineering | | | | | Electronics | | | | | | | | 1 | | 2 | | |
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| **Vrsta predmeta / Course type** | | | | | | | | | | | | Obvezni-strokovni / Compulsory professional | | | | | |
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| **Univerzitetna koda predmeta / University course code:** | | | | | | | | | | | | 64228 | | | | | |
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| **Predavanja**  **Lectures** | **Seminar**  **Seminar** | | | **Vaje**  **Tutorial** | | | **Klinične vaje**  **work** | | | | **Druge oblike študija** | | | **Samost. delo**  **Individual. work** | |  | **ECTS** |
| **45** |  | | | **30** | | |  | | | |  | | | **75** | |  | **6** |
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| **Nosilec predmeta / Lecturer:** | | | | | Anton Pleteršek | | | | | | | | | | | | |
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| **Jeziki /**  **Languages:** | | **Predavanja / Lectures:** | | | | **Slovenščina in angleščina/Slovene and English** | | | | | | | | | | | |
| **Vaje / Tutorial:** | | | | **Slovenščina in angleščina/Slovene and English** | | | | | | | | | | | |
| **Pogoji za vključitev v delo oz. za opravljanje študijskih obveznosti:** | | | | | | | | |  | **Prerequisits:** | | | | | | | |
| Vpis v letnik. | | | | | | | | |  | Enrolment in the year of the course. | | | | | | | |
| **Vsebina:** | | | | | | | |  | | **Content (Syllabus outline):** | | | | | | | |
| OSNOVNI PRINCIPI: predstavitev, pregled, primerjava in možnosti modernih CMOS in BiCMOS tehnologij ter osnovni pasivni in aktivni gradniki (upori, kondenzatorji, tuljave, diode, bipolarni transistorji, MOS transistorji itd.) ter njihovi nizkofrekvenčni in visokofrekvenčni modeli, šum. Projekcija lastnosti osnovni elementov v nanometerskih tehnologijah. NAČRTOVANJE: geometrije osnovnih elementov v izbranih tehnologijah ter načrtovalska pravila. Pregled orodij za načrtovanje ter njihova uporaba ( shematski vnos, simulacija in optimizacija vezja, ročno in avtomatsko načrtovanje geometrije, verifikacija načrtovalskih pravil DRC in avtomatska primerjava sheme in geometrije. OSNOVNI DIGITALNI GRADNIKI: Načrtovanje osnovnih digitalnih gradnikov na tranzistorskem nivoju ter visokonivojski modeli. OSNOVNI ANALOGNI GRADNIKI: Načrtovanje osnovnih analognih gradnikov (tokovna zrcala in izvori, tokovne in napetostne reference, diferencialne stopnje, izhodne stopnje, diferencialni ojačevalniki (stabilnost in kompenzacija), transkonduktačni ojačevalniki, komparatorji, translinearni elementi) ter modeli. OSNOVNI ANALOGNI MODULI: Načrtovanje vezja osnovnih analognih modulov: osnovni SC in gmC modul, oscilatorji, ter tehnološke omejitve (pod 100nm), AD in DA pretvornik s poudarkom na nizki napajalni napetosti (pod 1V) in nizki porabi moči (LPLV). Pregled in projekcija lastnosti osnovnih modulov v nano-metrskih tehnologijah.  Primeri načrtovanja LPLV (RFID sistemi – mešana analogno digitalna vezja in standardi).  VHODNO VHODNO/IZHODNE ENOTE: predstavitev ESD in thyristorskega efekta ter periferna vezja, za zaščito. | | | | | | | |  | | BASIC principles: Integrated circuit technologies, CMOS, BiCMOS and comparison. Active and passive devices available in CMOS technology.  Modeling and integration of passive devices like integrated inductors, focused on high frequency (RF). Parameters and devices performance comparison with scaled down technologies to 100nm and beyond.  IC circuit design, circuit geometry, design rules, process documentation.  Professional VLSI design CAD tools that composed of schematic and geometry entry, layout versus schematic verification,  Circuit analysis (HSPICE), worst-case analysis.  Chip geometry design, constrains, design rules (DRC), technology limitations, design for matching, high frequency layout, mixed signal layout guidelines  BASIC OF DIGITAL design, sequential logic and gates on MOS device level.  ANALOG circuit design: Requirements and constraints, basic guidelines. Basic building blocks like current mirrors, current and voltage references, bandgap reference sources, low noise amplifiers, power amplifiers, current and voltage comparators and their applications in more complex analog block design (D/A, A/D, RF circuits, oscillators, basic SC and gm\_C modul). Focus on LPLV (low power, low voltage) circuit architectures, low supply voltage design hints and expected performances (design for supply below 1V). Technologies limitations - focus on solutions in technologies below 100 nm and search for new architectures for amplifiers and other modules, suitable for integration SoC (systems on chip - mix signal design – RFID as an example).  I/O PERIPHERAL structures with focus on solutions for electrostatic discharge ESD, electromagnetic compatibility EMC, and robustness to latch-up. | | | | | | | |

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| **Temeljni literatura in viri / Readings:** | | | | | |
| 1. P.R. Gray, "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons, Inc. 2001, 2. C. Tomazou, G. Moschytz, B. Golbert, "Trade-offs in Analog Circuit Design," Kluwer 2002. 3. R.J.Baker, "CMOS: Circuit Design, Layout, and Simulation, 2nd, Revised Edition," Wiley 2007, 4. A. Pleteršek, "Načrtovanje analognih integriranih vezij v tehnologijah CMOS in BiCMOS, " 1. izd. Ljubljana: Fakulteta za elektrotehniko, 2006, 5. Predavanja se posodabljajo vsako leto, so v ang. jeziku in so skupaj z nalogami na razpolago na spletni strani predmeta: [http://lmfe.fe.uni-lj.si/wp-content/uploads/2016/03/lectures2010-2016.pdf](https://mail-fe.fe1.uni-lj.si/owa/redir.aspx?SURL=Z3bORtEDPrrt1G0hjxVH3mmm-7ellsrWnFi0j_6yk-ZH9_w9TnjTCGgAdAB0AHAAOgAvAC8AbABtAGYAZQAuAGYAZQAuAHUAbgBpAC0AbABqAC4AcwBpAC8AdwBwAC0AYwBvAG4AdABlAG4AdAAvAHUAcABsAG8AYQBkAHMALwAyADAAMQA2AC8AMAAzAC8AbABlAGMAdAB1AHIAZQBzADIAMAAxADAALQAyADAAMQA2AC4AcABkAGYA&URL=http%3a%2f%2flmfe.fe.uni-lj.si%2fwp-content%2fuploads%2f2016%2f03%2flectures2010-2016.pdf) 6. Priprave in vsebina laboratorijskih vaj se posodablja letno in je na razpolago na spletni strani predmeta: [http://lmfe.fe.uni-lj.si/wp-content/uploads/2016/03/vaje-2014-16.pdf](https://mail-fe.fe1.uni-lj.si/owa/redir.aspx?SURL=wCNH-KPlD0dpoKn5bxRSYLt5MJC-XHMuz-k6fLzUd9tH9_w9TnjTCGgAdAB0AHAAOgAvAC8AbABtAGYAZQAuAGYAZQAuAHUAbgBpAC0AbABqAC4AcwBpAC8AdwBwAC0AYwBvAG4AdABlAG4AdAAvAHUAcABsAG8AYQBkAHMALwAyADAAMQA2AC8AMAAzAC8AdgBhAGoAZQAtADIAMAAxADQALQAxADYALgBwAGQAZgA.&URL=http%3a%2f%2flmfe.fe.uni-lj.si%2fwp-content%2fuploads%2f2016%2f03%2fvaje-2014-16.pdf) | | | | | |
| **Cilji in kompetence:** | |  | | **Objectives and competences:** | |
| Cilj predmeta je pridobiti znanja s področja načrtovanja analognih integriranih vezji in VLSI sistemov. | |  | | This lecture builds the foundation for understanding the analogue integrated circuit design. The objective is to become familiar with the many fundamentals required to design high-performance analog circuits. | |
| **Predvideni študijski rezultati:** | | |  | **Intended learning outcomes:** | |
| Znanje in razumevanje:  Študent bo sposoben iz podanih sistemskih zahtev realizirati preprosto analogno integrirano vezje v enem od tehnoloških procesov (CMOS in BiCMOS) z uporabo načrtovalskih orodij.  Prenosljive/ključne spretnosti in drugi atributi:   * *Spretnosti komuniciranja:* pisna in ustna predstavitev rezultatov dela in raziskav. * *Razumevanje in priprava dokumentacije IC vezja.* * *Spretnosti računanja:* inženirski pristop k ocenjevanju parametrov in nabiranje ter uporaba preteklih izkušenj. * *Reševanje problemov:* razumevanje problemov in iskanje najugodnejše rešitve z upoštevanjem tehnoloških omejitev. * *Učenje za razmišljanje* | | |  | Knowledge and understanding:  The student will be able to understand adequate technology and analog circuit, and evaluate the feasibility to fulfill the system requirements; understand the CMOS and BiCMOS processes and parameters and use design tools for IC design in Linux environment.  Transferable/Key skills and other attributes:   * *Communication skills:* oral and written presentation of research work. * Understanding the Device specification document. * *Calculation skills:* Acceptance of engineering basic estimation approach based on getting filling, best personal judgment and verification using simplified non-equation approach. * *Problem solving:* understanding problems, finding best solution within technology limits. * This is training for – thinking. | |
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| **Metode poučevanja in učenja:** | | |  | **Learning and teaching methods:** | |
| Predavanje z projekcijo, gradivo pripravljeno v ANG jeziku, knjiga tudi v slovenskem jeziku. Vaje na programski opremi za načrtovanje VLSI vezij ob uporabi tehnološke podpore podjetja AMS in LMFE (350nm CMOS).  Celotna predavanja temeljijo na razlagi kritičnih konceptov integracije VLSI brez komplicirane analize sistemov. | | |  | Lectures prepared in English and projected literature in English and Slovene language; lab work in Linux environment, project oriented lab work and supported with real process technology (350nm CMOS, supported by ams and LMFE). This lecture attempts to present the critical underlying concepts of VLSI without overcomplicated circuit analyses. | |
| **Načini ocenjevanja:** | Delež (v %) /  Weight (in %) | | | | **Assessment:** |
| Način (pisni izpit, ustno izpraševanje, naloge, projekt)   * Aktivno sodelovanje na predavanjih (do 20%). * Zaključen projekt/vaje ( z dokumentacijo in rezultati) (50%). * Pisni izpit (10%). * Ustni izpit (20%).   Ocene 1-5 so negativne  Ocene 6-10 so pozitivne  Pozitivna ocena lab. vaj in zaključen projekt je pogoj za pristop k pisnemu izpitu | 20%  50%  10%  20% | | | | Type (examination, oral, coursework, project):   * Collaboration in lectures, (up to 20%) * Completed lab work (included documentation and results) (50%), * Written examination (10%), * Oral examination (20%)   Grades 1-5 are negative  Grades 6-10 are positive  Positive grade of Laboratory exercises and finished project is a prerequisite for the admission to the written exam |
| **Reference nosilca / Lecturer's references:** | | | | | |
| 1. ROZMAN, Jernej. PLETERŠEK, Anton. Linear optical encoder system with sinusoidal signal distortion below -60 dB. *IEEE transactions on instrumentation and measurement*, ISSN 0018-9456, Jun. 2010, vol. 59, no. 6, str. 1544-1549. 2. PLETERŠEK, Anton, SOK, Mihael, TRONTELJ, Janez. Monitoring, control and diagnostics using RFID infrastructure. *Journal of medical systems*, ISSN 0148-5598, 2012, vol. 36, no. 6, str. 3733-3739. 3. PLETERŠEK, Anton, TRONTELJ, Janez. A self-mixing NMOS channel-detector optimized for mm-wave and THZ signals. *Journal of infrared, millimeter, and terahertz waves*, ISSN 1866-6892, 2012, vol. 33, no. 6, str. 615-626 4. TREBAR, Mira, LOTRIČ, Metka, FONDA, Irena, PLETERŠEK, Anton, KOVAČIČ, Kosta. RFID data loggers in fish supply chain traceability. *International journal of antennas and propagation (Online)*, ISSN 1687-5877, 2013, vol. 2013, str. 1-9 5. MRAOVIĆ, Matija, MUCK, Tadeja, PIVAR, Matej, TRONTELJ, Janez, PLETERŠEK, Anton. Humidity sensors printed on recycled paper and cardboard. *Sensors*, ISSN 1424-8220, Aug. 2014, vol. 14, no. 8, str. 13628-13643 | | | | | |