ALC221
(P/N: ALC221-GR)

HIGH DEFINITION AUDIO CODEC WITH MONO CLASS-D SPEAKER AMPLIFIER

DATASHEET

Version 0.65
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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC221 HD Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.10	2010/10/01	Preliminary release
0.50	2010/10/25	Update features list and block diagram.
0.60	2011/03/03	1. Update hardware features list 2. Update pin description 3. Add application circuits
0.65	2011/05/25	1. Change package information

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1. General Description

The ALC221 is a High Definition Audio Codec that integrates 4-channel DAC, 4-channel ADC, and a mono and filter-less Class-D Speaker Amplifier with 2 Watt (rms) output power.

The 4-channel DAC and 4-channel ADC support two independent stereo sound outputs and two independent stereo inputs simultaneously, supporting multiple streaming playback and output for multimedia applications and voice communication. The codec has high performance and characteristics meets WLP (Windows Logo Program) audio requirements for Windows XP, Windows Vista and Windows 7 systems.

The ALC221 supports stereo digital microphone input with boost gain and digital volume control. With Realtek second generation of software Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technology, significantly improving voice input quality for VoIP application on PCs.

ALC221 has headphone amplifier can drive 32Ω headphone load without external DC blocking capacitors, eliminating pop noise caused by these capacitors. Addition to the cap-free headphone output port (HP-OUT), port LINE-OUT is also designed as a line level output without the need for DC blocking capacitors, that can keep away from pop noise whiling line level output connected to external power speaker.

The integrated mono Class-D amplifier is a filter-free design to directly drive mini speaker with as low as 4Ω impedance. Its maximum output power exceeds 2 Watt at 5V power supply. The inside high pass filter with selectable cut off frequency can prevent speaker burn up by low frequency sound. The class D amplifier output power also could be limited to avoiding damage mini speaker. ALC221 has over current and short circuit detection to protect integrated Class D amplifier and power system. Class D amplifier output will be shut down when connected speaker is broken with short and over-heating. More than protection functions, ALC221 has spread spectrum and slew rate control for Class D carrier frequency can reduce EMI radiation when Class D amplifier is in active.

Support for 16/20/24-bit S/PDIF output with up to 192kHz sample rate offers easy connection of PCs to consumer electronic products or transporting digital audio output to a High Definition Media Interface (HDMI) transmitter.

The ALC221 supports host audio from the Intel chipsets, and also from any other HDA compatible audio controller. With various software utilities like environment sound emulation, multiple-band and independent software equalizer, dynamic range compressor and expander, optional DTS® CONNECT™ and Surround Sensation UltraPC™, SRS® TruSurround HD, SRS® Premium Sound™ and Dolby® Digital Live, Dolby® PCEE program and 3rd party voice processing (Noise Suppression/Acoustic Echo Cancellation/Beam Forming) technology, the ALC221 provides an excellent package for PC users

2. Features

2.1. Hardware Features

- Meets WLP (Windows Logo Program) requirements for Windows XP, Vista and Windows 7
- Analog DAC output with 97dB Signal-to-Noise Ratio (A-weighting)
- Analog ADC input with over 90dB Signal-to-Noise Ratio (A-weighting)
- 4-channel DAC supports 16/20/24-bit PCM format for independent two stereo channel playback
- 4-channel ADC supports 16/20/24-bit PCM format for independent two stereo channel recording
- All DACs supports 44.1k/48k/96k/192kHz sample rate
- All ADCs support 44.1k/48k/96k/192kHz sample rate
- S/PDIF-OUT support 16/20/24-bit format and 44.1/48/88.2/96/192kHz sample rate
- Six stereo analog IO ports: LINE-OUT (output), MIC1 (input and output), MIC2 (input), LINE1 (input and output), LINE2 (input and output) and HP-OUT (output)
- *One mono port with Class D Amplifier to driver mini speaker: MONO-OUT*
- One stereo digital microphone input
- Supports external PCBEEP input and built-in digital BEEP generator
- *PCBEEP pass through to port MONO-OUT (Class D amplifier), LINE-OUT-OUT an HP-OUT*
- Built in headphone amplifiers at port LINE1 and HP-OUT
- Headphone amplifier at port HP-OUT does not require DC blocking capacitors
- *Port LINE-OUT is stereo output without DC blocking capacitors*
- Software selectable 2.3V/3.0V/4.0V VREFOUT as bias voltage for analog microphone input
- Programmable +12/+24/+36dB boost gain for analog microphone input
- *Programmable boost gain and volume control for digital microphone input*
- Two jack detection pins each can detect up to 4 jacks
- *Supports 4-conductor type headset combo jack (stereo headphone output and mono microphone input on a single jack)*

- Enhanced power management features for normal operation and standby mode
- *Mono Bridge-Tied Load Class-D amplifier at port-H (MONO-OUT) has 2Watt (rms) power for 4Ω load speaker*
- Short circuit and over current protections for Class-D amplifier
- Class D amplifier has high pass filter with selectable Cut-Off frequency to prevent low frequency signal damaging speaker
- *Class D amplifier output with slew rate and spread spectrum control to reduce EMI radiation*
- Intel low power ECR HDA015-B compliant: supports power status control, jack detection, and wake-up event in D3 mode
- 2 GPIOs (General Purpose Input and Output) pins for customized applications
- EAPD (External Amplifier Power Down) is supported
- Supports Anti-pop mode when analog power AVDD is on and digital power is off
- *Built in a 5V-to-4.5V LDO to power analog circuitry*
- Power support: 3.3V digital core power; 1.5V~3.3V digital IO power for HDA link; 4.5V~5.5V analog power; 4.5V~5.5V power stage voltage
- 48-pin QFN 'Green' package

2.2. Software Features

- Meet Windows Logo Program audio requirements for Windows Vista and Windows 7
- Support Linux driver based on kernel 2.6.0 and later version
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- I3DL2 compatible
- HRTF 3D Positional Audio (Windows XP only)
- Multi-band software equalizer and dynamic range control (expander, compressor, and limiter) with adjustable parameters
- Intuitive Configuration Panel (Realtek Audio Manager) to enhance user experience
- Enhanced Microphone Acoustic Echo Cancellation (AEC), Noise Suppression (NS), and Beam Forming (BF) technology for voice application
- HDMI audio driver for Intel and AMD chipsets
- Dolby® PCEE program™ (optional software feature)
- DTS® CONNECT™, DTS® Surround Sensation UltraPC™ (optional software feature)
- SRS® TruSurround HD, SRS® Premium Sound™ (optional software feature)
- Fortemedia® SAM™ technology for voice processing (Beam Forming and Acoustic Echo Cancellation) (optional software feature)
- Creative® Host Audio program (optional software feature)

3. System Applications

- Commercial desktop and laptop PCs
- Net-book and MID (Mobile Internet Device) with High Definition Audio Controller

4. Block Diagram

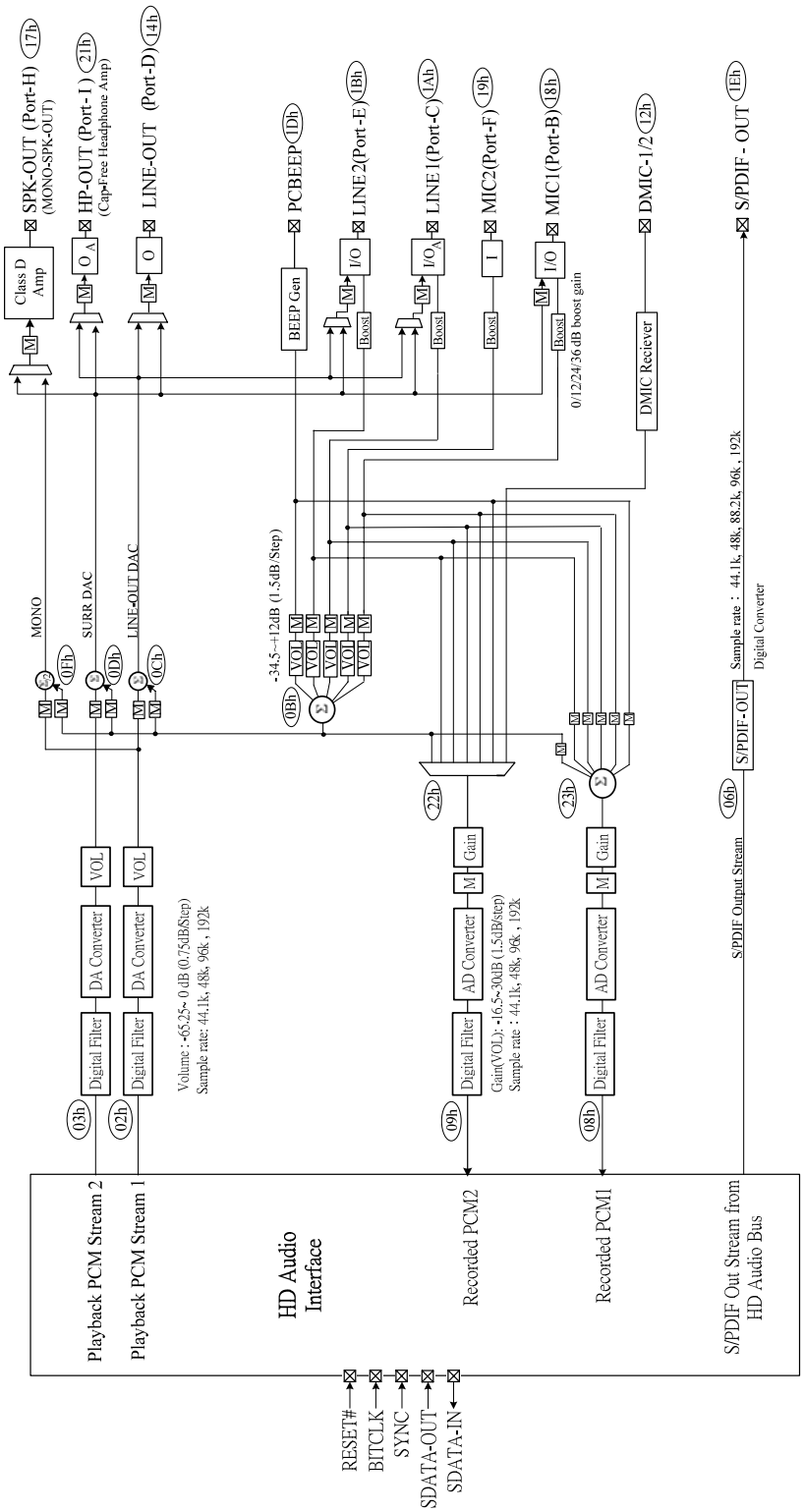


Figure 1. Block Diagram

4.1. Analog Input/Output Unit

Pin widgets NID=18h, 1Ah, and 1Bh are re-tasking IO supporting input units. NID=1Ah (Port-C, LINE1) and 21h (Port-I, HP-OUT) support amplifier units.

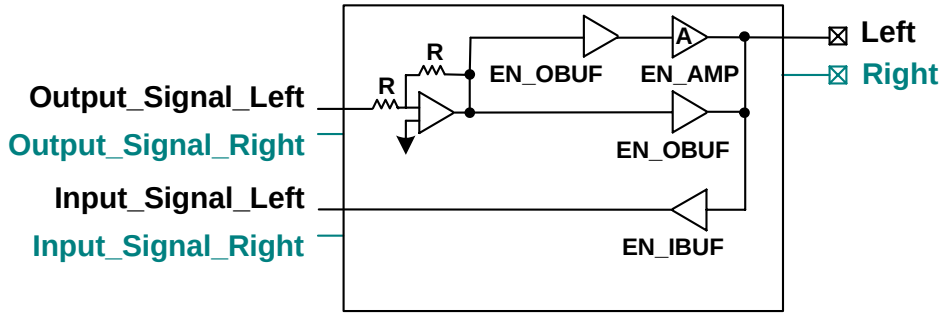


Figure 2. Analog Input/Output Unit

5. Pin Assignments

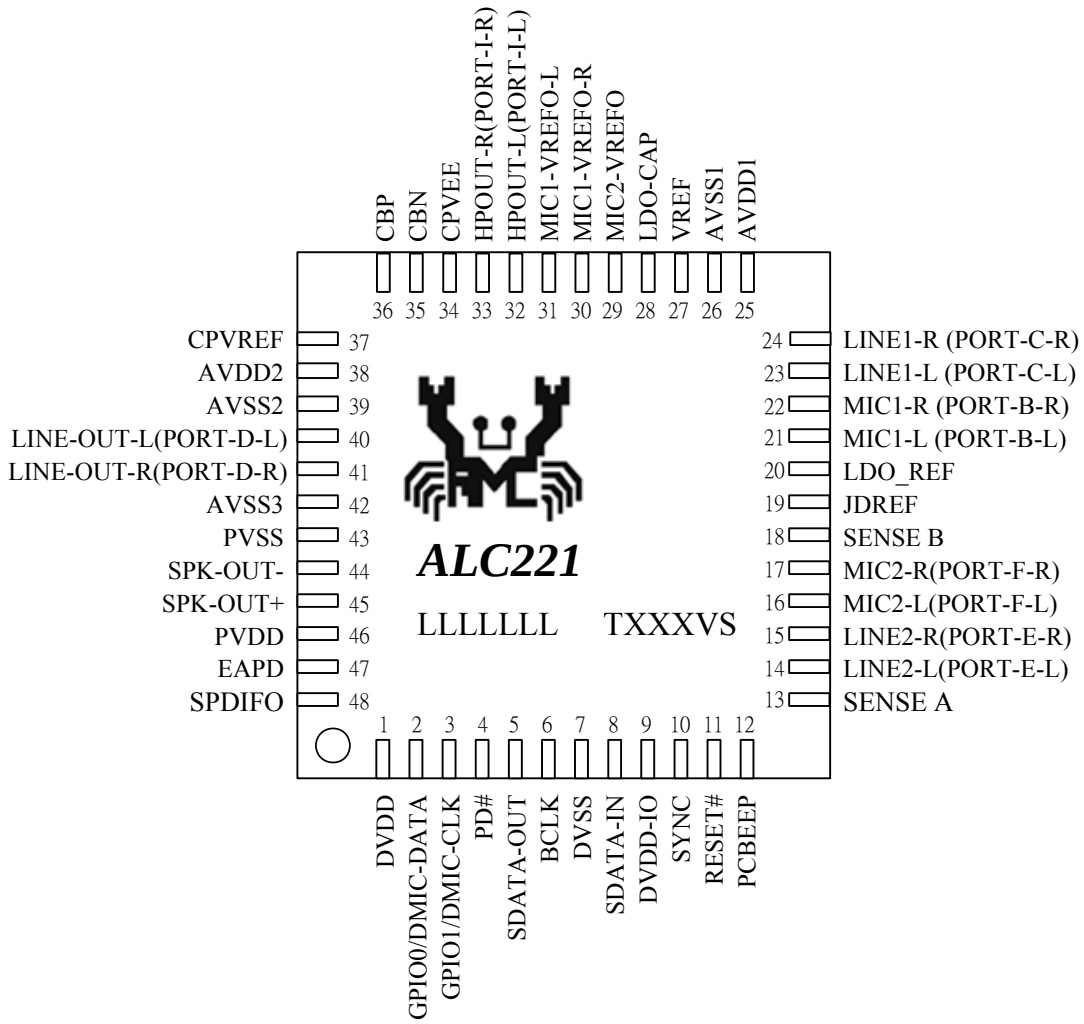


Figure 3. Pin Assignments - ALC221 (QFN-48)

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The silicon version and stepping number is shown in the location marked 'VS'.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
RESET#	I	11	H/W Reset Control	Input, V_T=0.20*(DVDD-IO)
SYNC	I	10	Sample Sync (48kHz)	Schmitt trigger input, V_{OL}=0.33*(DVDD-IO), V_{OH}=0.66*(DVDD-IO)
BCLK	I	6	24MHz Bit Clock Input	Schmitt trigger input, V_{OL}=0.33*(DVDD-IO), V_{OH}=0.66*(DVDD-IO)
SDATA-OUT	I	5	Serial TDM Data Input	Input, V_T=0.5*(DVDD-IO)
SDATA-IN	O	8	Serial TDM Data Output	Output, V_{OL}=0.1*(DVDD-IO), V_{OH}=0.9*(DVDD=IO)
EAPD	O	47	Signal to power down ext.	Output, V_{OL}=0V, V_{OH}=DVDD
SPDIFO	O	48	S/PDIF Output	Output with 12 mA@75Ω driving capability. (Internally pulled low by a 47K resistor.)
GPIO1/ DMIC-CLK	IO	3	General Purpose Input/Output 1 Clock output for digital MIC	Input/output; Shared with the digital MIC clock. Input, V_T =(2/3)*DVDD, internal pull high to DVDD by 47k ohm Output V_{OH}=DVDD, V_{OL}=DVSS, Default GPIO
GPIO0/ DMIC-DATA	IO	2	General Purpose Input/Output 0 Data input from digital MIC	Input/output; Shared with the digital MIC input data. Input, V_T =(2/3)*DVDD, internal pull high to DVDD by 47k ohm Output V_{OH}=DVDD, V_{OL}=DVSS, Default GPIO
				Total: 9 pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
PCBEEP	I	12	External PCBEEP Input	Analog input, 1.6Vrms of full-scale input
LINE2-L	IO	14	2nd Line Input Left Channel	Analog input/output, default is input (Port-E)
LINE2-R	IO	15	2nd Line Input Right Channel	Analog input/output, default is input (Port -E)
MIC2-L	I	16	2nd Stereo Microphone Input Left Channel	Analog input (Port -F)
MIC2-R	I	17	2nd Stereo Microphone Input Right Channel	Analog input (Port -F)
MIC1-L	IO	21	1st Stereo Microphone Input Left Channel	Analog input/output, default is input (Port -B)
MIC1-R	IO	22	1st Stereo Microphone Input Right Channel	Analog input/output, default is input (Port -B)
LINE1-L	IO	23	1st Line Input Left Channel	Analog input/output, default is input (Port -C)
LINE1-R	IO	24	1st Line Input Right Channel	Analog input/output, default is input (Port -C)
HP-OUT-L	O	32	Cap-Free Headphone Output Left Channel	Analog output (Port -I)
HP-OUT-R	O	33	Cap-Free Headphone Output Right Channel	Analog output (Port -I)
LINE-OUT-L	O	40	Cap-Free Line Output Left Channel	Analog output (Port -D)
LINE-OUT-R	O	41	Cap-Free Line Output Right Channel	Analog output (Port -D)
SPK-OUT -	O	44	Mono SPK Amplifier Negative Output	Pulse width modulation output (Port -H)

Name	Type	Pin	Description	Characteristic Definition
SPK-OUT +	O	45	Mono SPK Amplifier Positive Output	Pulse width modulation output (Port -H)
Sense A	I	13	Jack Detect Pin L	Resistor (5.1K, 10K, 20K, 39.2K) w/ 1% accuracy
Sense B	I	18	Jack Detect Pin 2	Resistor (5.1K, 10K, 20K, 39.2K) w/ 1% accuracy
PD#	I	4	Power Down Class D Output Control	Vil=1.25~1.45V / Vih=1.80~2.00V (internally pull-high by a 400k resistance)
				Total: 18 pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
JDREF	-	19	Ref. Resistor for Jack Detect	20K, 1% accuracy resistor to analog ground
LDO_REF	-	20	2.5V Reference Voltage	10µf capacitor to analog ground
VREF	-	27	0.5*LDO_OUT of Reference voltage	2.2µf capacitor to analog ground
LDO-CAP	-	28	LDO Output Reference for integrated regulator	10µf capacitor to analog ground
MIC2-VREFO	O	29	Bias Voltage for MIC2 Jack	2.3V/3.0V/4.0V reference voltage
MIC1-VREFO-R	O	30	Secondary Bias voltage for MIC1 jack	2.3V/3.0V/4.0V reference voltage
MIC1-VREFO-L	O	31	Bias Voltage for MIC1 Jack	2.3V/3.0V/4.0V reference voltage
CPVEE	-	34	Negative voltage output for Cap-Free	2.2µf capacitor to analog ground
CPVREF	-	37	0V Reference Voltage	Analog ground
CBN	-	35	Reference Capacitor	2.2µf capacitor to CBP
CBP	-	36	Reference Capacitor	2.2µf capacitor to CBN
				Total: 11 pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
AVDD1	P	25	Analog VDD (5.0V)	Analog power for mixer and amplifier
AVSS1	G	26	Analog GND	Analog ground for mixer and amplifier
AVDD2	P	38	Analog VDD (5.0V)	Analog power for DACs and ADCs
AVSS2	G	39	Analog GND	Analog ground for DACs and ADCs
AVSS3	G	42	Analog GND	Analog ground
DVDD	P	1	Digital core power (3.3V)	Digital core power for core logic
DVSS	G	7	Digital GND	Digital ground for core logic and HDA link
DVDD-IO	P	9	Digital IO power (1.5V~ 3.3V)	Digital I/O power for HDA link
PVDD	P	46	Power Stage VDD (5.0V)	Power supply for full-bridge Class D Amp
PVSS	G	43	Power Stage GND	Ground for full-bridge Class D Amp
Thermal Pad	G	49	Power Stage GND	Ground for full-bridge Class D Amp
				Total: 11 pins

7. High Definition Audio Link Protocol

7.1. Link Signals

The High Definition Audio (HDA) Link is the digital serial interface that connects the HDA codecs to the HDA Controller. The HDA link protocol is controller synchronous, based on a 24.0MHz BIT-CLK sent by the HDA controller. The input and output streams, including command and PCM data, are isochronous with a 48kHz frame rate. Figure 4 shows the basic concept of the HDA link protocol.

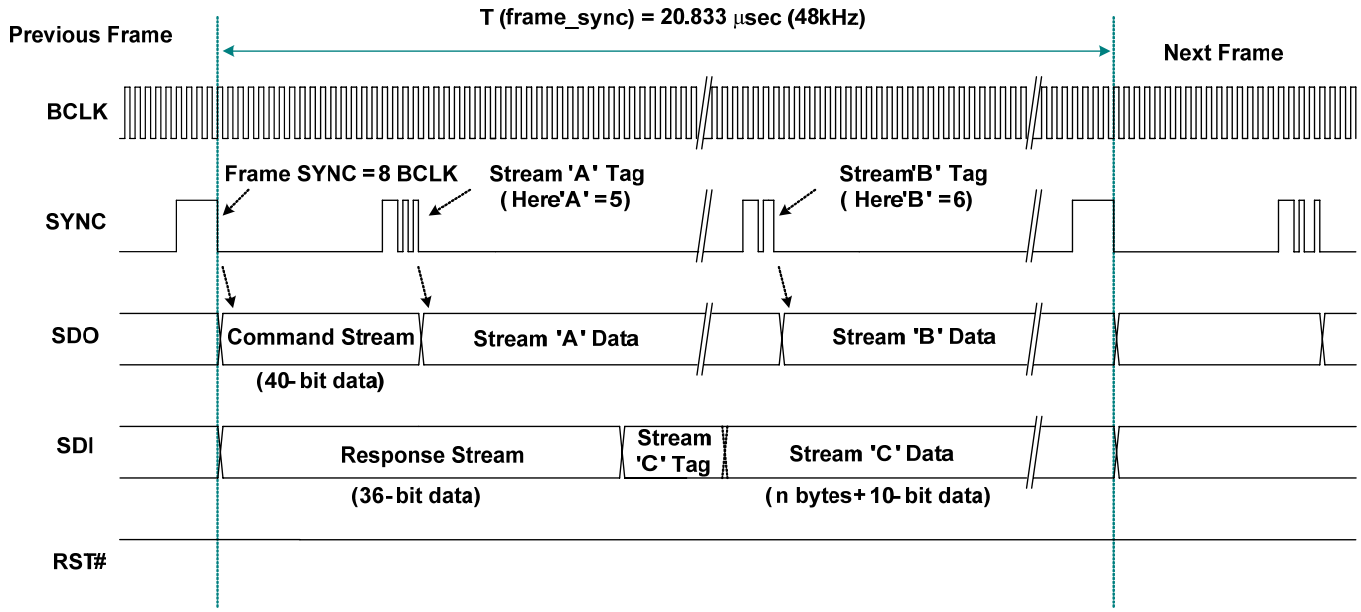


Figure 4. HDA Link Protocol

7.1.1. Signal Definitions

Table 5. Link Signal Definitions

Item	Description
BCLK	24.0MHz bit clock sourced from the HDA controller and connected to all codecs.
SYNC	48kHz signal used to synchronize input and output streams on the link. It is sourced from the HDA controller and connects to all codecs.
SDO	Serial Data Output signal driven by the HDA controller to all codecs. Commands and data streams are carried on SDO. The data rate is double pumped; the controller drives data onto the SDO, the codec samples data present on SDO with respect to each edge of BCLK. The HDA controller must support at least one SDO. To extend outbound bandwidth, multiple SDOs may be supported.
SDI	Serial Data Input signal driven by the codec. It is point-to-point serial data from the codec to the HDA controller. The controller must support at least one SDI, and up to a maximum of 15 SDI's can be supported. SDI is driven by the codec at each rising edge of BCLK, and sampled by the controller at each rising edge of BCLK. SDI can be driven by the controller to initialize the codec's ID.
RST#	Active low reset signal. Asserted to reset the codec to default power on state. RST# is sourced from the HDA controller and connects to all codecs.

Table 6. HDA Signal Definitions

Signal Name	Source	Controller Type	Description
BCLK	Controller	Output	Global 24.0MHz Bit Clock.
SYNC	Controller	Output	Global 48kHz Frame Sync and outbound tag signal.
SDO	Controller	Output	Serial Data Output from Controller.
SDI	Codec/Controller	Input/Output	Serial Data Input from codec. Weakly pulled down by the controller.
RST#	Controller	Output	Global Active Low Reset Signal.

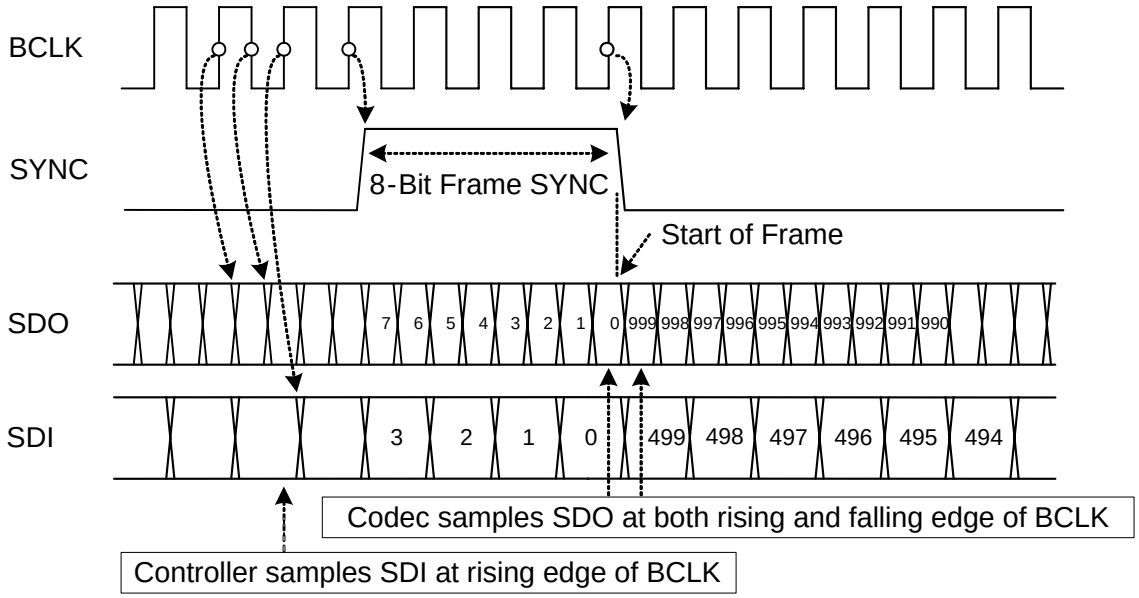


Figure 5. Bit Timing

7.1.2. Signaling Topology

The HDA controller supports two SDOs for the outbound stream, up to 15 SDIs for the inbound stream. RST#, BCLK, SYNC, SDO0 and SDO1 are driven by controller to codecs. Each codec drives its own point-to-point SDI signal(s) to the controller.

Figure 6 shows the possible connections between the HDA controller and codecs:

- Codec 0 is a basic connection. There is one single SDO and one single SDI for normal transmission
- Codec 1 has two SDOs for doubled outbound rate, a single SDI for normal inbound rate
- Codec 3 supports a single SDO for normal outbound rate, and two SDIs for doubled inbound rate
- Codec N has two SDOs and multiple SDIs

The multiple SDOs and multiple SDIs are used to expand the transmission rate between controller and codecs. Section 7.2 Frame Composition, page 13 describes the detailed outbound and inbound stream compositions for single and multiple SDOs/SDIs.

The connections shown in Figure 6 can be implemented concurrently in an HDA system. The ALC221 is designed to receive a single SDO stream.

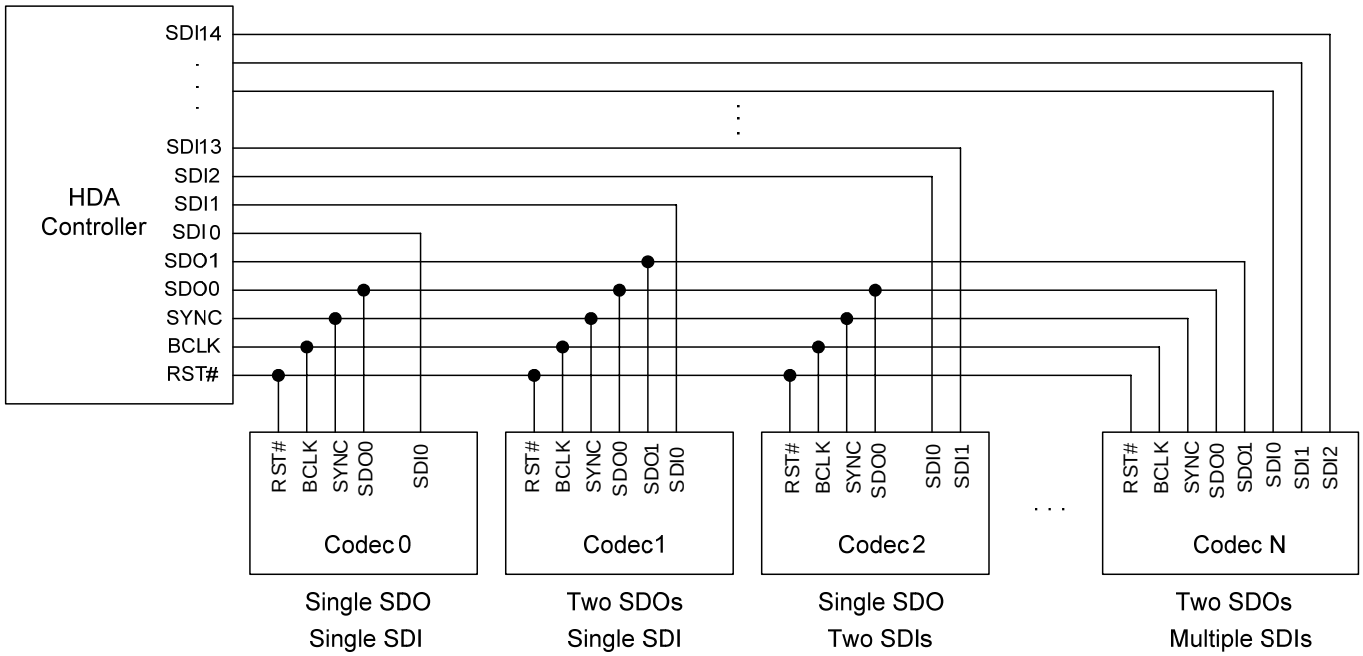


Figure 6. Signaling Topology

7.2. Frame Composition

7.2.1. Outbound Frame – Single SDO

An outbound frame is composed of one 32-Bit command stream and multiple data streams. There are one or multiple sample blocks in a data stream. Only one sample block exists in a stream if the HDA controller delivers a 48kHz rate of samples to the codec. Multiple sample blocks in a stream means the sample rate is a multiple of 48kHz. This means there should be 2 blocks in the same stream to carry 96kHz samples (Figure 7).

For outbound frames, the stream tag is not in SDO, but in the SYNC signal. A new data stream is started at the end of the stream tag. The stream tag includes a 4-Bit preamble and 4-Bit stream ID (Figure 8).

To keep the cadence of converters bound to the same stream, samples for these converters must be placed in the same block.

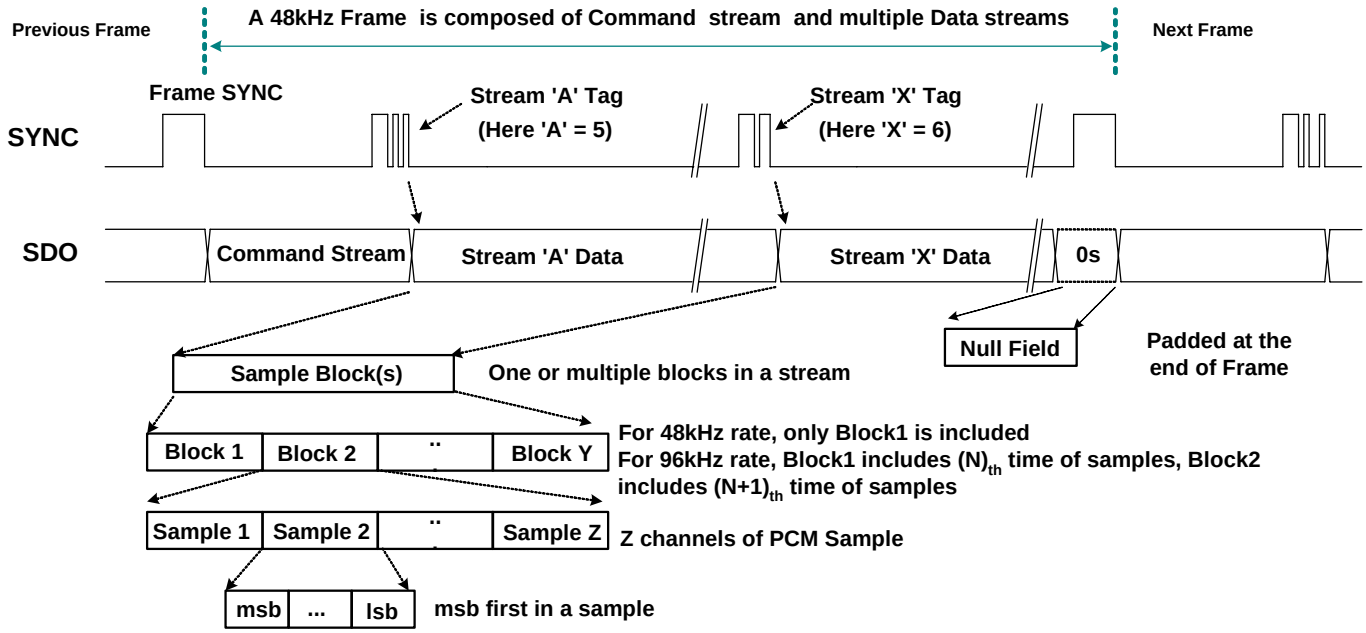


Figure 7. SDO Outbound Frame

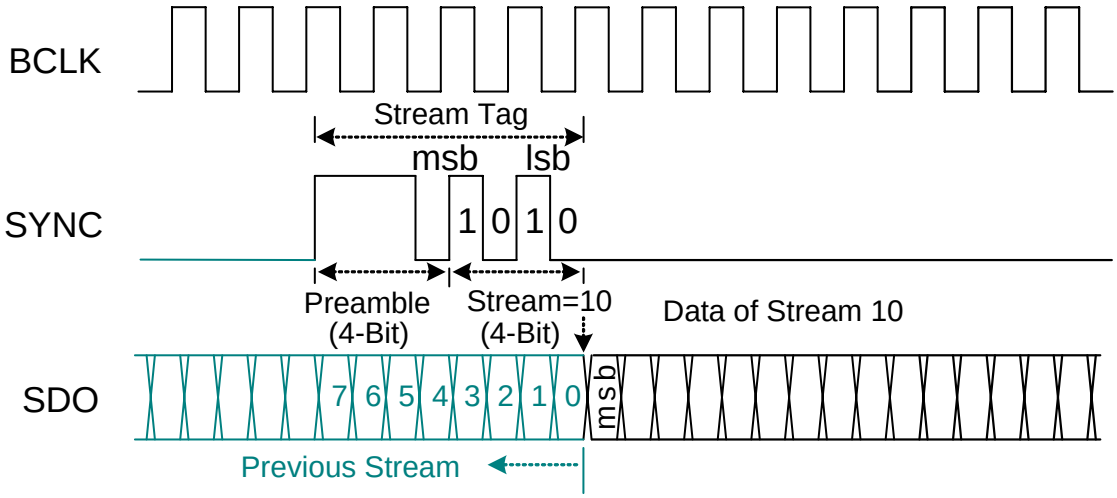


Figure 8. SDO Stream Tag is Indicated in SYNC

7.2.2. Inbound Frame – Single SDI

An Inbound Frame – Single SDI is composed of one 36-Bit response stream and multiple data streams. Except for the initialization sequence (turnaround and address frame), SDI is driven by the codec at each rising edge of BCLK. The controller also samples data at the rising edge of BCLK (Figure 9).

The SDI stream tag is not carried by SYNC, but included in the SDI. A complete SDI data stream includes one 4-Bit stream tag, one 6-Bit data length, and n-Bit sample blocks. Zeros will be padded if the total length of the contiguous sample blocks within a given stream is not of integral byte length (Figure 10).

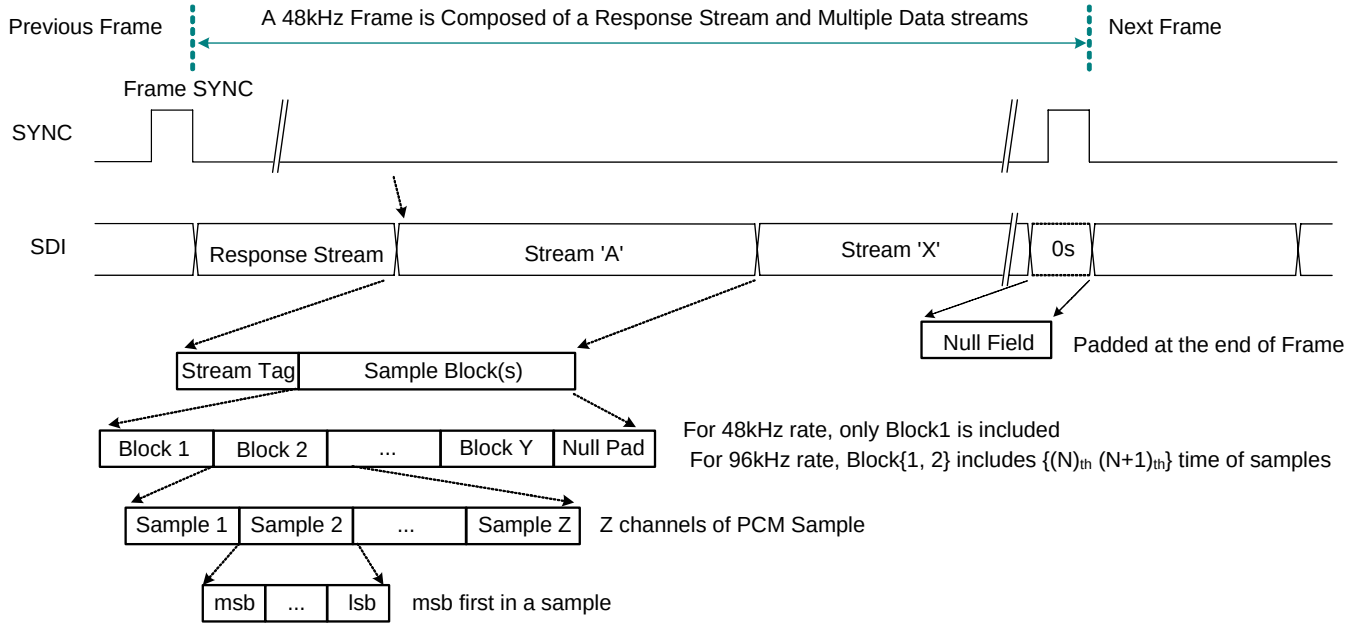


Figure 9. SDI Inbound Stream

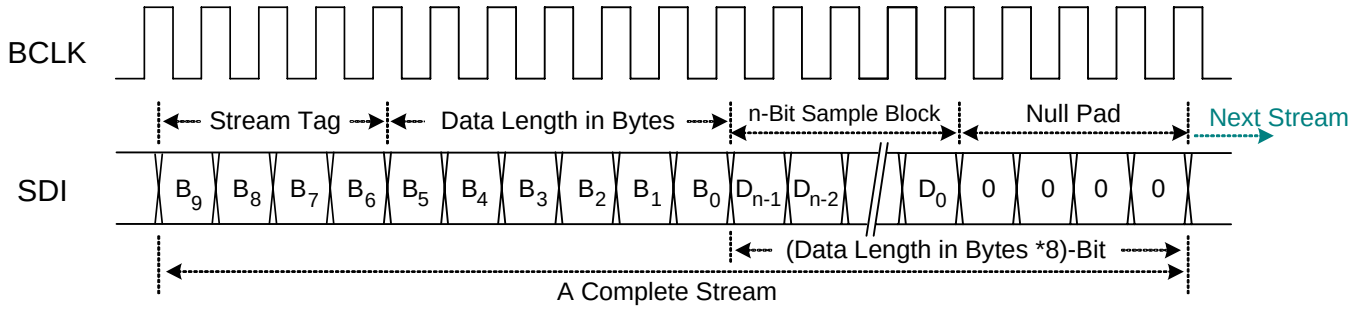


Figure 10. SDI Stream Tag and Data

7.2.3. Variable Sample Rates

The HDA link is designed for sample rates of 48kHz. Variable rates of sample are delivered in multiple or sub-multiple rates of 48kHz. Two sample blocks per frame result in a 96kHz delivery rate, one sample block over two frames results in a 24kHz delivery rate. The HDA specification states that the sample rate of the outbound stream be synchronized by the controller, not by the codec. Each stream has its own sample rate, independent of any other stream.

The HDA controller supports 48kHz and 44.1kHz base rates. Table 7, page 16, shows the recommended sample rates based on multiples or sub-multiples of one of the two base rates.

Rates in sub-multiples (1/n) of 48kHz are interleaving n frames containing no sample blocks. Rates in multiples (n) of 48kHz contain n sample blocks in a frame. Table 8, page 16, shows the delivery cadence of variable rates based on 48kHz.

The HDA link is defined to operate at a fixed 48kHz frame rate. To deliver samples in (sub) multiple rates of 44.1kHz, an appropriate ratio between 44.1kHz and 48kHz must be maintained to avoid frequency drift. The appropriate ratio between 44.1kHz and 48kHz is 147/160. Meaning 147 sample blocks are transmitted every 160 frames.

The cadence '12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)'interleaves 13 frames containing no sample blocks in every 160 frames. It provides a low long-term frequency drift for 44.1kHz of delivery rate. Rates in sub-multiples (1/n) of 44.1kHz also follow this cadence AND interleave n empty frames. Rates in multiples (n) of 44.1kHz applying this cadence contain n sample blocks in the non-empty frame AND interleave an empty frame between non-empty frames (Table 9, page 17).

Table 7. Defined Sample Rate and Transmission Rate

(Sub) Multiple	48kHz Base	44.1kHz Base
1/6	8kHz (1 sample block every 6 frames)	-
1/4	12kHz (1 sample block every 4 frames)	11.025kHz (1 sample block every 4 frames)
1/3	16kHz (1 sample block every 3 frames)	-
1/2	-	22.05kHz (1 sample block every 2 frames)
2/3	32kHz (2 sample blocks every 3 frames)	-
1	48kHz (1 sample block per frame)	44.1kHz (1 sample block per frame)
2	96kHz (2 sample blocks per frame)	88.2kHz (2 sample blocks per frame)
4	192kHz (4 sample blocks per frame)	176.4kHz (4 sample blocks per frame)

Table 8. 48kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence	Description
8kHz	YNNNNN (repeat)	One sample block is transmitted in every 6 frames
12kHz	YNNN (repeat)	One sample block is transmitted in every 4 frames
16kHz	YNN (repeat)	One sample block is transmitted in every 3 frames
32kHz	Y^2NN (repeat)	One sample block is transmitted in every 6 frames
48kHz	Y (repeat)	One sample block is transmitted in every 6 frames
96kHz	Y^2 (repeat)	Two sample blocks are transmitted in each frame
192kHz	Y^4 (repeat)	Four sample blocks are transmitted in each frame

N: No sample block in a frame. Y: One sample block in a frame. Yx: X sample blocks in a frame.

Table 9. 44.1kHz Variable Rate of Delivery Timing

Rate	Delivery Cadence
11.025kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
22.05kHz	{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{12}{-}{11}{-}{11}{-}{11}{-} (repeat)
44.1kHz	12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)
88.2kHz	12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-12^2-11^2-11^2-11^2- (repeat)
176.4kHz	12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-12^4-11^4-11^4-11^4- (repeat)

11.025kHz: {12}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN
{11}=YNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNNYNNN
{ - }=NNNN

22.050kHz: {12}=YNYNYNYNYNYNYNYNYNYNYNYN
{11}=YNYNYNYNYNYNYNYNYNYNYNYN
{ - }=NN

44.1kHz: 12- =Contiguous 12 frames containing 1 sample blocks each, followed by one frame with no sample block.

88.2kHz: 12^2- =Contiguous 12 frames containing 2 sample blocks each, followed by one frame with no sample block.

176.4kHz: 12^4- =Contiguous 12 frames containing 4 sample blocks each, followed by one frame with no sample block.

7.3. Reset and Initialization

There are two types of reset within an HDA link:

- Link Reset. Generated by assertion of the RST# signal, all codecs return to their power on state
- Codec Reset. Generated by software directing a command to reset a specific codec back to its default state

An initialization sequence is requested after any of the following three events:

1. Link Reset

2. Codec Reset

3. Codec changes its power state (For example, hot docking a codec to an HDA system)

7.3.1. Link Reset

A link reset may be caused by 3 events:

1. The HDA controller asserts RST# for any reason (power up, or PCI reset)

2. Software initiates a link reset via the 'CRST' bit in the Global Control Register (GCR) of the HDA controller

3. Software initiates power management sequences. Figure 11, page 19, shows the 'Link Reset' timing including the 'Enter' sequence (❶~❺) and 'Exit' sequence (❻~❾)

Enter 'Link Reset':

❶ Software writes a 0 to the 'CRST' bit in the Global Control Register of the HDA controller to initiate a link reset

❷ As the controller completes the current frame, it does not signal the normal 8-Bit frame SYNC at the end of the frame

❸ The controller drives SYNC and all SDOs to low. Codecs also drive SDIs to low

❹ The controller asserts the RST# signal to low, and enters the 'Link Reset' state

❺ All link signals driven by controller and codecs should be tri-state by internal pull low resistors

Exit from 'Link Reset':

❻ If BCLK is re-started for any reason (codec wake-up event, power management, etc.)

❼ Software is responsible for de-asserting RST# after a minimum of 100µsec BCLK running time (the 100µsec provides time for the codec PLL to stabilize)

❽ Minimum of 4 BCLK after RST# is de-asserted, the controller starts to signal normal frame SYNC

❾ When the codec drives its SDI to request an initialization sequence (when the SDI is driven high at the last bit of frame SYNC, it means the codec requests an initialization sequence)

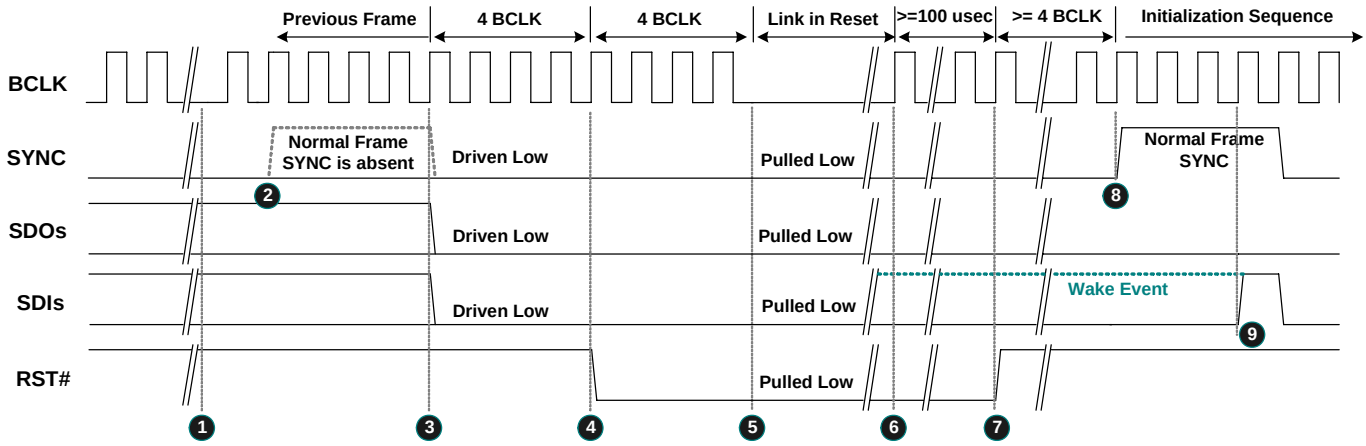


Figure 11. Link Reset Timing

7.3.2. Codec Reset

A 'Codec Reset' is initiated via the Codec RESET command verb. It results in the target codec being reset to the default state. After the target codec completes its reset operation, an initialization sequence is requested.

7.3.3. Codec Initialization Sequence

❶ The codec drives SDI high at the last bit of SYNC to request a Codec Address (CAD) from the controller

❷ The codec will stop driving the SDI during this turnaround period

❸❹❺❻ The controller drives SDI to assign a CAD to the codec

❼ The controller releases the SDI after the CAD has been assigned

❽ Normal operation state

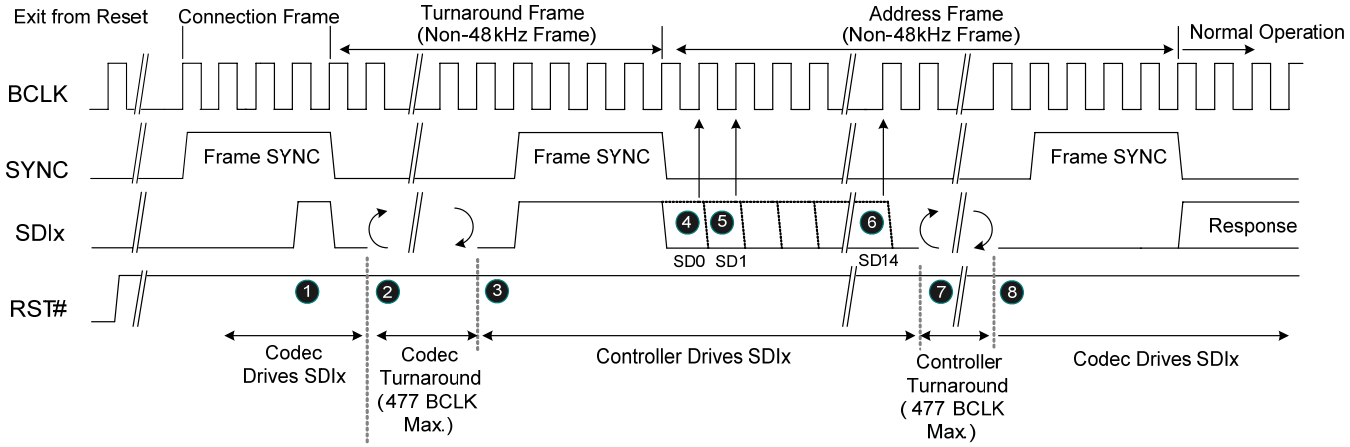


Figure 12. Codec Initialization Sequence

7.4. Verb and Response Format

7.4.1. Command Verb Format

There are two types of verbs: one with 4-Bit identifiers (4-Bit verbs) and 16-Bits of data, the other with 12-Bit identifiers (12-Bit verbs) and 8-Bits of data. Table 10 shows the 4-Bit verb structure of a command stream sent from the controller to operate the codec. Table 11 is the 12-Bit verb structure that gets and controls parameters in the codec.

Table 10. 40-Bit Commands in 4-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:16]	Bit [15:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

Table 11. 40-Bit Commands in 12-Bit Verb Format

Bit [39:32]	Bit [31:28]	Bit [27:20]	Bit [19:8]	Bit [7:0]
Reserved	Codec Address	Node ID	Verb ID	Payload

7.4.2. Response Format

There are two types of response from the codec to the controller. Solicited Responses are returned by the codec in response to a current command verb. The codec will send Solicited Response data in the next frame, without regard to the Set (Write) or Get (Read) command. The 32-Bit Response is interpreted by software, opaque to the controller.

Unsolicited Responses are sent by the codec independently of software requests. Jack Detection or GPI status information can be actively delivered to the controller and interpreted by software. The 'Tag' in Bit[31:28] is used to identify unsolicited events. This tag is undefined in the HDA specifications.

Table 12. Solicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:0]
Valid	Unsol=0	Reserved	Response

Table 13. Unsolicited Response Format

Bit [35]	Bit [34]	Bit [33:32]	Bit [31:28]	Bit [27:0]
Valid	Unsol=1	Reserved	Tag	Response

Note: The response stream in the link protocol is 36-Bits wide. The response is placed in the lower 32-bit field. Bit-35 is a 'Valid' bit to indicate the response is 'Ready'. Bit-34 is set to indicate that an unsolicited response was sent.

7.4.3. Double Function Reset

This reset is executed by sending two Function Group resets back to back. This Function Group "Double" reset shall do a full initialization and reset all settings to their power on defaults. This Double Reset is defined as two Function Group Reset verbs received without any other intervening valid verbs. The reset verbs are not necessary to be received in sequential frames, but there must not be any other verbs received in frames between the conceptive of the Function Group Reset verbs. It is allowed that there are several null commands received in frames between Function Group Reset verbs.

7.5. Power Management

ALC221 meet the INTEL's Audio CODEC low power state white paper and it's ECR HDA-015B compliant. And ALC221 has the follow 5 attributes (INTEL's white paper).

D3 state power < 30mW(without PC-Beep pass-through Function)

1. With PC-Beep pass-through Function, the criteria is 60mW.

2. Exit latency (D3 to D0 transfer) < 10ms.

3. Audio pop/click suppression during D3 and D0 transision < -65dBV.

4. Support Jack detection in D3 state.

5. D3 function work with or without the BITCLK.

ALC221 minimizes the idle power for D3 state that allow system to entry D3 mode when CODEC is idle. And it will save power consumption for idle mode and increase overall battery life for mobile system.

In D3 mode, only power on reset or "double function reset" could reset all settings of ALC221. SW would not spend a lot of time for configure the CODEC to the previous setting when CODEC entry to the D3. System would reduce the latency time for CODEC's D3 to D0 transition.

ALC221 supports Wake-Up event in low power mode, D3. ALC221 would generate the wake-up event caused by the changing of jack detection or GPIO status in D3, If HDA-Link was alive (with BCLK), CODEC would response as a normal operation. And if the BITCLK disappeared, CODEC would drive the SDI as high to wake up the system.

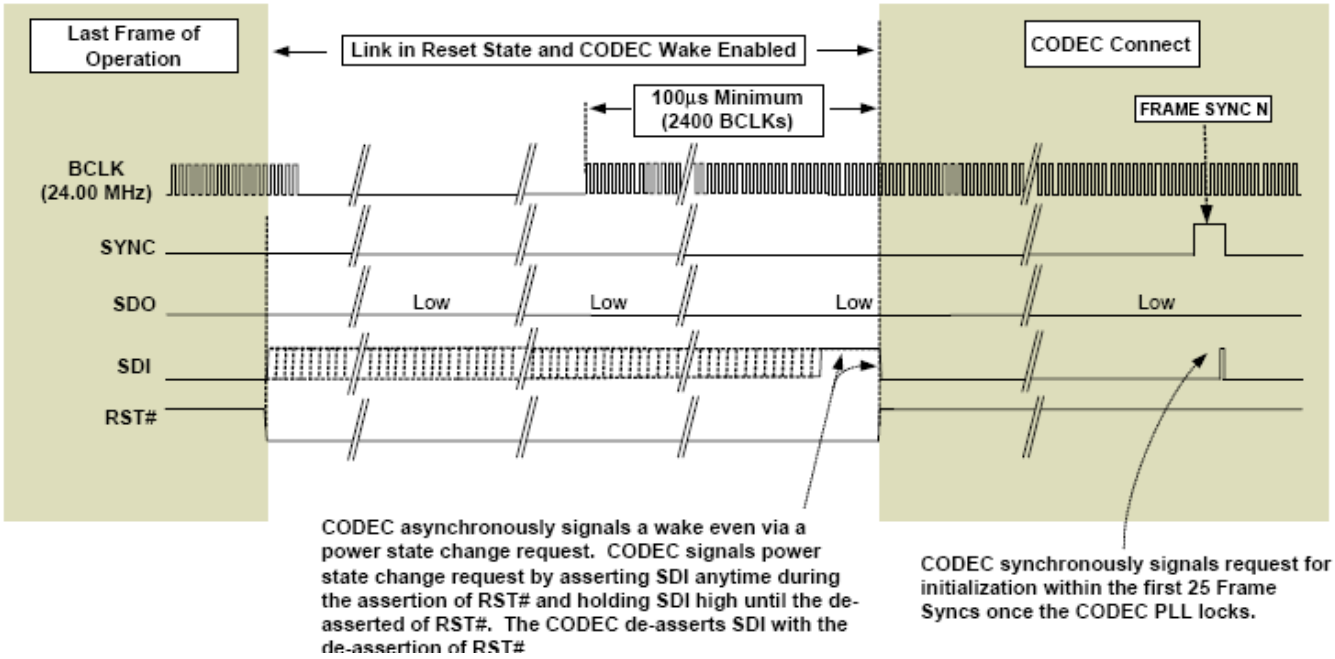


Figure 14. Resume from the external event (Wake-up event)

All power management state changes in widgets are driven by software. Table 17 indicates the definitions of power states.

In ALC221, the Audio Function (NID=01h), input converter, output converter, and every pin widget support power control. Software may have various power states dependent on system configuration. Table 18 indicates those Nodes supporting power management. To simplify power control, software can configure whole codec power states through the Audio Function (NID=01h) only. Output converters (DACs) and input converters (ADCs) also have no individual power control to supply fine-Grained power control.

Table 14. System Power State Definitions

Power States	Definitions
D0	All power on. Individual DACs and ADCs can be powered up or down as required.
D1	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, analog reference stays up.
D2	All amplifiers and converters (DACs and ADCs) are powered down. State maintained, but analog reference off (D1 + analog reference off).
D3	Power still supplied. The codec stops the internal clock. State is maintained.
D3 (No BitCLK)	Powers are still supplied, BITCLK stop and Reset in low state.

Table 15. Power Controls in NID=01h

	Description	D0	D1	D2	D3 (Hot/Cold)	Link Reset
Audio Function (NID=01h)	LINK Response	Normal	Normal	Normal	PD	PD
	DACs	Normal	PD	PD	PD	PD
	ADCs	Normal	PD	PD	PD	PD
	All Headphone Drivers	Normal	Normal	PD	PD	Normal
	All Mixers	Normal	Normal	PD	PD	Normal
	All Reference	Normal	Normal	PD	PD	Normal

Note: PD=Powered Down

Table 16. Powered Down Conditions

Condition	Description
LINK Response powered down	Internal clock is stopped. SDATA-IN and S/PDIF-OUT are floated with pulled low 47K resistors internally. Detection of 'Link Reset Entry' and 'Link Reset Exit' sequences are supported. All states are maintained if DVDD is supplied.
DAC powered down	Analog block and digital filter are powered down.
ADC powered down	Analog block and digital filter are powered down. The data on SDATA-IN is quiet.
Headphone Driver powered down	All headphone drivers are powered down.
Mixers powered down	All internal mixer widgets are powered down. The DC reference and VREFOUTx at individual pin complexes are still alive.
Reference power down	All internal references, DC reference, and VREFOUTx at individual pin complexes are off.

8. Supported Verbs and Parameters

This section describes the Verbs and Parameters supported by various widgets in the ALC221. If a verb is not supported by the addressed widget, it will respond with 32 bits of '0'.

8.1. Verb – Get Parameters (Verb ID=F00h)

The 'Get Parameters' verb is used to get system information and the function capabilities of the HDA codec. All the parameters are read-only. Refer to section 7.4.1 Command Verb Format, page 21, to get detailed information about supported parameters.

Table 17. Verb – Get Parameters (Verb ID=F00h)

Get Parameter Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=00h	Verb ID=F00h	Parameter ID[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Note: If the parameter ID is not supported, the returned response is 32 bits of '0'.

8.1.1. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Table 18. Parameter – Vendor ID (Verb ID=F00h, Parameter ID=00h)

Codec Response Format

Bit	Description
31:16	Vendor ID=10ECh (Realtek's PCI vendor ID).
15:0	Device ID=0221h.

Note: The Root Node (NID=00h) supports this parameter.

8.1.2. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Table 19. Parameter – Revision ID (Verb ID=F00h, Parameter ID=02h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	MajRev. The major version number (in decimal) of the HDA Spec to which the ALC221 is fully compliant.
19:16	MinRev. The minor version number (in decimal) of the HDA Spec to which the ALC221 is fully compliant.
15:8	Revision ID. The vendor's revision number. 00h is for the first silicon version A, 01h is for the second version B, etc.
7:0	Stepping ID. The vendor's stepping number within the given Revision ID.

Note: The Root Node (NID=00h in the ALC221) supports this parameter.

For example, Revision ID=00h and Stepping ID=00h indicates the silicon is the A0 version.

8.1.3. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

For the root node, the Subordinate Node Count provides information about audio function group nodes associated with the root node. For function group nodes, it provides the total number of widgets associated with this function node.

Table 20. Parameter – Subordinate Node Count (Verb ID=F00h, Parameter ID=04h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:16	Starting Node Number. The starting node number in the sequential widgets.
15:8	Reserved. Read as 0's.
7:0	Total Number of Nodes. For a root node, the total number of function groups in the root node. For a function group, the total number of widget nodes in the function group.

8.1.4. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Table 21. Parameter – Function Group Type (Verb ID=F00h, Parameter ID=05h)

Codec Response Format

Bit	Description
31:9	Reserved. Read as 0's.
8	UnSol Capable. 0: Unsolicited response is not supported by this function group 1: Unsolicited response is supported by this function group
7:0	Function Group Type. 00h: Reserved 01h: Audio Function 02h: Modem Function 03h~7Fh: Reserved 80h~FFh: Vendor Defined Function.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.5. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Table 22. Parameter – Audio Function Capabilities (Verb ID=F00h, Parameter ID=08h)

Codec Response Format

Bit	Description
31:17	Reserved. Read as 0's.
16	Beep Generator. A '1' indicates the presence of an integrated Beep generator within the Audio Function Group.
15:12	Reserved. Read as 0's.
11:8	Input Delay.
7:4	Reserved. Read as 0's.

3:0	Output Delay.

Note: The Audio Function Group (NID=01h) supports this parameter.

8.1.6. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Table 23. Parameter – Audio Widget Capabilities (Verb ID=F00h, Parameter ID=09h)

Codec Response Format

Bit	Description
31:24	Reserved. Read as 0's.
23:20	Widget Type. 0h: Audio Output 1h: Audio Input 2h: Mixer 3h: Selector 4h: Pin Complex 5h: Power Widget 6h: Volume Knob Widget 7h~Eh: Reserved Fh: Vendor defined audio widget
19:16	Delay. Samples delayed between the HDA link and widgets.
15:11	Reserved. Read as 0's.
10	Power Control. 0: Power state control is not supported on this widget 1: Power state is supported on this widget
9	Digital. 0: An analog input or output converter 1: A widget translating digital data between the HDA link and digital I/O (S/PDIF, I2S, etc.)
8	ConnList. Connection List. 0: Connected to HDA link. No Connection List Entry should be queried 1: Connection List Entry must be queried
7	UnsolCap. Unsolicited Capable. 0: Unsolicited response is not supported 1: Unsolicited response is supported
6	ProcWidget. Processing Widget. 0: No processing control 1: Processing control is supported
5	Reserved. Read as 0.
4	Format Override.
3	AmpParOvr. AMP Param Override.
2	OutAmpPre. Out AMP Present.
1	InAmpPre. In AMP Present.
0	Stereo. 0: Mono Widget 1: Stereo Widget

8.1.7. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Parameter in audio function provides default information about formats. Individual converters have their own parameters to provide supported formats if their 'Format Override' bit is set.

Table 24. Parameter – Supported PCM Size, Rates (Verb ID=F00h, Parameter ID=0Ah)

Codec Response Format

Bit	Description
31:21	Reserved. Read as 0's.
20	B32. Indicates whether 32-Bit audio format is supported. 0: Not supported 1: Supported
19	B24. Indicates whether 24-Bit audio format is supported. 0: Not supported 1: Supported
18	B20. Indicates whether 20-Bit audio format is supported. 0: Not supported 1: Supported
17	B16. Indicates whether 16-Bit audio format is supported. 0: Not supported 1: Supported
16	B8. Indicates whether 8-Bit audio format is supported. 0: Not supported 1: Supported
15:12	Reserved. Read as 0's.
11	R12. Indicates whether 384kHz (=8*48kHz) rate is supported. 0: Not supported 1: Supported
10	R11. Indicates whether 192kHz (=4*48kHz) rate is supported. 0: Not supported 1: Supported
9	R10. Indicates whether 176.4kHz (=4*44.1kHz) rate is supported. 0: Not supported 1: Supported
8	R9. Indicates whether 96kHz (=2*48kHz) rate is supported. 0: Not supported 1: Supported
7	R8. Indicates whether 88.2kHz (=2*44.1kHz) rate is supported. 0: Not supported 1: Supported
6	R7. Indicates whether 48kHz rate is supported. 0: Not supported 1: Supported
5	R6. Indicates whether 44.1kHz rate is supported. 0: Not supported 1: Supported
4	R5. Indicates whether 32kHz (=2/3*48kHz) rate is supported. 0: Not supported 1: Supported
3	R4. Indicates whether 22.05kHz (=1/2*44.1kHz) rate is supported. 0: Not supported 1: Supported
2	R3. Indicates whether 16kHz (=1/3*48kHz) rate is supported. 0: Not supported 1: Supported
1	R2. Indicates whether 11.025kHz (=1/4*44.1kHz) rate is supported. 0: Not supported 1: Supported
0	R1. Indicates whether 8kHz (=1/6*48kHz) rate is supported. 0: Not supported 1: Supported

8.1.8. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Parameters in this node only provide default information for audio function groups. Individual converters have their own parameters to provide supported formats if the 'Format Override' bit is set.

Table 25. Parameter – Supported Stream Formats (Verb ID=F00h, Parameter ID=0Bh)

Codec Response Format

Bit	Description
31:3	Reserved. Read as 0's.
2	AC3. 0: Not supported 1: Supported
1	Float32. 0: Not supported 1: Supported
0	PCM. 0: Not supported 1: Supported

Note: Input converters and output converters support this parameter.

8.1.9. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex widget.

Table 26. Parameter – Pin Capabilities (Verb ID=F00h, Parameter ID=0Ch)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	VREF Control Capability. '1' in corresponding bit field indicates signal levels of associated Vrefout are specified as a percentage of AVDD.

7:6	5	4	3	2	1	0
Reserved	100%	80%	Reserved	Ground	50%	Hi-Z

Bit	Description
7	L-R Swap. Indicates the capability of swapping the left and rights.
6	Balanced I/O Pin. '1' indicates this pin complex has balanced pins.
5	Input Capable. '1' indicates this pin complex supports input.
4	Output Capable. '1' indicates this pin complex supports output.
3	Headphone Drive Capable. '1' indicates this pin complex has an amplifier to drive a headphone.
2	Presence Detect Capable. '1' indicates this pin complex can detect whether there is anything plugged in.
1	Trigger Required. '1' indicates whether a software trigger is required for an impedance measurement.
0	Impedance Sense Capable. '1' indicates this pin complex can perform analog sense on the attached device to determine its type.

Note: Only Pin Complex widgets support this parameter.

8.1.10. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 27. Parameter – Amplifier Capabilities (Verb ID=F00h, Input Amplifier Parameter ID=0Dh)

Codec Response Format

Bit	Description
31	(Input) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.11. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Parameters in this node provide audio function group default information. Individual converters have their own parameters to provide amplifier capabilities if the 'AMP Param Override' bit is set.

Table 28. Parameter – Amplifier Capabilities (Verb ID=F00h, Output Amplifier Parameter ID=12h)

Codec Response Format

Bit	Description
31	(Output) Mute Capable.
30:23	Reserved. Read as 0.
22:16	Step Size. Indicates the size of each step in the gain range. Each step may be 0~32dB, specified in 0.25dB steps. '0' indicates a step of 0.25dB. '127' indicates a step of 32dB.
15	Reserved. Read as 0.
14:8	Number of Steps. Indicates the number of steps in the gain range. '0' means the gain is fixed.
7	Reserved. Read as 0.
6:0	Offset. Indicates which step is 0dB.

8.1.12. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Parameters in this node provide audio function widget connection information.

Table 29. Parameter – Connect List Length (Verb ID=F00h, Parameter ID=0Eh)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0.
7	Short Form. 0: Short Form 1: Long Form
6:0	Connect List Length. Indicates the number of inputs connected to a widget. If the Connect List Length is 1, there is only one input, and there is no Connection Select Control (Not a MUX widget).

8.1.13. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Table 30. Parameter – Supported Power States (Verb ID=F00h, Parameter ID=0Fh)

Codec Response Format

Bit	Description
31:4	Reserved. Read as 0's.
3	D3Sup. 1: Power state D3 is supported.
2	D2Sup. 1: Power state D2 is supported.
1	D1Sup. 1: Power state D1 is supported.
0	D0Sup 1: Power state D0 is supported.

8.1.14. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Table 31. Parameter – Processing Capabilities (Verb ID=F00h, Parameter ID=10h)

Codec Response Format

Bit	Description
31:16	Reserved. Read as 0's.
15:8	NumCoeff. Number of Coefficient.
7:1	Reserved. Read as 0's.

0	Benign. 0: Processing unit is not linear and time invariant 1: Processing unit is linear and time invariant

8.1.15. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Table 32. Parameter – GPIO Capabilities (Verb ID=F00h, Parameter ID=11h)

Codec Response Format

Bit	Description
31	GPIWake=0. The ALC221 does not support GPIO wake up function.
30	GPIUnsol=1. The ALC221 supports GPIO unsolicited response.
29:24	Reserved. Read as 0's.
23:16	NumGPIs=00h. No GPI pin is supported.
15:8	NumGPOs=00h. No GPO pin is supported.
7:0	NumGPIOs=02h. Two GPIO pins are supported.

8.1.16. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Table 33. Parameter – Volume Knob Capabilities (Verb ID=F00h, Parameter ID=13h)

Codec Response Format

Bit	Description
31:8	Reserved. Read as 0's.
7	Delta. 0: Software cannot modify the Volume Control Knob volume 1: Software can write a base volume to the Volume Control Knob
6:0	NumSteps. The number of steps in the range of the Volume Control Knob.

Note: The ALC221 does not support volume control knob.

8.2. Verb – Get Connection Select Control (Verb ID=F01h)

Table 34. Verb – Get Connection Select Control (Verb ID=F01h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F01h	0's

Codec Response Format

Response [31:0]
Bit[7:0] are Connection Index

Codec Response for Multiplexer Widget NID=14h (Port-D), 1Ah (Port-C), 1Bh (Port-E), 21h (Port-I)

Bit	Description
31:8	0's.
7:0	Connection Index currently Set (Default value is 00h). 00h: Pin Widget NID=0Ch 01h: Pin Widget NID=0Dh Other: Reserved

Codec Response for Multiplexer Widget NID=22h

Bit	Description
31:8	0's.
7:0	Connection Index Currently Set (Default value is 00h). 00h: Pin Widget NID=18h 01h: Pin Widget NID=19h 02h: Pin Widget NID=1Ah 03h: Pin Widget NID=1Bh 04h: Pin Widget NID=1Dh 05h: Pin Widget NID=0Bh 06h: Mixer Widget NID=12h 07h: Mixer Widget NID=0Ch 08h: Mixer Widget NID=0Dh Other: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.3. Verb – Set Connection Select (Verb ID=701h)

Table 35. Verb – Set Connection Select (Verb ID=701h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=701h	Select Index [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

8.4. Verb – Get Connection List Entry (Verb ID=F02h)

Table 36. Verb – Get Connection List Entry (Verb ID=F02h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F02h	Offset Index – N[7:0]

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=08h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 23h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=09h ADC

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 22h (Sum Widget) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Bh Mixer

Bit	Description
31:24	Connection List Entry (N+3), (N+2). Returns 1Bh (LINE2) for N=0~3. Returns 00h for N>3.
23:16	Connection List Entry (N+1). Returns 1Ah (LINE1) for N=0~3. Returns 00h for N>3.
15:8	Connection List Entry (N+1). Returns 19h (MIC2) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 18h (MIC1) for N=0~3. Returns 1Dh (PCBEEP) for N=4~7. Returns 00h for N>3.

Codec Response for NID=0Ch

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LINE-OUT DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Dh

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.

15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 03h (SURR DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=0Fh

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Bh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 02h (LINE-OUT DAC) for N=0~3. Returns 00h for N>3.

Codec Response for NID=14h (Pin Widget: LINE-OUT)

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Dh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 0Ch (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=17h (Pin Widget: MONO-OUT)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 0Fh (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=18h (Pin Widget: MIC1)

Bit	Description
31:8	Connection List Entry (N+3), (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Returns 0Dh (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=1Ah (Pin Widget: LINE1), 1Bh (Pin Widget: LINE2), 21h (Pin Widget: HP-OUT)

Bit	Description
31:16	Connection List Entry (N+3), (N+2). Returns 0000h.
15:8	Connection List Entry (N+1). Returns 0Dh (Mixer) for N=0~3. Returns 00h for N>3.
7:0	Connection List Entry (N). Returns 0Ch (Mixer) for N=0~3. Returns 00h for N>3.

Codec Response for NID=1Eh (Pin Widget: S/PDIF-OUT)

Bit	Description
31:8	Connection List Entry (N+3, (N+2), (N+1). Returns 000000h.
7:0	Connection List Entry (N). Return 06h (S/PDIF-OUT converter) for N=0~3. Returns 00h for N>3.

Codec Response for NID=22h (MUX Widget)

Bit	Description
31:24	Connection List Entry (N+3). Return 1Bh (Pin Complex - LINE2) for N=0~3. Return 00h for N>3.
23:16	Connection List Entry (N+2). Return 1Ah (Pin Complex - LINE1) for N=0~3. Return 12h (Pin Complex – Digital MIC) for N=4~7. Return 00h for N>7.
15:8	Connection List Entry (N+1). Return 19h (Pin Complex - MIC2) for N=0~3. Return 0Bh (Mixer) for N=4~7. Return 00h for N>7.
7:0	Connection List Entry (N). Return 18h (Pin Complex - MIC1) for N=0~3. Return 1Dh (Pin Complex - PCBEEP) for N=4~7. Return 00h for N>7.

Codec Response for NID=23h (Mixer Widget)

Bit	Description
31:24	Connection List Entry (N+3). Return 1Bh (Pin Complex - LINE2) for N=0~3. Return 00h for N>3.
23:16	Connection List Entry (N+2). Return 1Ah (Pin Complex - LINE1) for N=0~3. Return 00h for N>3.
15:8	Connection List Entry (N+1). Return 19h (Pin Complex - MIC2) for N=0~3. Return 0Bh (Mixer Widget) for N=4~7. Return 00h for N>3.
7:0	Connection List Entry (N). Return 18h (Pin Complex - MIC1) for N=0~3. Return 1Dh (Pin Complex - PCBEEP) for N=4~7. Return 00h for N>7.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.5. Verb – Get Processing State (Verb ID=F03h)

Table 37. Verb – Get Processing State (Verb ID=F03h)

Get Command Format	Codec Response Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F03h	0's

Response [31:0]
32-bit response

Codec Response for All NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.6. Verb – Set Processing State (Verb ID=703h)

Table 38. Verb – Set Processing State (Verb ID=703h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=703h	Processing State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.7. Verb – Get Coefficient Index (Verb ID=Dh)

Table 39. Verb – Get Coefficient Index (Verb ID=Dh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=20h	Verb ID=Dh	0's

Codec Response Format

Response [31:0]
Bit [15:0] are Coefficient Index

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Coefficient Index.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.8. Verb – Set Coefficient Index (Verb ID=5h)

Table 40. Verb – Set Coefficient Index (Verb ID=5h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=20h	Verb ID=5h	Coefficient Index [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's.

8.9. Verb – Get Processing Coefficient (Verb ID=Ch)

Table 41. Verb – Get Processing Coefficient (Verb ID=Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=20h	Verb ID=Ch	0's

Codec Response Format

Response [31:0]
Processing Coefficient [15:0]

Codec Response for NID=20h (Realtek Vendor Registers)

Bit	Description
31:16	Reserved. Read as 0's.
15:0	Processing Coefficient.

Codec Response for Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.10. Verb – Set Processing Coefficient (Verb ID=4h)

Table 42. Verb – Set Processing Coefficient (Verb ID=4h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=20h	Verb ID=4h	Coefficient [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for All NID

Bit	Description
31:0	0's

8.11. Verb – Get Amplifier Gain (Verb ID=Bh)

This verb is used to get gain/attenuation settings from each widget.

Table 43. Verb – Get Amplifier Gain (Verb ID=Bh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Bh	'Get' payload [15:0]

Codec Response Format

Response [31:0]
Bit[7:0] are responsible for 'Get'

'Get' Payload in Command Bit[15:0]

Bit	Description
15	Get Input/Output. 0: Input amplifier gain is requested 1: Output amplifier gain is requested
14	Reserved. Read as 0.
13	Get Left/Right. 0: Right amplifier gain is requested 1: Left amplifier gain is requested
12:4	Reserved. Read as 0's.
3:0	Index[3:0] for Input Source. Select amplifier for this converter. If a widget has no multiple input sources, the index will be ignored.

Codec Response for NID=02h (LINE-OUT DAC) and 03h (SURR DAC)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': 6-bit control specifying the volume from–65.25dB~ 0dB in 0.75dB step.

Node	Gain[6:0] (Default)	Gain Range
LINE-OUT DAC(NID=02h)	1010111b=57h (0dB)	–65.25dB~0dB in 0.75dB step
SURR DAC (NID=03h)	1010111b=57h (0dB)	–65.25dB~0dB in 0.75dB step

Codec Response for NID=08h, 09h (ADCs)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. Specifying the volume from –16.5dB~ 30dB in 1.5dB step. **Node** / **Gain[6:0] Default** / **Gain Range** ADC (NID=08h) / 0001011b=0Bh (0dB) / –16.5dB~30dB in 1.5dB step ADC(NID=09h) / 0001011b=0Bh (0dB) / –16.5dB~30dB in 1.5dB step Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=0Ch, 0Dh and 0Fh (Mixer)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': 1: Mute, 0:Unmute (Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0's (No Output Amplifier Gain).

Codec Response for NID=18h, 1Ah and 1Bh (Pin widget: MIC1, LINE1 and LINE2)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': 1: Mute, 0:Unmute (Output Amplifier Mute, default=1).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. The volume 0dB/12dB/24dB/36dB in 12dB per step (default=0, 0dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=12h and 19h (Pin widget: DMIC and MIC2)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. The volume 0dB/12dB/24dB/36dB in 12dB per step (default=0, 0dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=14h, 17h and 21h (Pin widget: SPK-OUT, MONO-OUT and HP-OUT)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Mute). Payload[15] is 1 in 'Get Amplifier Gain': 1: Mute, 0:Unmute (Output Amplifier Mute, default=1).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0's (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

Codec Response for NID=0Bh (Mixer)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default for all) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Gain [6:0]. Specifying the volume from -34.5dB~+12dB in 1.5dB step (Default: 17h, 0dB). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

	Index=0 (MIC1)	Index=1 (MIC2)	Index=2 (LINE1)	Index=3 (LINE2)	Index=4 (PCBEEP)	Index=5 (LINE-OUT DAC)
Mute [7]	0/1	0/1	0/1	0/1	0/1	0
Gain [6:0]	00h-1Fh	00h-1Fh	00h-1Fh	00h-1Fh	00h-1Fh	00h-1Fh
Default[7:0]	10000000	10000000	10000000	10000000	10000000	10000000

	Index > 6 Other
Mute [7]	0/1
Gain [6:0]	00h
Default[7:0]	00000000

Codec Response for NID=23h (Mixer)

Bit	Description
31:8	0's.
7	Payload[15] is 0 in 'Get Amplifier Gain': Input Amplifier Mute. 0: Unmute, 1: Mute (Default for all) Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Mute).
6:0	Payload[15] is 0 in 'Get Amplifier Gain': Read as 0 (No Input Amplifier Gain). Payload[15] is 1 in 'Get Amplifier Gain': Read as 0 (No Output Amplifier Gain).

	Index=0 (MIC1)	Index=1 (MIC2)	Index=2 (LINE1)	Index=3 (LINE2)	Index=4 (PCBEEP)	Index=5 (Mixer)	Index>7 (Other)
Mute [7]	0/1	0/1	0/1	0/1	0/1	0/1	0
Gain [6:0]	0s	0s	0s	0s	0s	0s	0
Default[7:0]	10000000	10000000	10000000	10000000	10000000	10000000	00000000

	Index=6 (LINE-OUT DAC)	Index=7 (SURR DAC)
Mute [7]	0/1	0/1
Gain [6:0]	0s	0s
Default[7:0]	10000000	10000000

Codec Response to Other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.12. Verb – Set Amplifier Gain (Verb ID=3h)

This verb is used to set amplifier gain/attenuation in each widget.

Table 44. Verb – Set Amplifier Gain (Verb ID=3h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=3h	'Set' payload [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
15	Set Output Amp. 1 indicates output amplifier gain will be set.
14	Set Input Amp. 1 indicates input amplifier gain will be set.
13	Set Left Amp. 1 indicates left amplifier gain will be set.
12	Set Right Amp. 1 indicates right amplifier gain will be set.
11:8	Index Offset (for input amplifiers on Sum widgets and Selector Widgets). 5 bits index offset in connection list is used to select which input gain will be set on a mixer or a multiplexer widget. The index is ignored if the node is not a mixer or a multiplexer widget, or the 'Set Input Amp' bit is not set.
7	Mute. 0: Unmute 1: Mute (-∞gain)
6:0	Gain[6:0]. A 7-bit step value specifying the amplifier gain.

8.13. Verb – Get Converter Format (Verb ID=Ah)

Table 45. Verb – Get Converter Format (Verb ID=Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=Ah	0's

Codec Response Format

Response [31:0]
Bit[15:0] are converter format

Codec Response for NID=02h, 03h, 06h (Output Converters: LINE-OUT DAC, SURR DAC, S/PDIF-OUT).
Codec Response for NID=08h, 09h (Input Converters: ADCs)

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8 The ALC221 does not support Divisor. Always read as 000b.
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels ..... 15: 16 channels

	BASE	MULT	DIV	BITS	Sample Rate
NID=02h (LOUT-OUT DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K,192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=03h (SURR DAC)	0	000b, 001b, 011b	000b	001b, 010b, 011b	48K, 96K,192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=06h (S/PDIF-OUT)	0	000b, 001b, 011b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b, 001b	000b	001b, 010b, 011b, 100b	44.1K, 88.2K
	0	001b	010b	001,010b, 011b	32K
NID=08h (ADC)	0	000b, 001b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K
NID=09h (ADC)	0	000b, 001b	000b	001b, 010b, 011b, 100b	48K, 96K, 192K
	1	000b	000b	001b, 010b, 011b	44.1K

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.14. Verb – Set Converter Format (Verb ID=2h)

Table 46. Verb – Set Converter Format (Verb ID=2h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:16]	Payload Bit [15:0]
Cad=X	Node ID=Xh	Verb ID=2h	Set format [15:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Set' Payload in Command Bit[15:0]

Bit	Description
31:16	Reserved. Read as 0.
15	Stream Type (TYPE). 0: PCM 1: Non-PCM
14	Sample Base Rate (BASE). 0: 48kHz 1: 44.1kHz
13:11	Sample Base Rate Multiple (MULT). 000b: *1 001b: *2 010b: *3 011b: *4 100b~111b: Reserved.
10:8	Sample Base Rate Divisor (DIV). 000b: /1 001b: /2 010b: /3 011b: /4 100b: /5 101b: /6 110b: /7 111b: /8
7	Reserved. Read as 0.
6:4	Bits per Sample (BITS). 000b: 8 bits 001b: 16 bits 010b: 20 bits 011b: 24 bits 100b: 32 bits 101b~111b: Reserved
3:0	Number of Channels. 0: 1 channel 1: 2 channels 2: 3 channels ..... 15: 16 channels

8.15. Verb – Get Power State (Verb ID=F05h)

Table 47. Verb – Get Power State (Verb ID=F05h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F05h	0's

Codec Response Format

Response [31:0]
Power State [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:11	Reserved, read as 0s.

Codec Response for NID=01h (Audio Function Group)

10	PS-Settings Reset 0: Setting of widgets has been reset during any low power state. 1: The setting were changed from the defaults have been reset to their default during any low power state. Read as 1 after single-function-reset in D0/D1/D2/D4. Read as 1 after link-reset in D0/D1/D2/D4. Read as 1 after double-function-reset in D0/D1/D2/D3Clk. The PS-Settings Reset bit will be cleared to zero after Get-Power-State-verb's response.
9	PS-ClkStopOk 0: No capability to operate normally with BITCLK stop 1: operate properly with no BICLK Read as 1 when PS-Set, Set Power State [1:0] = 011b. Read as 0 when PS-Set, Set Power State [1:0] = 000b/001b/010b/100b.
8	PS-Error No support in ALC221
7	**Reserved**, read as 0s.
6:4	PS-Act. Actual Power State [1:0]. 000: Power state is D0 001: Power state is D1 010: Power state is D2 011: Power state is D3 100: Power state is D4 PS-Act indicates the actual power state of the referenced node. For Audio Function Group nodes (NID=01h), PS-Act is always equal to PS-Set. D0: Fully on D1: The lowest possible power consuming state it can return to fully on state (D0) wthin 10msec, except analog pass through is fully on. (Mixer on) D2: The lowest possible power consuming state it can return to fully on state (D0) wthin 10msec. D3: The lowest possible power consuming state under software control. D4: The lowest power consumption state
3	Reserved. Read as 0.
2:0	PS-Set, Set Power State [1:0]. 000: Power state is D0 001: Power state is D1 010: Power state is D2 011: Power state is D3 100: Power state is D4 PS-Set controls the current power setting of the referenced node.

Note: Specific blocks will be powered down in each power state. Refer to section 7.5 Power Management, page 22.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.16. Verb – Set Power State (Verb ID=705h)

Table 48. Verb – Set Power State (Verb ID=705h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=705h	Power State [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Power State' in Command Bit[7:0]

Bit	Description
7:6	Reserved. Read as 0's.
5:4	PS-Act. Actual Power State [1:0]. 000: Power state is D0 001: Power state is D1 010: Power state is D2 011: Power state is D3 100: Power state is D4 PS-Act indicates the actual power state of the referenced node.
3:2	Reserved. Read as 0's.
1:0	PS-Set. Set Power State [1:0]. 000: Power state is D0 001: Power state is D1 010: Power state is D2 011: Power state is D3 100: Power state is D4

8.17. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Table 49. Verb – Get Converter Stream, Channel (Verb ID=F06h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F06h	0's

Codec Response Format

Response [31:0]
Stream & Channel [7:0]

Codec Response for NID=02h, 03h, 06h (Output Converters: LINE-OUT DAC, SURR DAC, S/PDIF-OUT).
Codec Response for NID=08h, 09h (Input Converters: ADCs)

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
3:0	Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.18. Verb – Set Converter Stream, Channel (Verb ID=706h)

Table 50. Verb – Set Converter Stream, Channel (Verb ID=706h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=706h	Stream & Channel [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Stream and Channel' in Command Bit[7:0]

Bit	Description
31:8	Reserved. Read as 0's.
7:4	Set Stream[3:0]. The link stream used by the converter. 0000b is stream 0, 0001b is stream 1, etc.
1:0	Set Channel[3:0]. The lowest channel used by the converter. A stereo converter will use the set channel n as well as n+1 for its left and right channel.

Note: This verb assigns stream and channel for output converters (NID=02h, 03h, 06h) and input converters (NID=08h, 09h). Other widgets will ignore this verb.

8.19. Verb – Get Pin Widget Control (Verb ID=F07h)

Table 51. Verb – Get Pin Widget Control (Verb ID=F07h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F07h	0's

Codec Response Format

Response [31:0]
Pin Control [7:0]

Codec Response for pin widget NID=12h, 14h, 17h, 18h~1Bh, 1Dh, 1Eh and 21h. (Pin Complex: DMIC, LINE-OUT, MONO-SPK-OUT, MIC1, MIC2, LINE1, LINE2, PCBEEP, S/PDIF_OUT and HP-OUT).

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable (Headphone Amplifier Enable, EN_AMP for an I/O unit). 0: Disabled *(Default for NID= 1Ah and 21h)* 1: Enabled.
6	Out Enable (Output Buffet Enable, EN_OBUF for an I/O unit). 0: Disabled *(Default for NID=14h, 17h, 18h, 1Ah.1Bh, and 21h)* 1: Enabled. *(Default for NID= 1Eh)*
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled *(Default for NID=12h)* 1: Enabled. *(Default for NID= 18h, 19h, 1Ah, 1Bh, and 1Dh)*
4:3	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD (2.3V) 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD (3.0V) 101b: 100% of AVDD (4.0V) 110b~111b: Reserved

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.20. Verb – Set Pin Widget Control (Verb ID=707h)

Table 52. Verb – Set Pin Widget Control (Verb ID=707h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=707h	Pin Control [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Pin Control' in command [7:0]: pin widget NID=12h, 14h, 17h, 18h~1Bh, 1Dh, 1Eh and 21h. (Pin Complex: DMIC, LINE-OUT, MONO-SPK-OUT, MIC1, MIC2, LINE1, LINE2, PCBEEP, S/PDIF_OUT and HP-OUT).

Bit	Description
31:1	Reserved. Read as 0's.
7	H-Phn Enable. 0: Disabled 1: Enabled
6	Out Enable. 0: Disabled 1: Enabled
5	In Enable (Input Buffer Enable, EN_IBUF for an I/O unit). 0: Disabled 1: Enabled
4:	Reserved.
2:0	VrefEn (Vrefout Enable Control). 000b: Hi-Z (Disabled) 001b: 50% of AVDD 010b: Ground 0V 011b: Reserved 100b: 80% of AVDD 101b: 100% of AVDD 110b~111b: Reserved

8.21. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Determines whether a widget is enabled to send an unsolicited response. An HDA codec can use an unsolicited response to inform software of a real time event.

Table 53. Verb – Get Unsolicited Response Control (Verb ID=F08h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F08h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (GPIO in Audio Function Group), 14h, 18h~1Ah, 1Eh and 21h

Bit	Description
31:8	Reserved. Read as 0's.
7	Unsolicited Response is Enabled. 0: Disabled 1: Enabled
6:4	Reserved. Read as 0's.
3:0	Assigned Tag for Unsolicited Response. The tag[3:0] is assigned by software to determine which widget generates unsolicited responses.

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.22. Verb – Set Unsolicited Response Control (Verb ID=708h)

Enable a widget to generate an unsolicited response.

Table 54. Verb – Set Unsolicited Response Control (Verb ID=708h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=708h	EnableUnsol [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'EnableUnsol' in Command Bit[7:0]
For NID=01h (GPIO in Audio Function Group), 14h, 18h~1Ah, 1Eh and 21h

Bit	Description
31:8	Reserved. Read as 0's.
7	Enable Unsolicited Response. 0: Disable 1: Enable
6:4	Reserved. Read as 0's.
3:0	Tag for Unsolicited Response. Tag[3:0] is defined by software to assign a 4-bit tag for nodes that are enabled to generate unsolicited responses.

8.23. Verb – Get Pin Sense (Verb ID=F09h)

Returns the Presence Detect status and the impedance of a device attached to the pin.

Table 55. Verb – Get Pin Sense (Verb ID=F09h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F09h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response: Pin widget 14h (LINE-OUT), 18h-1Bh (MIC1, MIC2, LINE1, LINE2), 21h (HP-OUT)

Bit	Description
31	Presence Detect Status. 0: No device is attached to the pin 1: Device is attached to the pin
30:0	Measured Impedance. *Note: The ALC221 does not support impedance sensing. Read as 0's.*

Codec Response for other NID

Bit	Description
31:0	Not Supported (returns 00000000h).

8.24. Verb – Execute Pin Sense (Verb ID=709h)

Table 56. Verb – Execute Pin Sense (Verb ID=709h)

Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=709h	Right Channel[0]

Codec Response Format

Response [31:0]
0's for all nodes

'Payload' in Command Bit[7:0]

Bit	Description
7:1	Reserved. Read as 0's.
0	Right (Ring) Channel Select. 0: Sense Left channel (Tip) 1: Sense Right channel (Ring)

Note: The ALC221 does not support 'Execute Pin Sense' and will ignore this verb and respond with 0's.

8.25. Verb – Get Configuration Default (Verb ID=F1Ch)

Read the 32-bit sticky register for each Pin Widget configured by software.

Table 57. Verb – Get Configuration Default (Verb ID=F1Ch)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F1Ch	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for Pin Widget: NID=12h (Digital MIC), 14h (LINE-OUT), 21h (HP-OUT), 17h (MONO-SPK-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Bh (LINE2), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT)

Bit	Description
31:0	32 bits configured information for each pin widget. Default value for each pin widget [31:30]: Port Connectivity [29:24]: Location [23:20]: Default Device [19:16]: Connection Type [15:12]: Color [11:08]: Misc [07:04]: Default Association [03:00]: Sequence

NID 14h	NID 17h	NID 18h	NID 19h	NID 1Ah	NID 1Bh
01014030h	411111F0h	01A19050h	02A19080h	0181305Fh	411111F0h

NID 1Dh	NID 21h	NID 1Eh	NID 12h❹
411111F0h	411111F0h	01441170h	411111F0h

Note: The 32-bit registers for each Pin Widget are sticky and will not be reset by a LINK Reset or Codec Reset (Function Reset Verb).

Note: The default configuration for each pin widget,

	NID-14h	NID-17h	NID-18h	NID-19h	NID-1Ah	NID-1Bh
Name	FRONT	MONO	MIC1	MIC2	LINE1	LINE2
Port	Jack	No Connection	Jack	Jack	Jack	No Connection
Location	Rear	Other	Rear	Front	Rear	Other
Device	Line Out	Other	Mic In	Mic In	Line In	Other
Con Type	1/8" Jack	Other	1/8" Jack	1/8" Jack	1/8" Jack	Other
Color	Green	Other	Pink	Pink	Blue	Other

	NID-1Dh	NID-21h	NID-1Eh	NID-12h
Name	PCBEEP	HP-OUT	S/PDIF-OUT	DMIC-1/2
Port	No Connection	No Connection	Jack	No Connection

Location	Other	Other	Rear	Other
Device	Other	Other	S/PDIF Out	Other
Con Type	Other	Other	RCA	Other
Color	Other	Other	Orange	Other

8.26. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

The BIOS can use this verb to figure out the default conditions for the Pin Widgets 14h~1Bh and 1Eh~1Fh such as placement and expected default device.

Table 58. Verb – Set Configuration Default Bytes 0, 1, 2, 3 (Verb ID=71Ch/71Dh/71Eh/71Fh for Bytes 0, 1, 2, 3)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=71Ch, 71Dh, 71Eh, 71Fh	Label [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Note: Supported by Pin Widget NID=12h (Digital MIC), 14h (LINE-OUT), 21h (HP-OUT), 17h (MONO-SPK-OUT), 18h (MIC1), 19h (MIC2), 1Ah (LINE1), 1Bh (LINE2), 1Dh (PCBEEP), 1Eh (S/PDIF-OUT)

Codec Response for All NID

Bit	Description
31:0	0's.

8.27. Verb – Get BEEP Generator (Verb ID=F0Ah)

Table 59. Verb – Get BEEP Generator (Verb ID=F0Ah)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F0Ah	0's

Codec Response Format

Response [31:0]
Divider [7:0]

'Response' for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.28. Verb – Set BEEP Generator (Verb ID=70Ah)

Table 60. Verb – Set BEEP Generator (Verb ID=70Ah)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Ah	Divider [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Divider' in Set Command

Bit	Description
31:8	Reserved.
7:0	Frequency Divider, F[7:0]. The internal BEEP frequency is the result of dividing the 48kHz clock by 4 times the number specified in F[7:0]. The lowest tone is 48kHz/(255*4)=47Hz. The highest tone is 48kHz/(1*4)=12kHz. A value of 00h in F[7:0] disables the internal BEEP generator and allows external PCBEEP input.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.29. Verb – Get GPIO Data (Verb ID=F15h)

Table 61. Verb – Get GPIO Data (Verb ID=F15h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F15h	0's

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Data. Not supported in the ALC221.
1:0	GPIO[1:0] Data. The value written (output) or sensed (input) on the corresponding pin if it is enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.30. Verb – Set GPIO Data (Verb ID=715h)

Table 62. Verb – Set GPIO Data (Verb ID=715h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=715h	Data [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

'Data' in Set command for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Output Data. Not supported in the ALC221.
1:0	GPIO[1:0] Output Data. The value written determines the value driven on a pin that is configured as an output pin.

Codec Response for All NID

Bit	Description
31:0	0's.

8.31. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Table 63. Verb – Get GPIO Enable Mask (Verb ID=F16h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F16h	0's

Codec Response Format

Response [31:0]
EnableMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:2	Reserved.
1:0	GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state. 1: The corresponding GPIO pin is enabled. It's behavior is determined by the GPIO direction control.

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description

Codec Response for Other NID

31:0	0's.

8.32. Verb – Set GPIO Enable Mask (Verb ID=716h)

Table 64. Verb – Set GPIO Enable Mask (Verb ID=716h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=716h	Enable Mask [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Enable Mask. Not supported in the ALC221.
1:0	GPIO[1:0] Enable Mask. 0: The corresponding GPIO pin is disabled and is in Hi-Z state 1: The corresponding GPIO pin is enabled. It's behavior is determined by the GPIO direction control

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for All NID

Bit	Description
31:0	0's.

8.33. Verb – Get GPIO Direction (Verb ID=F17h)

Table 65. Verb – Get GPIO Direction (Verb ID=F17h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F17h	0's

Codec Response Format

Response [31:0]
Direction [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Direction Control. Not supported in the ALC221.
1:0	GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.34. Verb – Set GPIO Direction (Verb ID=717h)

Table 66. Verb – Set GPIO Direction (Verb ID=717h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=717h	Direction [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Direction Control. Not supported in the ALC221.
1:0	GPIO[1:0] Direction Control. 0: The corresponding GPIO pin is configured as an input 1: The corresponding GPIO pin is configured as an output

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.35. Verb – Get GPIO Wake Enable Mask(Verb ID=F18h)

Table 67. Verb – Get GPIO Wake Enable Mask (Verb ID=F18h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F18h	0's

Codec Response Format

Response [31:0]
WakeEnalbeMask [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Wake Enable Mask. Not supported in the ALC221.
1:0	GPIO[1:0] Wake Enable Mask. 0: The corresponding GPIO pin will not generate a wake-up event 1: The corresponding GPIO pin will generate a wake-up event

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.36. Verb – Set GPIO Wake Enable Mask (Verb ID=718h)

Table 68. Verb – Set GPIO Wake Enable Mask (Verb ID=718h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=718h	WakeEnalbeMask [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Wake Enable Mask. Not supported in the ALC221
1:0	GPIO[1:0] Wake Enable Mask. 0: The corresponding GPIO pin will not generate a wake-up event 1: The corresponding GPIO pin will generate a wake-up event

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.37. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Table 69. Verb – Get GPIO Unsolicited Response Enable Mask (Verb ID=F19h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=F19h	0's

Codec Response Format

Response [31:0]
UnsolEnable [7:0]

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC221.
1:0	GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Codec Response for NID=01h (Audio Function Group)

Note: All nodes except Audio Function Group (NID=01h) will ignore this verb.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.38. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Table 70. Verb – Set GPIO Unsolicited Response Enable Mask (Verb ID=719h)

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=719h	UnsolEnable [7:0]

Codec Response Format

Response [31:0]
0's for all nodes

Codec Response for NID=01h (Audio Function Group)

Bit	Description
31:8	Reserved.
7:2	GPIO[7:2] Unsolicited Enable Mask. Not supported in the ALC221
1:0	GPIO[1:0] Unsolicited Enable Mask. 0: Unsolicited response will not be sent on link 1: Unsolicited response will be sent on link when state of corresponding GPIO has been changed

Note 1: All nodes except the Audio Function Group (NID=01h) will ignore this verb.
Note 2: The unsolicited response of corresponding GPIO is enabled when it's 'Enable Mask' and Verb-'Unsolicited Response' for NID=01h are enabled.

Codec Response for Other NID

Bit	Description
31:0	0's.

8.39. Verb – Function Reset (Verb ID=7FFh)

Table 71. Verb – Function Reset (Verb ID=7FFh)

Command Format (NID=01H)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=01h	Verb ID=7FFh	0's

Codec Response Format

Response [31:0]
0's

Codec Response

Bit	Description
31:0	Reserved. Read as 0's.

Note: The Function Reset command causes all widgets in the ALC221 to return to their power-on default state.

8.40. Verb – Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Table 72. Verb –Get Digital Converter Control 1 & Control 2 (Verb ID=F0Dh, F0Eh)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=F0Dh/F0Eh	0's

Codec Response Format

Response [31:0]
Bit[31:0] are SIC bit

NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Dh (Control 1 for SIC bit[15:0]).
NID=06h (S/PDIF-OUT) Response to 'Get verb' – F0Eh (Control 2 for SIC bit[31:16])

Bit	Description – SIC (S/PDIF IEC Control) Bit[31:0]
31:24	Read as 0's.
23	**Keep Alive Enable** 0: Disable SPDIF Out would be disable in D2/D3/D4 mode 1: Enable SPDIEF Out would be keep alive in D0/D1/D2/D3, but not D4.
12:15	Reserved. Read as 0's.
14:8	CC[6:0] (Category Code).
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

Codec Response for Other NID

Bit	Description
31:0	0's.

8.41. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Table 73. Verb – Set Digital Converter Control 1 & Control 2 (Verb ID=70Dh, 70Eh)

Set Command Format (Verb ID=70Dh, Set Control 1)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Dh	SIC [7:0]

Codec Response Format

Response [31:0]
0's

Set Command Format (Verb ID=70Eh, Set Control 2)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
Cad=X	Node ID=Xh	Verb ID=70Eh	SIC [15:8]

Codec Response Format

Response [31:0]
0's

'Payload' in Set Control 1 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	LEVEL (Generation Level).
6	PRO (Professional or Consumer Format). 0: Consumer format 1: Professional format
5	/AUDIO (Non-Audio Data Type). 0: PCM data 1: AC3 or other digital non-audio data
4	COPY (Copyright). 0: Asserted 1: Not asserted
3	PRE (Pre-Emphasis). 0: None 1: Filter pre-emphasis is 50/15 microseconds
2	VCFG for Validity Control (control V bit and data in Sub-Frame).
1	V for Validity Control (control V bit and data in Sub-Frame).
0	Digital Enable. DigEn. 0: OFF 1: ON

'Payload' in Set Control 2 for NID=06h (S/PDIF-OUT)

Bit	Description – SIC (S/PDIF IEC Control) Bit[7:0]
7	Reserved. Read as 0's.
6:0	CC[6:0] (Category Code).

8.42. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

32-bit Read/Write register for Audio Function Group (NID=01h)

Table 74. Verb – Get Subsystem ID [31:0] (Verb ID=F20h/F21h/F22h/F23h)

Get Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=01h	Verb ID=F20h	0s

Codec Response Format

Response [31:0]
32-bit Response

Codec Response for NID=01h

Bit	Description
31:16	Subsystem ID[23:8] (Default=10ECh).
15:8	Subsystem ID[7:0] (Default=02h).
7:0	Assembly ID[7:0] (Default=21h).

8.43. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Table 75. Verb – Set Subsystem ID [31:0] (Verb ID=723h for [31:24], 722h for [23:16], 721h for [15:8], 720h for [7:0])

Set Command Format

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd = X	Node ID=01h	Verb ID=723h, 722h, 721h, 720h	Label [7:0]

Codec Response Format

Response [31:0]
0s for All Nodes

Codec Response for all NID

Bit	Description
31:0	0s.

8.44. Verb – Get EAPD Control (Verb ID=F0Ch for Get)

Table 76. Verb – Get EAPD Control (Verb ID=F0Ch)

Get Command Format (NID=14h, 17h and 21h)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=14h/17h/21h	Verb ID=F0Ch	0s

Codec Response Format

Response [31:0]
Bit[1] is EAPD Control

Codec response in Get Command for NID=14h (LINE-OUT), 17h (MONO-SPK-OUT) and 21h (HP-OUT)

Bit	Description
31:3	Reserved.
2	L-R Swap. The ALC221 does not support swapping left and right channels. Read as 0.
1	EAPD Value. 0: EAPD pin state is low 1: EAPD pin state is high
0	Bridge Tied Load (BTL) Enable. The ALC221 does not support BTL output. Read as 0.

Codec Response in for Other NID

Bit	Description
31:0	0's.

8.45. Verb – Set EAPD Control (Verb ID=70Ch for Set)

Table 77. Verb – Set EAPD Control (Verb ID=70Ch for Set)

Set Command Format (NID=14h, 17h and 21h)

Bit [31:28]	Bit [27:20]	Bit [19:8]	Payload Bit [7:0]
CAd=X	Node ID=14h/17h/21h	Verb ID=70Ch	Bit[1] is EAPD Control

Codec Response Format

Response [31:0]
0s

Payload in Set Command for NID=14h (LINE-OUT), 17h (MONO-SPK-OUT) and 21h (HP-OUT)

Bit	Description
7:3	Reserved, Written Data is Ignored.
2	L-R Swap. The ALC221 does not support swapping left and right channels, written data is ignored.
1	EAPD Value. 0: EAPD pin state is low 1: EAPD pin state is high
0	Bridge Tied Load (BTL) Enable. The ALC221 does not support BTL output. Written data is ignored.

Codec Response

Bit	Description
31:0	0's.

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 78. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DVDD	3.0	3.3	3.6	V
Digital Power for Link*1	DVDD-IO	1.5	3.3	3.6	V
Analog Power	AVDD1, AVDD2	4.5	5.0	5.5	V
BTL Analog Power	PVDD	4.5	5.0	5.5	V
Ambient Operating Temperature	Ta	0	-	+70	°C
Storage Temperature	Ts	-	-	+125	°C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
All Pins	3500V				

Note1: DVDD-IO must be lower than DVDD.

9.1.2. Threshold Voltage

DVDD-IO=3.3V±5%, $T_{ambient}$=25°C, with 50pF external load.

Table 799. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IL}	-	-	0.30*DVDDIO	V
High Level Input Voltage (BCLK, RST#, SDO, SYNC, SDI)	V_{IH}	0.65*DVDDIO	-	-	V
Low Level Input Voltage (GPIOs)	V_{IL}	-	(2/3)*DVDD	-	V
High Level Input Voltage (GPIOs)	V_{IH}	-	(2/3)*DVDD	-	V
High Level Output Voltage (S/PDIF-OUT)	V_{OH}	0.9*DVDD	-	-	V
Low Level Output Voltage (S/PDIF-OUT)	V_{OL}	-	-	0.1*DVDD	V
Input Leakage Current	-	-10	-	10	µA
Output Leakage Current (Hi-Z)	-	-10	-	10	µA
Output Buffer Drive Current	-	-	5	-	mA
Internal Pull Up Resistance	-	-	47k	-	Ω

9.1.3. Digital Filter Characteristics

Table 80. Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-76.0	-	dB
	Passband Ripple	-	±0.05	-	dB
DAC Lowpass Filter	Passband	0	-	0.454*Fs (-1dB)	kHz
	Stopband	28.8	-	-	kHz
	Stopband Rejection	-	-78.5	-	dB
	Passband Ripple	-	±0.05	-	dB

9.1.4. S/PDIF Output Characteristics

DVDD=3.3V, $T_{ambient}$=25°C, with 75Ω external load.

Table 81. S/PDIF Input/Output Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT High Level Output	V_{OH}	3.0	3.3	-	V
S/PDIF-OUT Low Level Output	V_{OL}	-	0	0.3	V

9.2. AC Characteristics

9.2.1. Link Reset and Initialization Timing

Table 82. Link Reset and Initialization Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# Active Low Pulse Width	T_{RST}	100.167	-	-	µs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	100	-	-	µs
SDI Initialization Request	T_{FRAME}	-	-	25	Frame Time

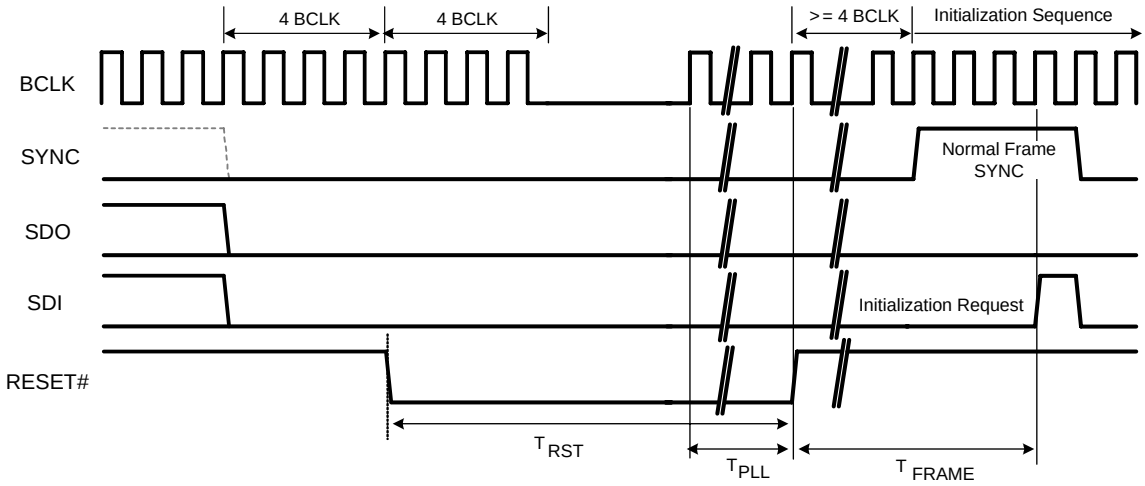


Figure 13. Link Reset and Initialization Timing

9.2.2. Link Timing Parameters at the Codec

Table 83. Link Timing Parameters at the Codec

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK Frequency	-	-	24.0	-	MHz
BCLK Period	T_{cycle}	-	41.67	-	ns
BCLK Jitter	T_{jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{high}	18.75 (45%)	-	22.91 (55%)	ns (%)
BCLK Low Pulse Width	T_{low}	18.75 (45%)	-	22.91 (55%)	ns (%)
SDO Setup Time at Both Rising and Falling Edge of BCLK	T_{setup}	2.1	-	-	ns
SDO Hold Time at Both Rising and Falling Edge of BCLK	T_{hold}	2.1	-	-	ns
SDI Valid Time After Rising Edge of BCLK (1:50pF external load)	T_{tco}	-	7.5	8.0	ns
SDI Flight Time	T_{flight}	-	2.0	-	ns

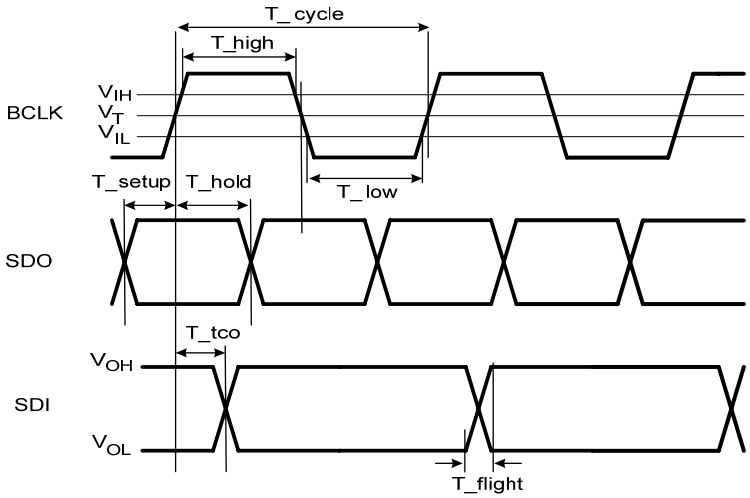


Figure 14. Link Signals Timing

9.2.3. S/PDIF Output Timing

Table 84. S/PDIF Output Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
S/PDIF-OUT Frequency*1	-	-	3.072	-	MHz
S/PDIF-OUT Period*1	T_{cycle}	-	325.6	-	ns
S/PDIF-OUT Jitter	T_{jitter}	-	-	4	ns
S/PDIF-OUT High Level Width*1	T_{High}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Low Level Width*1	T_{Low}	156.2 (48%)	162.8 (50%)	169.2 (52%)	ns (%)
S/PDIF-OUT Rising Time	T_{rise}	-	2.0	-	ns
S/PDIF-OUT Falling Time	T_{fall}	-	2.0	-	ns

**1: Bit parameters for 48kHz sample rate of S/PDIF-OUT.*

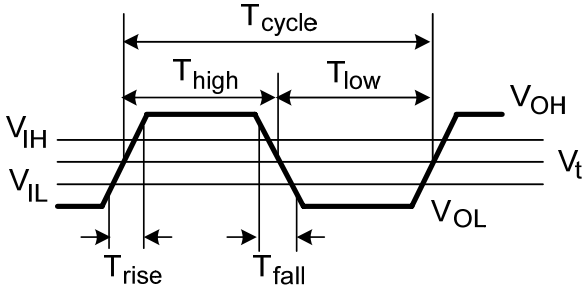


Figure 15. Output Timing

9.3. Analog Performance

Standard Test Conditions

- $T_{ambient}$=25°C, DVDD-CORE=3.3V ±5%, AVDD=5.0V±5%
- 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms
- 10KΩ/50pF load; Test bench Characterization BW:10Hz~22kHz

Table 85. Analog Performance

Parameter	Min	Typ	Max	Units
Full-Scale Input Voltage				
All ADC (Gain=0dB)	-	1.3	-	Vrms
Full-Scale Output Voltage				
All DAC (Gain=0dB)	-	1.2	-	Vrms
Dynamic Range with 1kHz Tone, DR (A Weighted)				
ADC	-	90	-	dB FSA
DAC	-	97	-	dB FSA
Headphone Out @32Ω Load	-	97	-	dB FSA
Total Harmonic Distortion Plus Noise, THD+N				
ADC	-	-80	-	dB FS
DAC	-	-92	-	dB FS
Headphone Out @32Ω Load	-	-80	-	dB FS
Frequency Response				
ADC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	Hz
DAC (-3dB lower edge, -1dB higher edge)	10	-	0.454*Fs	Hz
Power Supply Rejection Ratio	-	-60	-	dB
Total Out-of-Band Noise (28.8kHz~100kHz)	-	-60	-	dB
Amplifier Gain Step				
ADC	-	1.5	-	dB
DAC	-	0.75	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
Input Impedance (Gain=0dB)	-	47	-	KΩ
Output Impedance				
Amplified Output	-	1	-	Ω
Non-Amplified Output	-	200	-	Ω
Digital Power Supply Current (Normal Operation) DVDD=3.3V, DVDD-IO=3.3V	-		35	mA
Digital Power Supply Current (Power Down Mode) DVDD=3.3V, DVDD-IO=3.3V	-		100	uA
Analog Power Supply Current (Normal Operation) AVDD1, AVDD2=5.0V	-		68	mA
Analog Power Supply Current (Power Down Mode) AVDD1, AVDD2=5.0V	-		<1	mA
VREFOUTx Output Voltage	0	2.50	3.75	V
VREFOUTx Output Current	-	5	-	mA

Note: FSA=Full-Scale with A-weighting filter. *FS=Full-Scale.*

9.4. Class-D Power Amplifier Performance

Table 86. Class-D Power Amplifier Performance

Parameter	Min	Typ	Max	Units
Maximum Output Peak Current @ BTL Mode	-	1.3	-	A
Maximum Output Power (THD+N=1%, 4Ω Load, PVDD=5V)	-	2.2	-	W
Maximum Output Power (THD+N=1%, 8Ω Load, PVDD=5V)	-	1.3	-	W
Power Efficiency η @ BTL Mode into 4ohm	-	80	-	%
Power Efficiency η @ BTL Mode into 4ohm with Filter	-	84	-	%
Power Efficiency η @ BTL Mode into 8ohm	-	88	-	%
Power Efficiency η @ BTL Mode into 8ohm with Filter	-	92	-	%
Full-Scale Output Voltage @ BTL Mode PCM/PWM Converter	-	+/-4.34	-	Vpeak
S/N (A weighted) @ BTL Mode PCM/PWM Converter	-	100	-	dB FSA
THD+N @ BTL Mode at test signal around 20Hz~22KHz PCM/PWM Converter	-	-60	-	dB FS
Frequency Response @ BTL Mode PCM/PWM Converter	20	-	20K	Hz
Total Quiescent Current (Iq)	-	1.25	-	nA
P-Type MOS Output Impendence (Rds)	-	150	-	mΩ
N-Type MOS Output Impendence (Rds)	-	250	-	mΩ
PWM Frequency	-	400K	-	Hz
Dead Time (Shoot)	-	0	-	nS
Modulation Index	-	0.8896	-	N/A
Minimum Pulse Width	-	150	-	nS
QFN-48 Package Thermal Characteristic, Θ_{JA}	-	32.4	-	°C/W
Output Voltage Noise(Vn) at Mute Condition	-	50	-	μV
Output Short Circuit Protection Limit	-	2.5	-	A
Class-D Output RMS Current, I_L (BTL 4Ω Load, PVDD = 5.0V, Full Power Output)	-	0.6	-	A
Class-D Output RMS Current, I_L (BTL 4Ω Load, PVDD = 5.0V, Power Down)	-	0	-	mA

10. Application Circuits

To get the best compatibility in hardware design and software driver, please contact Realtek to get the application circuit is appropriate for various system connections, any modification should be confirmed by Realtek's application engineers. Realtek may update the latest application circuits onto our web site (www.realtek.com) without modifying this datasheet

10.1. Filter Connection

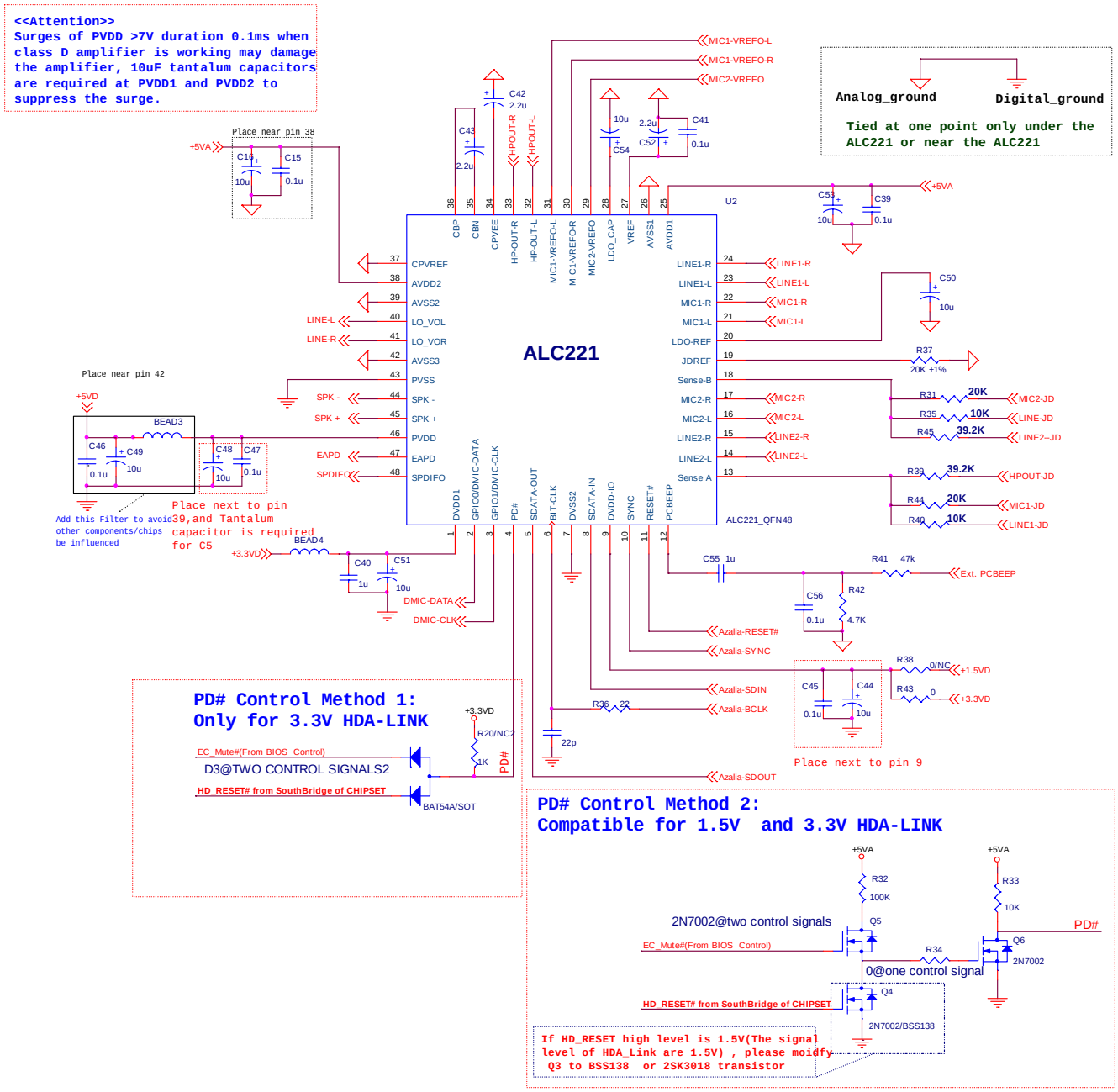


Figure 16. Filter Connection

10.2. Power and Jack Connection

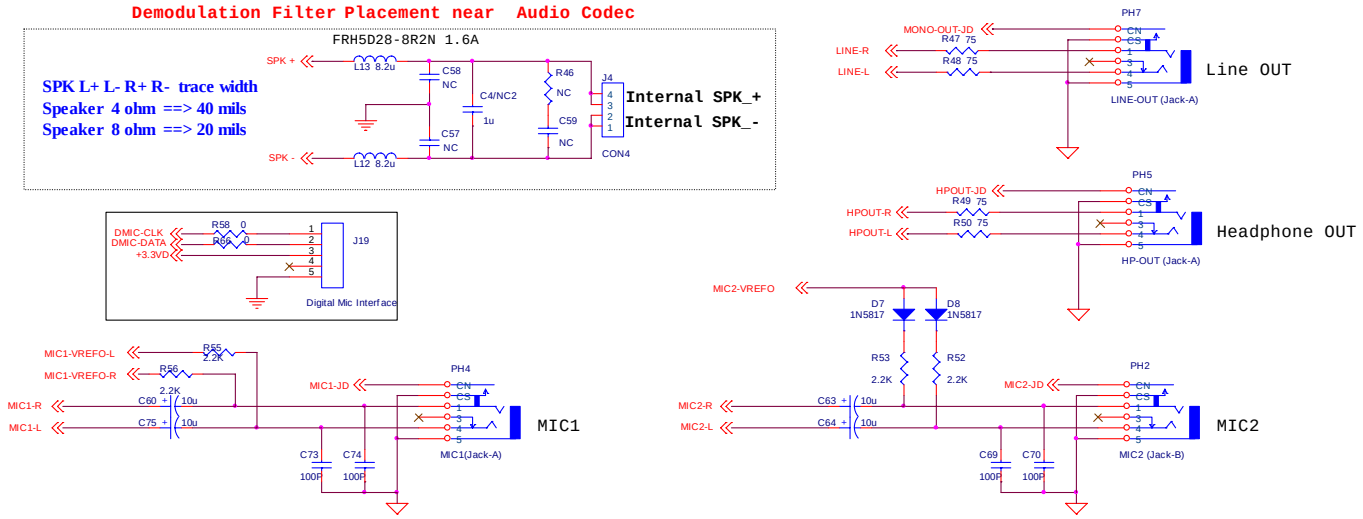


Figure 17. Power and Jack Connection

10.3. S/PDIF-OUT Connection

S/PDIF module option 1: Optical

S/PDIF module option 2: Coaxial

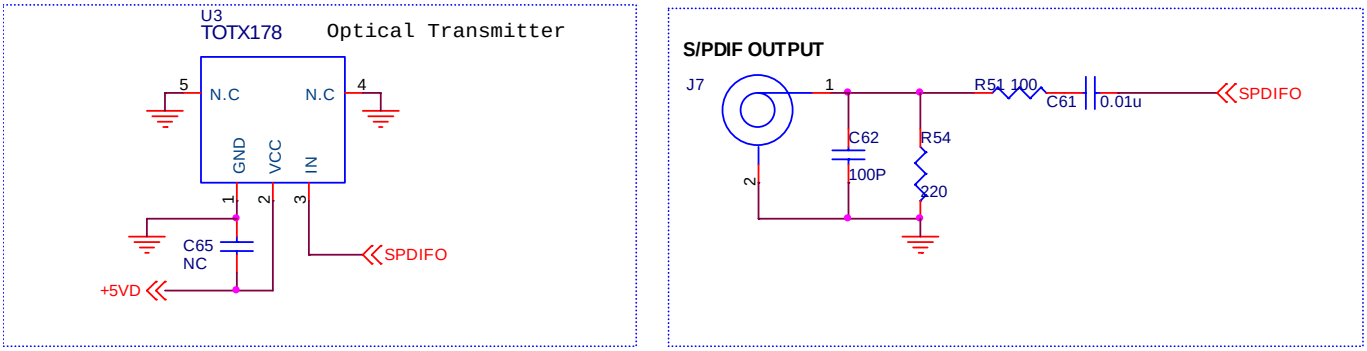
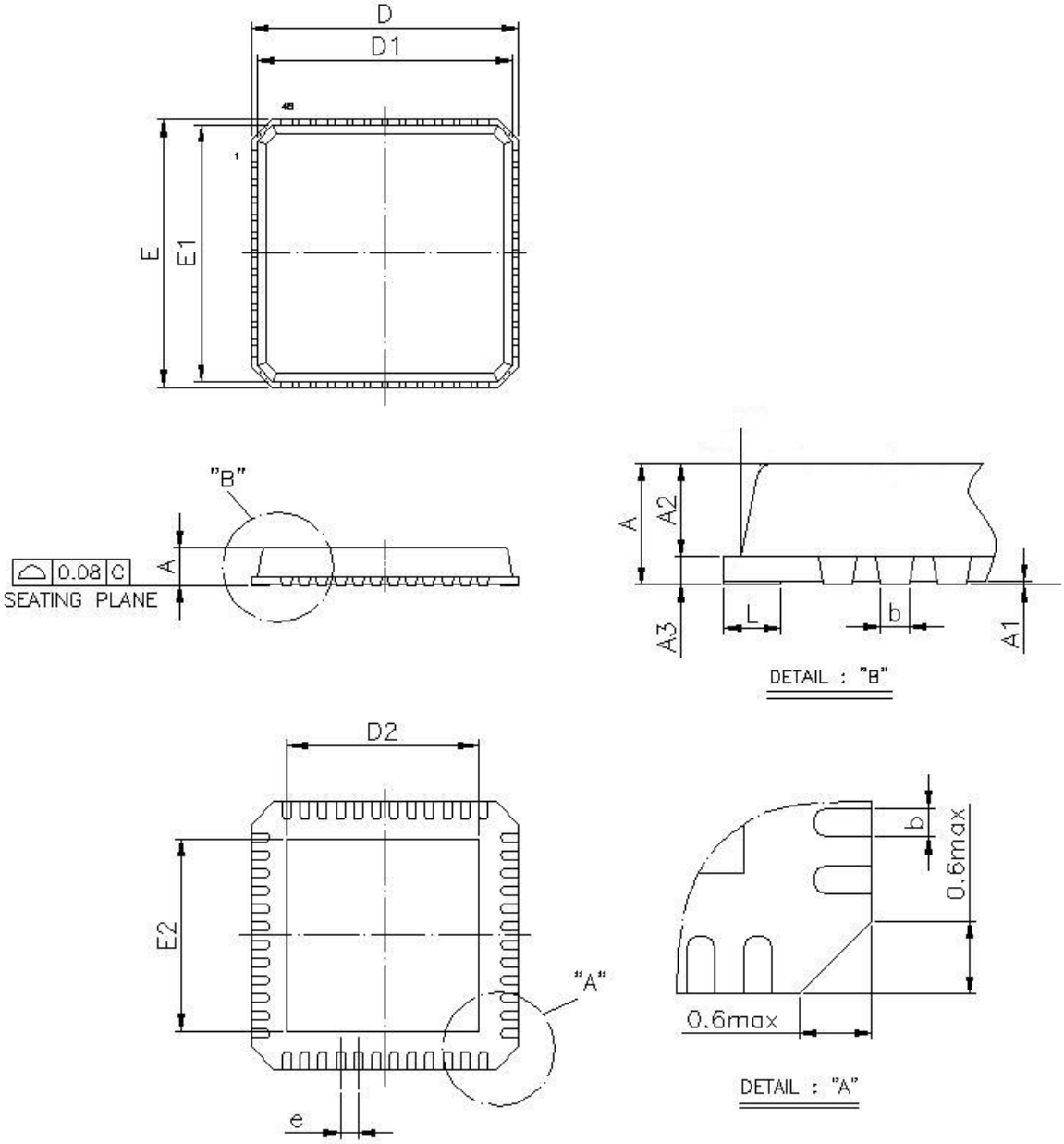


Figure 18. S/PDIF-OUT Connection

11. Mechanical Dimensions (QFN-48)

Plastic Quad Flat No-Lead Package 48 Leads 7x7mm^2 Outline



11.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.55	0.65	0.80	0.022	0.026	0.032
A_3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	7.00BSC			0.276BSC		
D_1/E_1	6.75BSC			0.266BSC		
D_2/E_2	5.20	5.45	5.70	0.205	0.215	0.225
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

12. Ordering Information

Table 87. Ordering Information

Part Number	Description	Status
ALC221-GR	QFN-48 'Green' Package	Production

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