University of California

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Schottky-collector Resonant Tunnel Diodes for Sub-Millimeter-Wave Applications

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of the requirements for the degree of
Doctor of Philisophy
in
Electrical and Computer Engineering
by
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Abstract

Schottky-collector Resonant Tunnel Diodes for
Submm-wave Applications

by
Madhukar Reddy

Submicron Schottky-collector resonant tunnel diodes (SRTDs) have been developed in the InGaAs/AlAs/InP material system. The Schottky-collector devices have much smaller series resistance than the conventional resonant tunnel diodes. The SRTDs have an estimated bandwidth of 2.2 THz, which is at least twice the bandwidth of the best conventional resonant tunnel diodes in this material system. Submm-wave slot antenna coupled SRTD oscillator arrays were also developed to demonstrate a useful application of these devices. These submm-wave oscillators incorporate on-wafer bias stabilization, a technique developed in this project to overcome the problems associated with DC bistability and parasitic low frequency oscillations of the RTD biasing circuit. The bias stabilization technique eliminates the limitations on the maximum RTD output power imposed by bias circuit stability requirements. A microwave RTD oscillator at 6.9 GHz was demonstrated employing the proposed bias stabilization technique. Extending bias stabilization of RTD oscillators to submm-wave frequencies demands a on-wafer Schottky-diode. This was realized through a graded band gap AlInAs Schottky-diode fabricated on the same wafer as the InGaAs SRTD. The submm-wave SRTD oscillator arrays were fabricated in a 8 mask layer integrated circuit (IC) process which achieves monolithic integration of 0.1 μm SRTDs, Schottky-diode bias stabilizers, slot antennas, MIM capacitors, and N++ resistors. SRTD oscillator arrays were tested with a quasi-optical measurement system. Arrays as large as 64 elements oscillated at frequencies as high as 650 GHz. A 16-element array produced at least 28 μW at 300 GHz.

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Chapter 1

Introduction

Solid-state signal sources at submm-wave frequencies (300-1500 GHz) are required for a variety of applications in wide band secure communication systems, high resolution radar and imaging systems for low-visibility environments, remote sensing of earth's atmosphere and study of ozone layer depletion chemistry [1], [2]. These frequencies are currently beyond the limits of the state of the art transistor bandwidths. The highest frequency transistor oscillators built to date are at 215 GHz [3]. Given their large bandwidths, resonant tunnel diodes (RTDs) can be utilized to build submm-wave signal sources for these various applications.

There has been a tremendous increase in interest in RTDs for various circuit applications since the pioneering work of Tsu and Esaki [4] who first proposed the resonant tunneling structures. RTDs are currently the widest bandwidth active semiconductor devices. Resonant tunneling through the double barrier structure in these devices gives rise to negative differential resistance (NDR) characteristics. Due to their large bandwidths, the NDR characteristics of RTDs have been useful for several high frequency applications including oscillators, pulse generators and trigger circuits. Trigger circuits employing fast switching AlAs/GaAs RTDs have been demonstrated upto 110 GHz [5]. Pulse generator circuits with 1.7 ps switching transition times have been demonstrated with InAs/AlSb RTDs [6]. Waveguide oscillators have been reported at 420 GHz with AlAs/GaAs [7] RTDs and at 712 GHz with InAs/AlSb [8] RTDs. A quasi-optical RTD waveguide oscillator operating at 220 GHz has been reported with InGaAs/AlAs/InP RTDs [9].

Given further improvements in RTD bandwidth, terahertz signal sources can be realized for the various applications mentioned above. In this project, a new

type of RTD, the Schottky-collector resonant tunneling diode (SRTD) is proposed and developed for mm-wave and submm-wave applications. By replacing the Ohmic contacted collector of a conventional RTD with a Schottky-collector, it is possible to apply simple device scaling laws to reduce the parasitic resistance in the device, thus obtaining large improvements in the RTD bandwidths. SRTDs with 0.1 μm wide Schottky-collectors similar to those used for T-gate HEMTS [10] were fabricated in InGaAs/AlAs/InP system. From the measured DC and microwave characteristics a maximum frequency of oscillation (f_{max}) of 2200 GHz was calculated for the InGaAs/AlAs/InP SRTDs. This is at least a $2:1$ improvement in the estimated bandwidth for any previously reported RTD in this material system [11]. This device technology can be now utilized for building several useful RTD circuits including oscillators, pulse generators and reflection amplifiers at submm-wave frequencies.

Despite the demonstration of high frequency RTD waveguide oscillators [7] [8], the achieved power levels are quite low, limiting their potential applications. The limited power levels are due to constraints imposed on maximum RTD area by bias circuit stability requirements to suppress DC bistability and low frequency parasitic bias circuit oscillations [12], [13]. DC bistability and low frequency parasitic bias circuit oscillations arise in RTD oscillators due to the presence of NDR characteristics from DC to f_{max}. In this project, SRTD oscillator arrays are developed. The oscillator arrays can potentially obtain significant power levels at submm-wave frequencies. A on-wafer bias stabilization technique is proposed that achieves bias circuit stability without any constraints on maximum RTD area. The limitations on maximum RTD output power are thus eliminated. The bias stabilization technique demands shunting the RTD by a low impedance bias stabilizer at a distance of $\lambda_{osc}/4$ from the RTD, where λ_{osc} is the wavelength corresponding to the design frequency of oscillation, f_{osc}.

To demonstrate the bias stabilization technique, a microwave oscillator was constructed. This consisted of a hybrid assembly of a RTD and a low impedance bias stabilizer. The problems of DC bistability and low frequency bias circuit oscillations associated with the RTD were eliminated in this hybrid oscillator. Oscillations were observed at 6.9 GHz. Extending the bias stabilization technique to submm-wave SRTD oscillators demands a on-wafer low impedance bias stabilizer. This was realized through a graded band gap AlInAs Schottky-diode fabricated on the same wafer as the 0.1 μm InGaAs SRTD.

Monolithic slot antenna coupled oscillator arrays employing the on-wafer bias stabilization technique were designed, fabricated and tested. The oscillator arrays were fabricated in a 8 mask layer integrated circuit (IC) process. The pro-

cess achieves monolithic integration of 0.1 μm InGaAs SRTDs, graded bandgap AlInAs Schottky-diode bias stabilizers, slot antennas, MIM capacitors and N++ resistors. The monolithic process enables an easy fabrication of various oscillator array designs in a single process run. The difficulties and the hardware expenses associated with submm-wave waveguide oscillators are eliminated by a monolithic IC process. The monolithic techniques developed in this project can be easily extended to large quasi-optical oscillator arrays for generating useful power levels at submm-wave frequencies.

The oscillator arrays were tested with a quasi-optical measurement system to determine the oscillation frequencies. The oscillator array, when mounted on Silicon lens, forms the quasi-optical oscillator. The Si lens forms a high Q resonant cavity that determines the exact oscillation frequency as well as the Q of the quasi-optical oscillator. Oscillations upto 200 GHz were detected by a Schottky-diode harmonic mixer. Oscillation frequencies were observed at 94, 109, and 196 GHz for different designs with this setup. Signals above 200 GHz were detected by a liquid Helium cooled Germanium bolometer. A scanning Fabry-Perot interferometer determined the oscillation frequency. With the bolometer and interferometer, oscillations were observed at 290, 300, 310, 470, 560, and 650 GHz. The highest oscillation frequency obtained is believed to be limited by layout considerations, e.g. the slot antenna length becomes comparable to the dimensions of the SRTDs, MIM capacitors and stabilizer diodes beyond 500 GHz. A calibrated power measurement with a thermo-acoustic detector indicated at least a 28 μW signal level for a 16-element, 300 GHz oscillator array. The signal levels from the higher frequency oscillators were found to be close to the threshold of the detector. Hence, calibrated power measurements could not be obtained. Despite this, the 650 GHz oscillation frequency of a 64-element monolithic oscillator array and the 28 μW output power of a 16-element array at $\approx$ 300 GHz represent record results for RTDs. The ultimate goal of the technology developed in this project is to demonstrate 1.0 to 1.5 THz oscillator arrays for applications in far infra-red heterodyne receivers.

This thesis will describe the various efforts that were undertaken to achieve the record results described above. The thesis is organized in a chronological order of the various developments. Chapter 2 will propose and describe the large improvements in bandwidths attained by submicron Schottky-collector RTDs. Chapter 3 will describe the fabrication and measurements of 0.1 μm SRTDs in the InGaAs material system. Chapter 4 will address the problems of DC bistability and parasitic bias circuit oscillations. Bias stabilization technique is proposed to overcome these problems without limiting RTD area or maximum output

power. Chapter 5 will describe the approach and circuit design efforts for submm-wave monolithic slot antenna coupled SRTD oscillator arrays. Chapter 6 will describe the oscillator array fabrication and testing. Chapter 7 will summarize the research effort and outline directions for future work to attain a 1.0 THz signal source.

Chapter 2

Schottky-Collector Resonant Tunneling Diodes

In this chapter, Schottky-collector resonant tunneling diodes (SRTDs) are described. These achieve at least a two-fold increase in the device bandwidth over the best reported Ohmic-collector RTDs. The improved bandwidth is obtained by a modification to the electron collection mechanism in the device, replacing the Ohmic-collector of a conventional RTD by a direct Schottky-contact to the space-charge region. The Schottky-collector electrode eliminates the parasitic series resistance associated with the collector electrode. Further reductions in series resistance are obtained by laterally scaling the Schottky-collector to submicron dimensions. These reductions in series resistance lead to an increased device bandwidth.

2.1 Theory of RTD Operation

First, the operation of an RTD is explained qualitatively with a simple model. The device cross-section and the corresponding conduction band diagram of an RTD is shown in figure 2.1. The RTD primarily consists of 1) an Emitter region, which is the source of electrons, 2) a Double-Barrier Structure consisting of a quantum-well sandwiched between two barriers of large bangap material, 3) a Space-Charge drift region and 4) a Collector region to collect the electrons tunneling through the double-barrier structure. The double-barrier structure is designed such that bound states are present in the quantum-well. Electrons from the emitter can tunnel through the barriers if their longitudinal energy is equal to the energy of the quasi-bound state in the quantum-well.

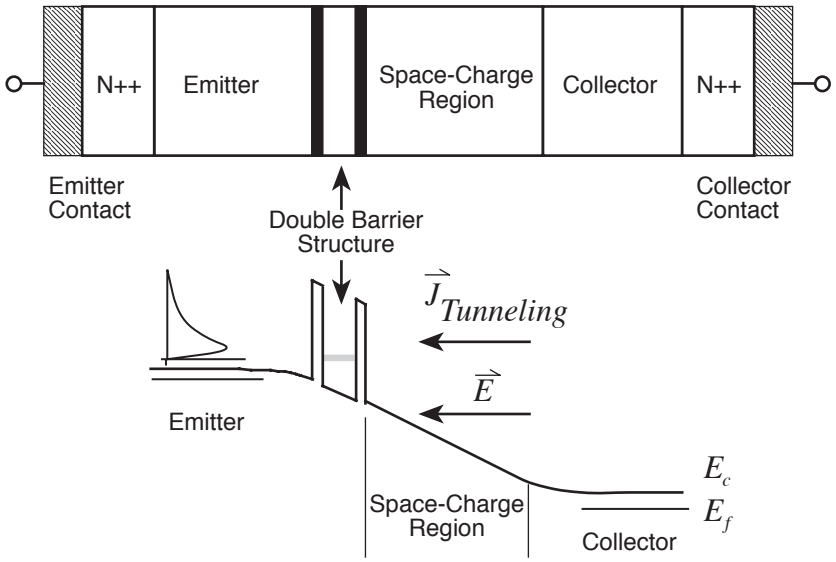

Figure 2.1: Cross-section of an RTD and the corresponding conduction band diagram under forward bias. The shaded region in the double-barrier structure represents the quasi-bound state in the quantum well. The energy distribution of the electrons in the emitter is also shown.

As the applied forward voltage (positive on the collector) to the RTD is increased, an electric field is created that causes electrons to move from the emitter towards the collector. At near-zero electrical bias, there is no current as the electrons from the emitter are stopped by the barriers. Therefore, the electrons from the emitter form an accumulation layer near the barrier. A small fraction of these electrons have an energy equal to the quasi-bound state energy in the quantum well. These electrons can tunnel through the double-barrier structure, giving rise to a current. With increasing bias, the energy level of the quasi-bound state in the quantum well is lowered with respect to the energy level of electrons in the emitter. A greater number of electrons can then participate in the tunneling process, giving rise to an increasing current with applied voltage. This continues until the electric field across the double-barrier structure is such that the energy level of the bound state coincides with the energy level at which the peak in the emitter electron distribution occurs. This corresponds to the peak in the I-V characteristics (figure 2.2). Beyond this voltage, a fewer number of electrons are available to tunnel and the current decreases for increasing voltage and negative differential resistance (NDR) is produced. Beyond a certain applied voltage, the barriers are lowered to the point that a substantial thermionic emission over the

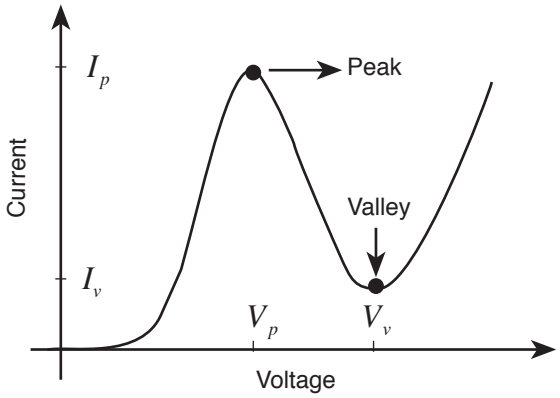

Figure 2.2: Typical I-V characteristics of an RTD. The peak current (I_p) occurs at the peak voltage (V_p) and the valley current (I_v) occurs at the valley voltage (V_v).

barriers occurs. The current then begins to rise with increased applied voltage.

These observed NDR characteristics are of primary importance for various RTD applications. The NDR region is characterized by the peak current and voltage (I_p, V_p) and the valley current and voltage (I_v, V_v). The current peak to valley ratio (PVR=I_p/I_v), and negative conductance ($G_n = |\partial I/\partial V|$) are other important parameters for specifying the NDR region. The slope of the I-V characteristics ($|\partial I/\partial V|$) is negative in the NDR region and is equal to $-G_n$.

The design of quantum-well, barriers, emitter and space charge layers directly affect the various NDR region parameters discussed above. For high frequency applications, very high peak current densities are required. This can be achieved in several ways. Reducing the thicknesses of the barriers leads to a broader quasi-bound state energy band. More electrons can participate in the tunneling process, leading to an increase in the peak current density. However, a broader quasi-bound state energy band also implies a reduced sharpness of the resonance, and so the PVR is reduced. Another way to increase the peak current density is to increase the emitter doping level, increasing the electron flux. This also increases the valley current and thus reduces the PVR. In both cases the valley current could be so large that the device may not exhibit significant NDR. This sometimes limits the minimum barrier thickness or the maximum emitter doping levels. The peak voltage (V_p) is determined by the thickness of the space-charge region and the quasi-bound state energy level. Reducing the quasi-bound state energy level or the thickness of the space-charge region leads to a lower V_p. Reducing the peak voltage reduces the power dissipation. Higher tunneling

currents can therefore be accommodated before device destruction.

A rigorous overview of the resonant tunneling process is found in [14] which arrives at the I-V characteristics quantitatively. Several theoretical models have been proposed to calculate the NDR characteristics of an RTD [14] [15]. Most of these models predict the peak current reasonably accurately but do not accurately predict the valley current. The excess valley current is explained through excess current mechanisms in the double-barrier structure. In one model [16], the valley current arises from scattering events in the presence of phonons in the accumulation layer. The electron is scattered to an energy level equal to quasi-bound state energy level, giving rise to a leakage current. Evidence of LO-phonon scattering in the valley current has been experimentally observed [17]. Another mechanism for valley current is tunneling through states in X-conduction band minima [18]. The X-band minima is smaller than the Γ-band minima in the barriers. An interaction between electrons and longitudinal optical phonons or acoustical phonons is also believed to cause an excess valley current.

RTD device design strategies vary depending on the application. For switching applications it is important to have a small valley current [19], to minimize the off-state power dissipation. Such large PVRs are usually achieved by increasing the barrier thicknesses. For high frequency oscillator applications, the available current $(I_p - I_v)$ in the NDR region is of primary importance, because this is directly related to the power available from the RTD oscillator. Increasing the available current is much more easily achieved by increasing the peak current rather than by reducing the valley current to zero because the peak current density is a much stronger function of the barrier thickness than the valley current density. It is much more advantageous to increase the peak current at the expense of the PVR. In fact, by using very thin barriers, the peak current increases more rapidly than the PVR degrades, so both G_n and the available current are increased and this is the adopted design strategy for high frequency oscillators.

2.2 Small Signal Model

In this section, a small signal model [7] (figure 2.3) is developed for an RTD biased in the NDR region. The model consists of a parasitic resistance R_s, a space-charge capacitance C, a negative resistance $-R_n$ (R_n by definition is positive) and a quantum-well inductance L_{qw}. L_{qw} is associated with the temporal delay due to the tunneling of electrons through the barriers and quantum-well .

The negative resistance term is $R_n = 1/G_n$, where G_n is the small signal

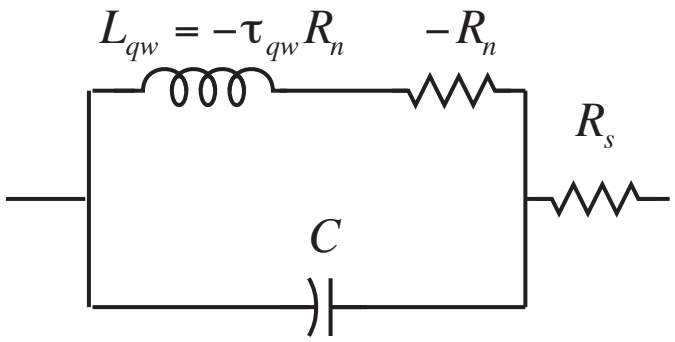

Figure 2.3: Small signal equivalent circuit model of an RTD biased in NDR region.

conductance calculated as $|\partial I/\partial V|$ at the bias voltage in the NDR region. G_n attains a peak value for a particular bias voltage in the NDR region. The space-charge capacitance C, is due to the depletion region between the collector and emitter. C is calculated assuming a parallel plate capacitor having the widths of the space-charge depletion layer, the double-barrier structure and the accumulation layer in the emitter. The quantum-well inductance L_{qw} [20], models the finite tunneling time required for electrons to tunnel through the barriers and quantum-well. L_{qw} is calculated as $-\tau_{qw}R_n$, where τ_{qw} is the quantum-well lifetime. τ_{qw} represents the time required for electrons to tunnel through the double-barrier structure. When the quantum-well inductance model was first proposed [20], a series of experiments were performed on RTDs intentionally designed to have very large values of L_{qw} and the measured results confirmed the validity of the model. $\tau_{qw} = 2\hbar/\Delta E$, where ΔE is the width in energy of the transmission probability for the double-barrier structure.

Finally, the resistance R_s, is composed of all the parasitic resistances in the RTD. The parasitic resistance R_s, consists of five main components as shown in the cross-section of an RTD (figure 2.4) of collector length L and width W. The five main components are the top Ohmic-collector resistance R_{top}, the Emitter layer resistance R_e, the spreading resistance R_{spr}, the Emitter N++ sheet resistance R_{bl}, and the Emitter N++ Ohmic contact resistance R_{oc}. These can be calculated in terms of the various material and geometry parameters. ρ_{cont} is the Ohmic contact resistance in $\Omega - \mu\text{m}^2$, while ρ_{top}, ρ_e and ρ_{bot} in $\Omega - \mu\text{m}$ are the resistivities of the Collector N++, the Emitter and the Emitter N++ layers respectively. T_{top}, T_e and T_{bot} are the thicknesses of the Collector N++, the Emitter and the Emitter N++ layers respectively.

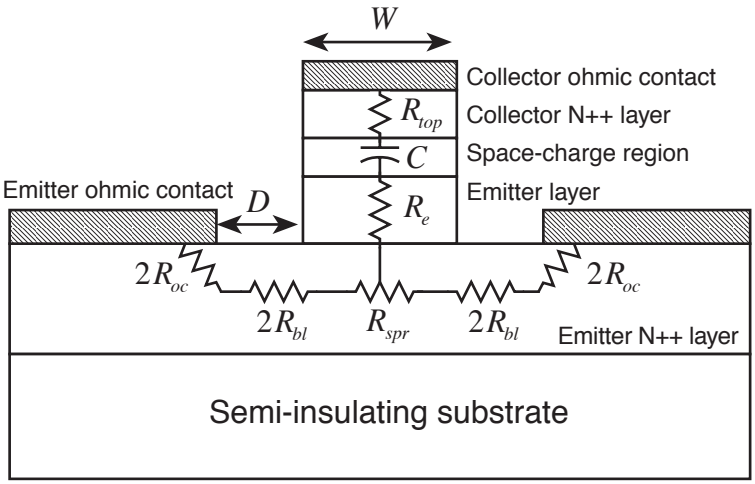

Figure 2.4: Cross-sectional diagram of an RTD showing the various components of the parasitics from the different regions of the device.

The top Ohmic-collector resistance (R_{top}) is associated with the Ohmic contact to the Collector N++ layer. It consists of the Ohmic contact resistance and the collector N++ layer resistance (equation 2.1). Both these are inversely proportional to the collector area. The thickness of the collector N++ layer (T_{top}) is usually small and its resistance is insignificant.

$$R_{top} = \frac{\rho_{cont}}{WL} + \frac{\rho_{top} T_{top}}{WL} \tag{2.1}$$

The vertical resistance through the Emitter layer (R_e) is associated with the current flow in this layer. It depends on the doping and the thickness of the Emitter layer (equation 2.2. The doping is primarily chosen to determine the electron flux incident upon the quantum-well. The emitter thickness T_e, can be reduced to make R_e small.

$$R_e = \frac{\rho_e T_e}{WL} \tag{2.2}$$

Current flow in the Emitter N++ layer is through a resistance R_{bl} (equation 2.3), while the resistance associated with the Emitter Ohmic contact metallization is R_{oc} (equation 2.4).

$$R_{bl} = \frac{1}{2}\frac{D}{L}\frac{\rho_{bot}}{T_{bot}} \tag{2.3}$$

$$R_{oc} = \frac{1}{2L}\sqrt{\rho_{cont}\frac{\rho_{bot}}{T_{bot}}} \tag{2.4}$$

There is also a spreading resistance that accounts for the current spreading in the Emitter N++ layer. When the collector width W is reduced to submicron dimensions, the current flow in this region is two-dimensional and the spreading resistance can be approximated as in equation 2.5.

$$R_{spr} = \frac{\rho_{bot}}{\pi L}\ln\left(\frac{T_{bot}}{W}\right) \tag{2.5}$$

The parasitic resistance R_s, is sum of the five contributions described above.

$$R_s = R_{top} + R_e + R_{bl} + R_{oc} + R_{spr} \tag{2.6}$$

The small signal model described above in detail neglects the space-charge transit time (τ_{tr}) delay. This can be accounted for by applying small-signal transit time theory with the electron injector consisting of the double-barrier structure and the accumulation layer in the emitter on the cathode side and the drift region consisting of the space-charge region on the anode side [21]. The electrons are assumed to be drifting through the space-charge region at a constant drift velocity. However, for the devices in this thesis, the space-charge transit times are extremely small. The space-charge drift region thickness (T_{sc}) is 350 Å . Electron velocities (v_b) in thin InGaAs layers are known to be $>4.0\times10^7$ cm/s. The space-charge transit time is therefore $\tau_{tr} = T_{sc}/2v_b$ =44 fs. This is small compared to other time delays in the device.

2.3 RTD Bandwidth

The bandwidth of an RTD is specified by the maximum frequency of oscillation, f_{max}. It is the highest frequency at which the RTD has extrinsic negative differential resistance. Equivalently, f_{max} is the highest frequency at which the admittance of the network of figure 2.3 has a negative real part. f_{max} can be solved for by setting the real part of the network's admittance to zero. Exact expressions for f_{max} can be derived by solving for the quadratic equation 2.7 in $\omega_{max}(= 2\pi f_{max})$. It should be noted that transit time τ_{tr} is neglected in these expressions for f_{max} under the assumption that the other time delays are larger than the transit time delay.

$$\omega_{max}^4\tau_{qw}^2C^2R_n^2R_s + \omega_{max}^2\left(C^2R_n^2R_s + 2\tau_{qw}CR_nR_s\right) - R_n + R_s = 0 \tag{2.7}$$

While equation 2.7 is exact, it is not easily interpreted. To more clearly understand, the device bandwidth limits, the exact expression (equation 2.7) is approximated to simpler expressions in the limit of $R_s \ll R_n$. When $\tau_{qw} \ll C(R_sR_n)^{-1/2}$, f_{max} (equation 2.8) is inversely proportional to the simple geometric mean of the time constants R_sC and R_nC.

$$f_{max} \approx (2\pi)^{-1} (R_nC)^{-1/2} (R_sC)^{-1/2} \tag{2.8}$$

In the other limit, $\tau_{qw} \gg C(R_sR_n)^{-1/2}$, quantum well lifetime τ_{qw} becomes the dominant time constant. In this limit, f_{max} (equation 2.9) is inversely proportional to the geometric mean of the time constants τ_{qw} and $C(R_sR_n)^{1/2}$.

$$f_{max} \approx (2\pi)^{-1} (\tau_{qw})^{-1/2} (R_nC)^{-1/4} (R_sC)^{-1/4} \tag{2.9}$$

From these expressions, it is clear that f_{max} is determined by the time constants R_sC, R_nC and τ_{qw} and large improvements in f_{max} are obtained by reducing each of these terms. The R_nC time constant is related to the current density (equation 2.10),

$$\frac{1}{R_nC} = \frac{1}{\epsilon}\frac{\partial J}{\partial E} \tag{2.10}$$

where ϵ is the dielectric constant of the material, J is the operating current density and E is the electric field across the double-barrier structure.

Increasing the space-charge layer thickness to reduce C also increases R_n, and the product R_nC does not change. Instead, in order to reduce the time constant R_nC, the operating current density should be maximized. This is achieved by using thin barriers.

The time constant τ_{qw} is also dependent on the thickness of the barriers and can be reduced by using thin barriers [14]. Therefore, thin barriers result in both small τ_{qw} and a high current density which reduces R_nC. Reduction in τ_{qw} and R_nC through the use of very thin barriers is ultimately limited by degradation in current peak to valley ratio (PVR) and by high device power dissipation. With a modification that will be proposed to the existing conventional RTD (next section), the third time constant R_sC is reduced to a very large extent. Reducing this time constant leads to a large improvement in RTD bandwidth.

2.4 Schottky-collector RTD

The Schottky-collector RTD obtains significant improvements in bandwidth by reducing the time constant R_sC, through a dramatic reduction in the parasitic

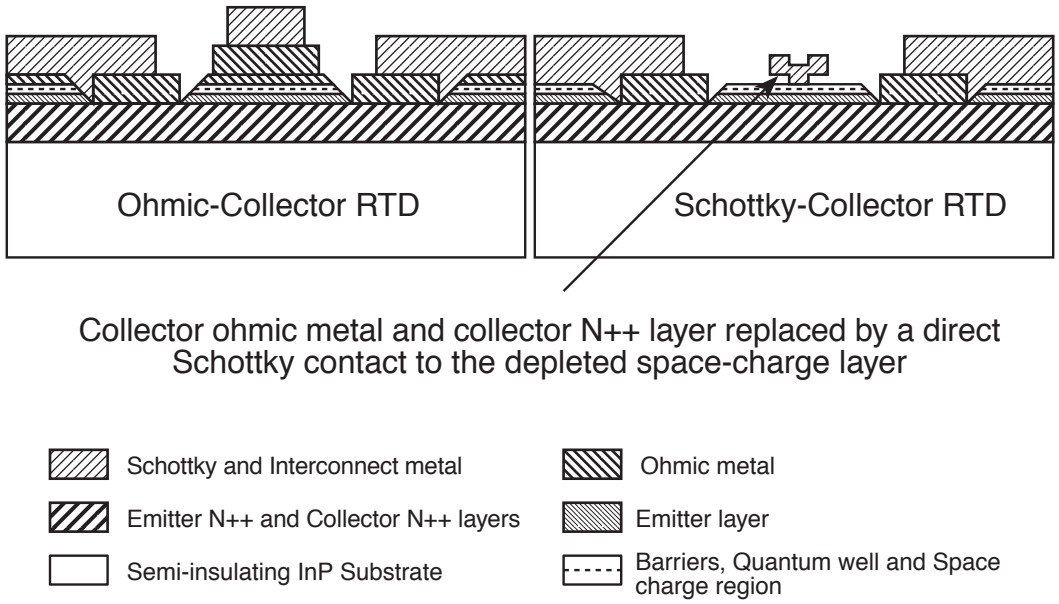

Figure 2.5: Cross-sectional views of a conventional Ohmic-collector RTD and a Schottky-collector RTD. In a SRTD, the Ohmic-collector consisting of the top Ohmic contact and the collector N++ layer is replaced by a direct Schottky-contact to the space-charge region.

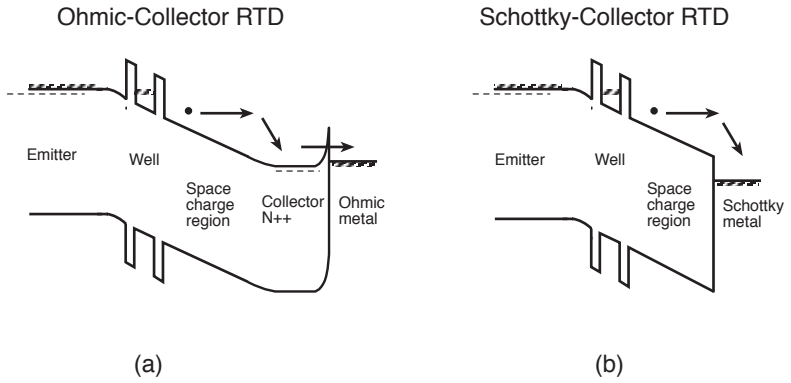

Figure 2.6: Band diagrams of a conventional RTD and a SRTD showing that the only change in a SRTD is in the collection mechanism for the electrons.

resistance R_s. In a conventional Ohmic-collector RTD, a parasitic resistance is associated with the top Ohmic-collector (equation 2.1). In a Schottky-collector RTD, this top Ohmic-collector is replaced by a direct Schottky-contact to the space-charge region as shown in figure 2.5. This directly eliminates the parasitic resistance associated with the top Ohmic-collector. The modification introduced in a SRTD does not change the resonant tunneling physics of the device and only effects the collection mechanism as shown in figure 2.6. In a conventional Ohmic-collector RTD, the electrons after traversing through the space-charge region thermalize in the collector N++ layer and are eventually collected by the Ohmic-collector contact metallization. In a Schottky-collector RTD, the electrons after traversing through the space-charge region simply drop over the Schottky-barrier at the metal-semiconductor interface and are collected by the Schottky-metal. The potential difference across the Schottky interface is simply the difference between the work function of the metal and the electron affinity of the semiconductor. This is independent of the current and there is therefore no associated incremental resistance.

Quantum mechanical reflection of electrons at the metal-semiconductor interface would result in increased electron density in the space-charge layer, e.g. an increased electron transit time. However, the reflection probability for typical electron energies is very small.

Further reduction in R_s is obtained by applying simple device scaling laws to reduce periphery dependent resistances in the emitter N++ layer and the emitter Ohmic metallization by several fold. Figure 2.4 shows the various terms contributing to the parasitic resistance R_s. As can be seen from the geometry de-

pendencies, R_{bl}, R_{oc}, and R_{spr} (equations 2.3, 2.4, 2.5) are inversely proportional to L. By reducing the width W of the device to deep submicron dimensions, while increasing the length L to maintain a constant device area, the periphery-to-area ratio is increased. The periphery dependent resistance terms (R_{bl}, R_{oc} and R_{spr}) are driven towards zero. Thus, the overall parasitic resistance R_s is reduced dramatically in a submicron Schottky-collector RTD. The R_sC time constant is thus reduced, leading to a large improvement in RTD bandwidth.

The improvement in bandwidth with scaling for a submicron Schottky-collector RTD is clearly illustrated in figure 2.7. The figure uses identical parameters R_n, C, ρ_{cont}, ρ_{bot}, T_{bot} and τ_{qw} for the 2 devices, with typical values characteristic of the InGaAs material system. The plot shows the significant improvements in bandwidth obtained by replacing the top Ohmic-collector by a direct submicron Schottky-collector to the space-charge region. Even at large collector widths ($W \approx 1.0$ μm) an improvement in bandwidth is obtained in a SRTD because of the elimination of the top Ohmic contact resistance. Further, as the Schottky-collector width is reduced to submicron dimensions the periphery dependent bottom Ohmic contact resistances are driven to zero, leading to improvement in bandwidth. For the conventional Ohmic-contacted device, there is little improvement in the f_{max}, as W is reduced below about 1.0 μm because the area dependent top Ohmic-contact resistance does not reduce.

Submicron scaling itself can introduce parasitics. For submicron Schottky collectors, there will be an additional resistance and inductance along the collector finger, analogous to the gate resistance and inductance of submicron FET or HEMT [22]. The measured end to end dc resistance of a submicron gate ($\rho_{gate}L/A_{cross}$) is used to obtain an estimate for the gate resistance (equation 2.11) for a distributed model [23], where ρ_{gate} is the gate metal resistivity in $\Omega - \mu m$ and A_{cross} is the cross-sectional area of the gate.

The inductance is also estimated by a distributed model , where the submicron gate is assumed as a CPW transmission line between the two Ohmic pads [24]. An approximate value for gate inductance is given by equation 2.12, which assumes a typical value of 1.0 pH/μm inductance per unit length for a 0.1 μm gate.

$$R_{gate} = \frac{\rho_{gate}}{A_{cross}}\frac{L}{3} \tag{2.11}$$

$$L_{gate} \approx (1.0 \text{ pH}/\mu\text{m})L \tag{2.12}$$

A T-gate structure is necessary to increase the cross-sectional area of the collector finger thereby minimizing the parasitic gate resistance [25]. Without the

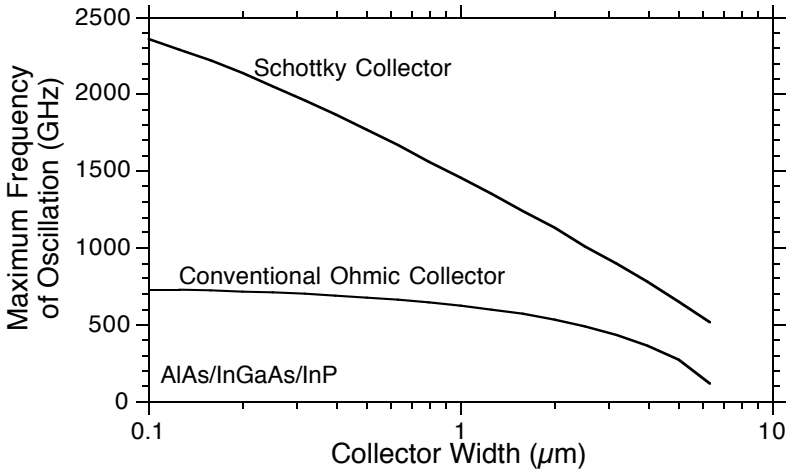

Figure 2.7: Dependence of f_{max} on collector contact width for a conventional Ohmic-collector RTD and a Schottky-collector RTD. Material parameters of InGaAs were assumed for estimating f_{max}.

T-gate, the gate resistance could take away all the benefits obtained by scaling the SRTD to submicron dimensions. Even with the T-gate, setting $R_{gate} = R_s$ determines the maximum acceptable stripe length.

The space-charge capacitance C is fixed by the width of the undoped region between the Schottky collector and the emitter layer. $C = \epsilon WL/d$, where d is the sum of the thicknesses of the space-charge region, the double-barrier quantum well and the accumulation layer in the emitter. When d becomes an appreciable fraction of W, there will be significant lateral extent of the electric field under the Schottky contact, and it becomes more appropriate to compute C in terms of an effective contact width, $W_{eff} = W + 2d$. Therefore, at deep submicron dimensions the effective collector width is slightly larger than the actual contact width.

For deep submicron Schottky-collector RTDs, R_s is extremely small. The effect of τ_{qw} on f_{max} is then dramatic. For SRTDs with a 0.1 μm collector width, there is almost a $2:1$ reduction in f_{max} when the effect of τ_{qw} is included in the device model. This implies that the external parasitics of the device have been reduced to such a large extent that the bandwidth of the device is now substantially limited by intrinsic transport properties of the device. Therefore,

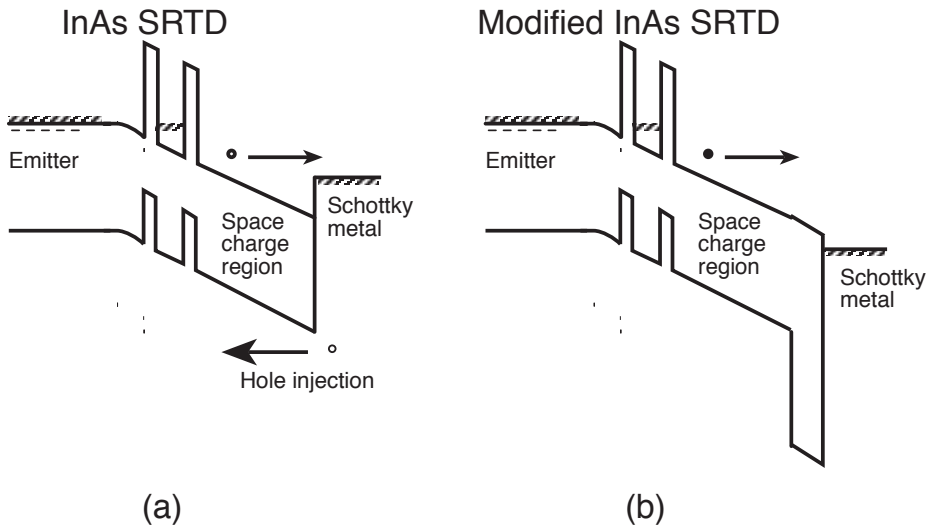

Figure 2.8: (a) Band diagram of InAs SRTD showing possible hole injection current, and (b) band diagram of modified InAs SRTD that utilizes a larger band gap material at the surface to suppress hole injection currents.

a submicron SRTD can achieve the best possible bandwidth for a given material system by reducing the external device parasitics.

2.5 InGaAs Material System

As seen in the previous section, submicron SRTDs can achieve large improvements in device bandwidths. Initially, submicron SRTDs were fabricated in the GaAs material system, because of its mature epitaxial growth and mature fabrication technology. 0.1 μm GaAs SRTDs [26] were fabricated. These had an estimated bandwidth of 900 GHz, a two-fold improvement over the best Ohmic-contacted RTDs fabricated in this material system [7]. Bandwidths above 900 GHz could not be readily obtained, because of the high Ohmic contact resistances and low tunneling current densities associated with GaAs/AlAs devices. Since, the overall goals of the project demand RTD bandwidths in excess of 2.0 THz, efforts were undertaken to find the most suitable material system.

The best RTD bandwidths were reported for InAs/AlSb RTDs [8], with estimated f_{max} over 1.24 THz. The high f_{max} is attributed to higher current densities, higher carrier velocities (shorter transit times), lower Ohmic contact resistance in InAs material system. Due to a very low series resistance in a

submicron SRTD, the advantage of low Ohmic contact resistance to InAs is of less importance. The primary advantages are obtained from the higher tunneling current densities and shorter transit times in a InAs SRTD. However, a difficulty exists with a Schottky-collector on undoped InAs surface for a InAs SRTD (figure 2.8(a)). Due to the lower valence band offset at the surface, there could be sufficient hole injection from the Schottky-metal into the semiconductor. The electric field causes these injected holes to flow from the metal towards the barriers in opposite direction as the electrons. Since the InAs/AlSb band offsets are staggered type II at the Γ point there are no barriers for holes in the valence band. These holes could simply cross over to the emitter leading to a large hole current that swamps out the NDR characteristics of the electron current. Therefore, a different material (like AlSb) with a larger hole barrier at the Schottky surface is necessary (figure 2.8(b)). With a larger hole barrier at the surface, hole injection from the Schottky-metal into the semiconductor is suppressed. The growth and fabrication technologies in this material system are immature compared to InGaAs or GaAs material system. Even though best SRTD bandwidths could be potentially obtained in this material system, a sufficient amount of work is required at material and process development which would hamper the progress towards the ultimate project goal of oscillator fabrication. Hence, the InAs/AlSb SRTD system was not chosen. The next best RTD material system is InGaAs/AlAs/InP. Due to its mature fabrication and growth technologies, InGaAs material system was investigated for SRTDs.

Conventional RTDs fabricated in InGaAs/AlAs/InP [11] material system have been reported with bandwidths in the vicinity of 1.0 THz. This was attributed to the superior material parameters of this system. The larger barrier height and lower electron effective mass in InGaAs/AlAs RTDs lead to significantly higher PVR than the best GaAs/AlAs RTDs for the same current densities [11]. This implies that the NDR characteristics can be observed at much higher current densities than in GaAs RTDs. A higher peak negative conductance per unit area can be obtained, which is a critical requirement for improving the f_{max} of RTDs. Peak current densities as high as $5{\times}10^5$A/cm^2 have been reported for InGaAs/AlAs/InP RTDs [27]. Chow et. al. [15] conducted an extensive study of InGaAs RTDs for high speed switching and estimated 1.6 ps risetimes with InGaAs RTDs. Additional benefits of the InGaAs system over GaAs/AlAs system are the lower Schottky-barrier height, lower effective electron mass and a greater solid-state solubility for n-type dopants. The tunneling current (J_{ohm}) due to electron flow from the Emitter N++ layer to the Emitter Ohmic contact metallization is proportional to $e^{-K\phi_b\sqrt{m_{eff}/N}}$ [28], where K is a constant, ϕ_b

is the Schottky-barrier height, m_{eff} is the electron effective mass and N is the doping in the N++ layer. The tunneling current is therefore larger for InGaAs than GaAs, leading to lower Ohmic contact resistance in InGaAs. Besides, the higher doping level of N++ layer gives a lower sheet resistance in InGaAs system. These factors lead to a much lower series resistance for the InGaAs RTDs. InGaAs RTDs with f_{max} over 1.0 THz have been reported [11]. With the SRTD, further improvements in bandwidth can be achieved in this material system. Therefore, efforts were undertaken to fabricate submicron InGaAs SRTDs with an aim of obtaining RTD bandwidths over 2.0 THz.

Chapter 3

Submicron InGaAs SRTDs

This chapter will describe in detail the important stages of development of submicron SRTDs in the InGaAs material system. The effort to develop these very high f_{max} InGaAs SRTDs started with the material characterization. This was followed by the fabrication of 0.1 μm InGaAs SRTDs. A sophisticated electron-beam lithography process was developed at Jet Propulsion Laboratories (JPL) for defining the submicron Schottky-collector. From their measured DC and microwave characteristics, the 0.1 μm InGaAs SRTDs had an estimated f_{max} of 2.2 THz. This f_{max} is twice that reported for the best conventional Ohmic-collector InGaAs/AlAs RTDs and 1.8 : 1 higher than the highest f_{max} reported for any RTD.

3.1 Material Characterization

InGaAs material was grown by molecular beam epitaxy (MBE) by Dr. Mark Mondry at UCSB. The goal of material characterization was to obtain growth parameters and layer structure design for fabricating very high f_{max} InGaAs SRTDs. Since these SRTDs were to be eventually utilized for building monolithic submm-wave circuits, reproducibility and uniformity of device characteristics across a 2-inch wafer was a primary consideration. The MBE layer structure was designed through iterative cycles of growth and simple characterization of material by fabricating and measuring DC characteristics of large area SRTDs. A simple 3 mask layer process for fabrication of large-area SRTDs was designed for the purpose of material characterization. Growth parameters were frozen after the desired DC characteristics were obtained.

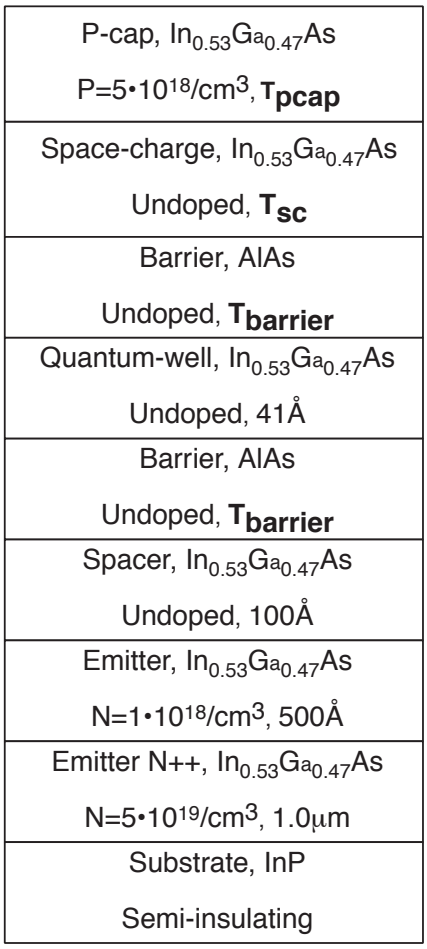

Figure 3.1: MBE layer structure for fabrication of InGaAs SRTDs.

3.1.1 Layer Structure Design

The layer structure design (figure 3.1) started with the designs developed by Chow et. al. [15]. For the SRTD, modifications to their layer structure were necessary. In SRTDs, the collector electrode is on the top. This implies that the electrons must tunnel towards the wafer surface, hence the conventional RTD layer structure must be turned upside down. This requirement introduces potential problems.

Upward movement of Si dopants has been observed during the growth of inverted AlInAs-InGaAs modulation doped structures [29]. In the SRTD growth, a similar phenomenon would cause movement of Si dopants from the emitter layer

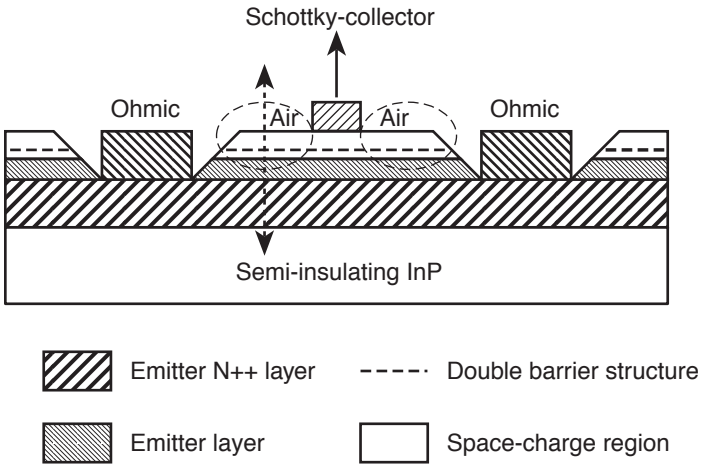

Figure 3.2: Cross-section of an SRTD showing regions surrounding the Schottky-collector in a dotted circle. The depleted semiconductor layers in these regions have sufficient free electron charge density to cause parasitic leakage paths between the Schottky-collector and the adjacent Ohmic pads.

into the double-barrier structure. If the double-barrier structure were heavily doped, applied fields would not deplete it, and the RTD would not function as desired. To prevent this, a 100 Å spacer layer was therefore placed between the emitter and the double-barrier structure. Further, the growth temperature of this spacer layer was reduced to 320 °C to suppress Si dopant movement.

For obtaining high f_{max}, the critical material requirement is obtaining the highest possible peak current density. This is achieved through thinning the barriers to a point limited by either serious degradations of the PVR or device power densities sufficient for device burnout. Barrier thicknesses of 5 and 6 monolayers (ML) were investigated. Chow et. al. [15] had observed that these barrier thicknesses yield tunneling current densities in the vicinity of 3×10^5 A/cm^2 to 5×10^5 A/cm^2.

The Ohmic collector layers used in Chow's [15] devices were removed as there is no requirement for a collector Ohmic contact in a SRTD. The Schottky-contact is made directly to the space-charge region. Simply eliminating the top collector N++ layer (as in GaAs SRTDs [26]) is not sufficient. A fully depleted P-cap layer is also required. The P-cap layer increases the Schottky-barrier height at the air-semiconductor interface. This modification is necessary due to the low bandgap (0.7 eV) of InGaAs and also the low surface pinning (0.2 eV from conduction band) of the Fermi-level at the air- semiconductor interface [30].

In the regions surrounding the Schottky collector contact (figure 3.2), where the semiconductor is exposed to air, free electrons can exist within the semiconductor space-charge region. If present, these electrons would provide leakage paths between the Schottky-collector and the adjacent Ohmic contacts. The peak to valley ratio would thereby be degraded. Because, these leakage paths are dependent upon RTD periphery, and not on the RTD junction area, they will become very significant as the Schottky-collector is scaled to deep submicron geometries. This leakage problem is not significant in GaAs/AlAs SRTDs. In GaAs/AlAs, the surface pinning of the Fermi-level (0.7 eV from the conduction band) and the wide bandgap (1.42 eV) lead to insignificant free electron charge concentrations.

To suppress the edge leakage effect in InGaAs/AlAs SRTDs, the barrier at the air-semiconductor interface was increased by a fully-depleted P-cap layer. The increase in barrier height is approximately $(qN_aT_{pcap}^2)/(2\epsilon)$, where N_a is the P- doping in the P-cap layer, T_{pcap} is its thickness, and ϵ is the dielectric constant of the semi-conductor. The effect of the P-cap layer is clearly illustrated by the band diagrams (figures 3.3, 3.4) drawn across the SRTD layers in the regions surrounding the Schottky-collector (shown by the double arrow dotted line in figure 3.2). The P-cap layer increases the barrier height near the surface thereby increasing the separation between the Fermi-level and the conduction band in the space-charge region as when compared to the band diagram without a P-cap layer. This increased separation implies a lower electron charge concentration in the space-charge region which depends exponentially upon the separation between the Fermi-level and the conduction band as shown in figure 3.5.

The barrier height for electrons increases with increased P-cap doping or thickness. Increasing the barrier height has the effect of reducing the free electron charge density in the region between double-barrier structure and the semiconductor surface. However, the doping or thickness cannot be increased forever as this leads to increase in free hole charge (figure 3.6) in the space-charge region which is undesirable as well. Therefore, the doping and thickness of the P-cap layer were optimized to obtain a minimum total free electron and hole charge concentration in the region between the double barrier structure and the semiconductor surface (figure 3.7). The optimized layer structure consists of a 100 Å thick P-cap layer, Be-doped to $5\times10^{18}/\text{cm}^3$.

The total free charge (electrons and holes) concentration (in units of $/\text{cm}^2$) can be obtained by integrating the total free charge concentration (in units of $/\text{cm}^3$ in figure 3.7) across the space-charge region between the barriers and the semiconductor surface. The total free charge concentration in the space-charge

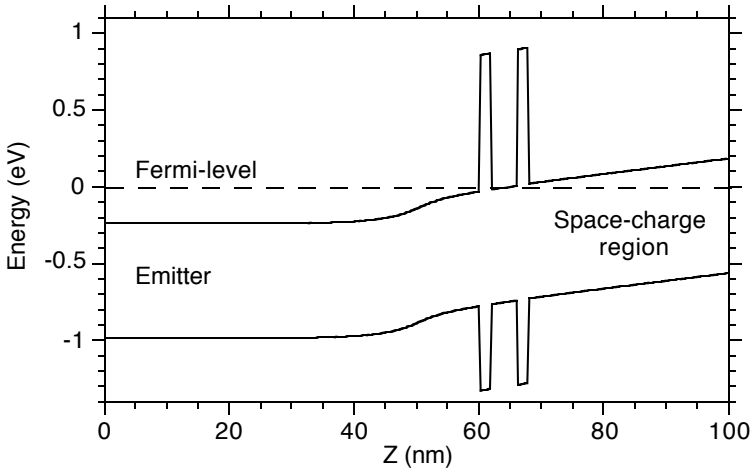

Figure 3.3: Band diagram of SRTD layers without a P-cap in regions surrounding the Schottky-collector.

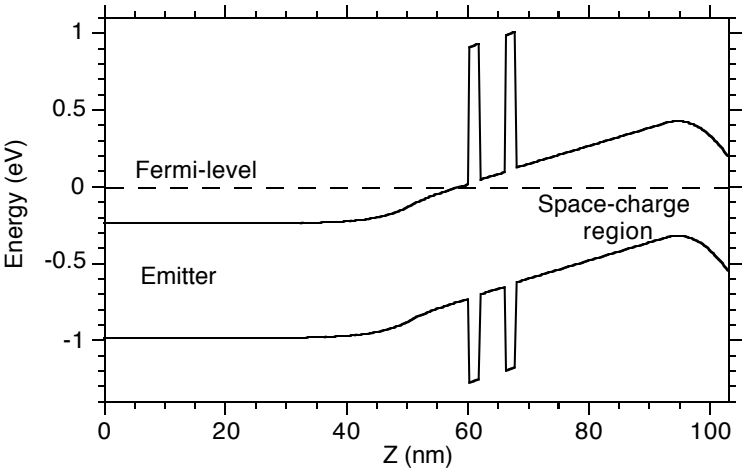

Figure 3.4: Band diagram of SRTD layers with a P-cap in regions surrounding the Schottky-collector.

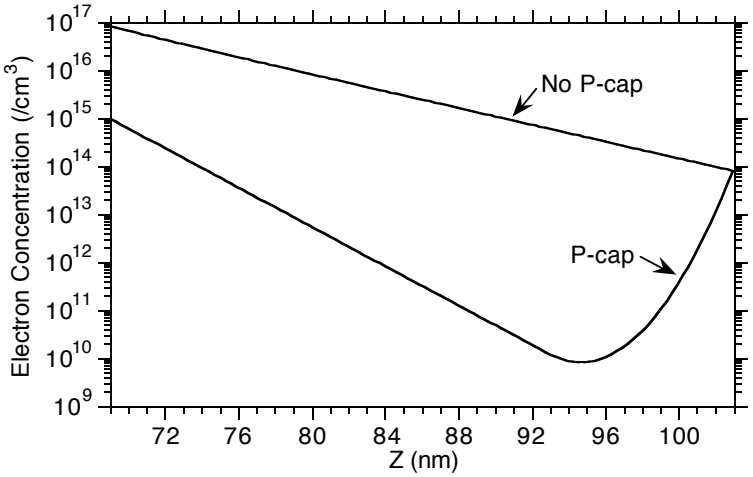

Figure 3.5: Electron concentration in the space-charge region with and without the P-cap layer.

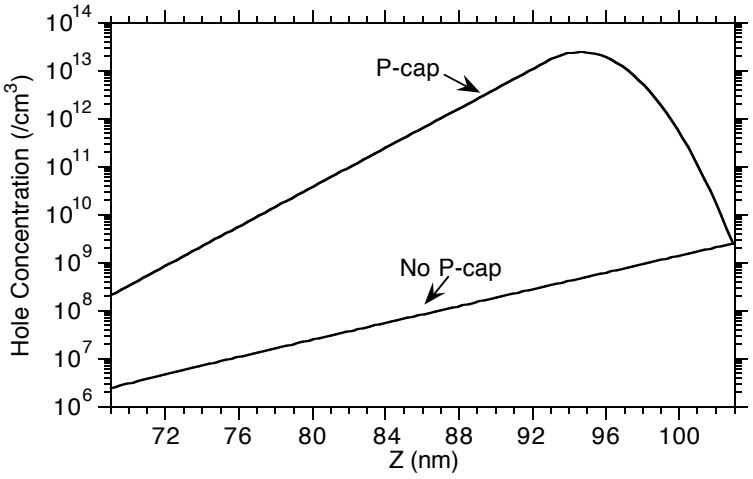

Figure 3.6: Hole concentration in the space-charge region with and without the P-cap layer.

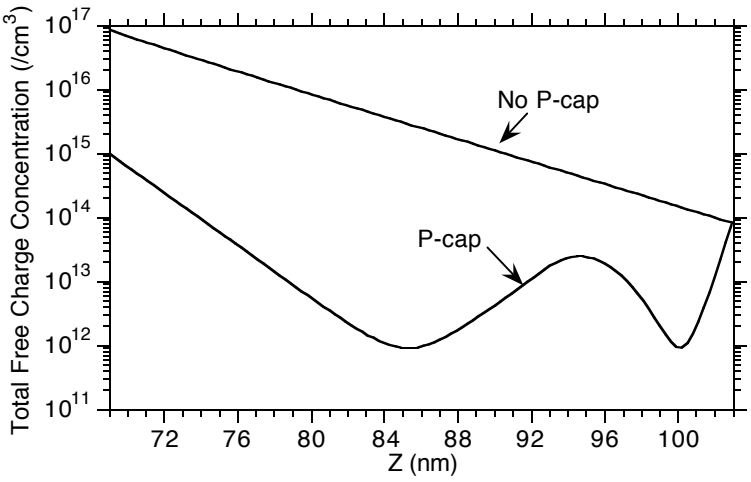

Figure 3.7: Total free charge concentration in the space-charge region with and without the P-cap layer.

region was calculated as $10^{11}/\text{cm}^2$ without the P-cap layer. This total free charge concentration is reduced to $10^9/\text{cm}^2$ with the fully depleted P-cap layer. This indicates that the periphery dependent leakage currents would be at least two orders of magnitude lower with the P-cap layer.

A disadvantage of the addition of the P-cap layer is the increase in applied voltage required to achieve resonance condition across the double-barrier structure. This is illustrated in figure 3.8, where the conduction band diagram at resonance is shown for both cases, with and without the P-cap layer. For the same electric field across the double-barrier structure, the applied voltage is roughly $(qN_aT_{pcap}^2)/(2\epsilon)$ larger for the case with the P-cap layer.

3.1.2 Material Growth

Molecular beam epitaxial growth of the layer structure (figure 3.1) starts with the nucleation of a 1.0 μm, $10^{19}/\text{cm}^3$ Si-doped $In_{0.53}Ga_{0.47}As$ Emitter N++ layer to the [100] InP substrate at 540 °C substrate temperature. This is followed by a 500 Å , $10^{18}/\text{cm}^3$ Si-doped $In_{0.53}Ga_{0.47}As$ Emitter layer and 100 Å , undoped $In_{0.53}Ga_{0.47}As$ Spacer layer. The top 100 Å of the Emitter layer and the entire Spacer layer are grown at 320 °C substrate temperature to minimize the

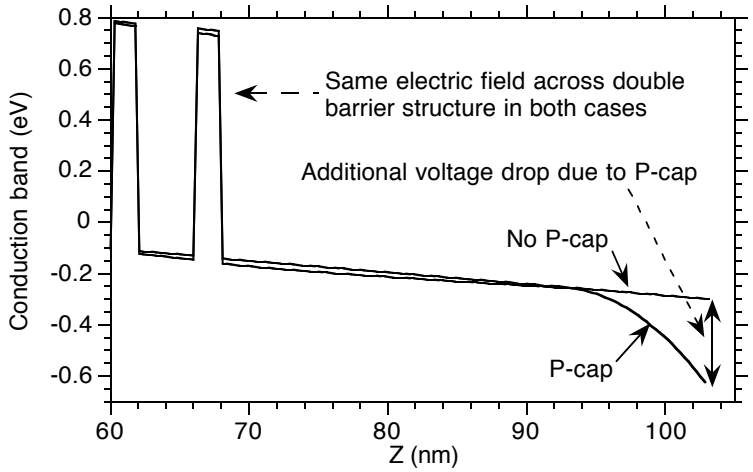

Figure 3.8: Conduction band diagram of SRTD under forward bias with and without the P- cap layer. An additional voltage is required for the P-cap layer for the condition to obtain the same electric field across the double-barrier structure.

out diffusion of Si dopants into the barriers and the quantum-well. Growth interruptions were used before and after the low temperature growth to stabilize the substrate temperature. The Double-Barrier structure grown at 510 °C consists of either 14 Å (5ML) or 17 Å (6ML) undoped AlAs barriers and a 41 Å, undoped $In_{0.53}Ga_{0.47}As$ quantum-well. The Space-Charge region also grown at 510 °C consists of a undoped $In_{0.53}Ga_{0.47}As$ layer of thickness T_{sc} and a 100 Å, $5\times10^{18}/cm^3$ Be-doped $In_{0.53}Ga_{0.47}As$ P-cap layer. The uniformity of the barrier thicknesses is critical for obtaining uniform peak current density across the wafer. Since the ultimate goal of the project was to build SRTD circuits, efforts were also undertaken to obtain growth parameters that would give a uniform barrier thickness and hence a uniform peak current density across a 2-inch wafer. This was achieved by increasing the rotation speed of the MBE wafer holder from 15 rpm to 25 rpm during the growth of the barriers. Details of the MBE growth are given in Appendix A.

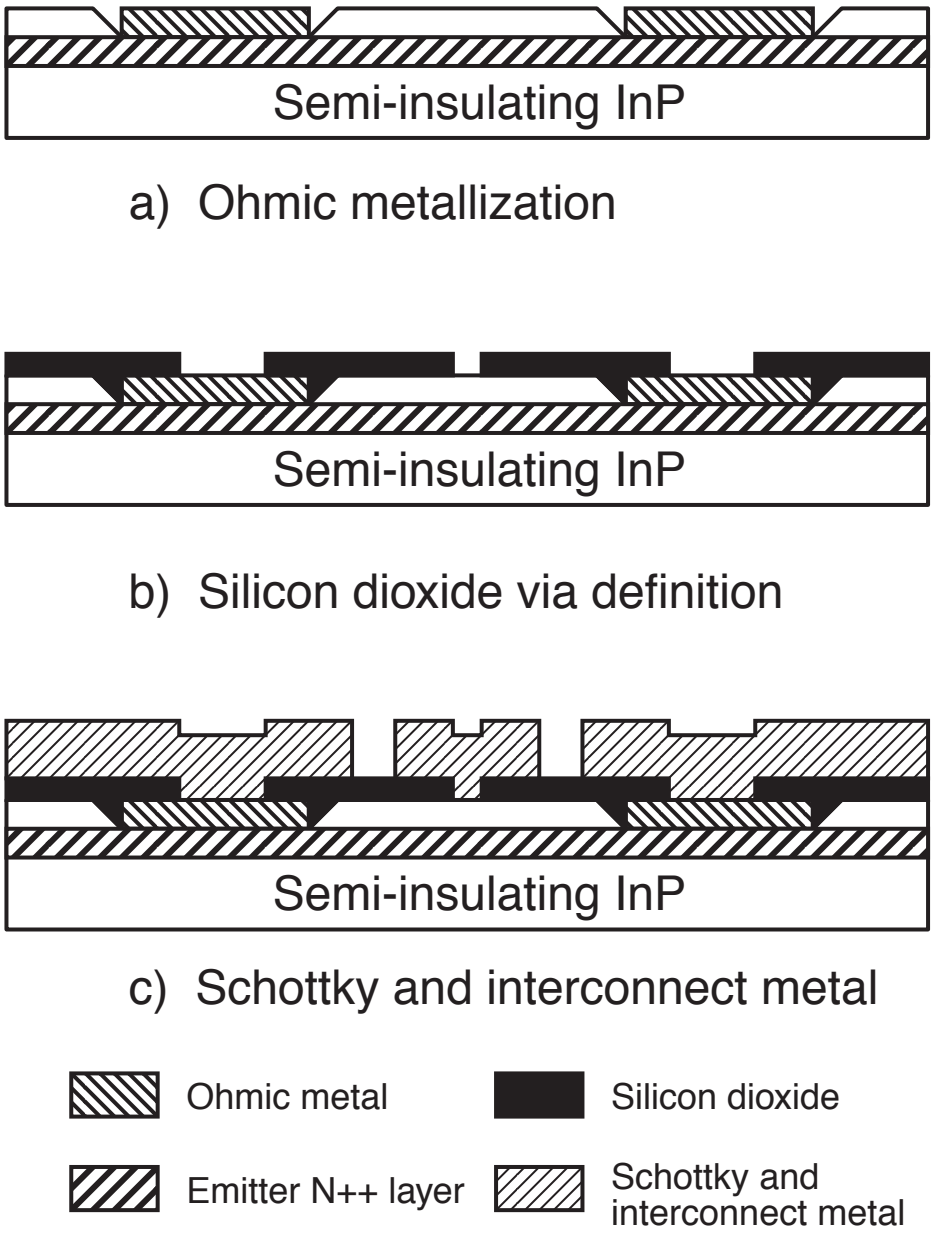

Figure 3.9: Process flow for fabricating large area SRTDs in a 3 mask process.

Sample	T_{pcap} (Å)	T_{sc} (Å)	$T_{barrier}$ (Å)
Sample A	100	350	17 (6ML)
Sample B	100	350	14 (5ML)
Sample C	100	250	17 (6ML)
Sample D	100	250	14 (5ML)
Sample E	0	350	17 (6ML)

Table 3.1: Layer structure parameter variations for the different samples during material characterization.

3.1.3 Large Area SRTDs

A simple 3 mask layer process was designed for fabricating large area SRTDs to evaluate the DC characteristics of the material after MBE growth. The nominal device area varied from 1.0 μm^2 to 12.0 μm^2. The process (figure 3.9) starts with the formation of Ohmic contacts to the emitter. This is achieved by recess etching to the emitter N++ layer and depositing Au-Ge-Ni metal. The Ohmic contacts are subsequently annealed at 360 °C for 10 s. Next, a 1000 Å silicon dioxide (SiO_2) layer is deposited by PECVD at 250 °C. Vias are then patterned by etching the SiO_2 layer in buffered hydrofluoric acid (BHF). The SiO_2 layer is removed both in regions where Schottky-collector contacts are required and above the emitter Ohmic metal. The SRTD junction area is determined by the size of the oxide via above the Schottky-collector. Hence, the undercut of the SiO_2 during the BHF etch should be well-controlled. Use of a dry etch in a reactive ion etcher (RIE) to minimize the undercut of the via to reproduce mask dimensions was ruled out for the fear of damage to the semiconductor surface. The undercut during the BHF etching of SiO_2 varied for different process runs. Therfore for small devices, the actual device contact area was grossly larger than the mask dimensions. In the last mask step, Schottky and interconnect metal (Ti/Pt/Au) is deposited. This forms both the Schottky-collectors and the contact pads for DC probing. DC characteristics can be now obtained to characterize the material growth. The complete process flow details are summarized in Appendix B.

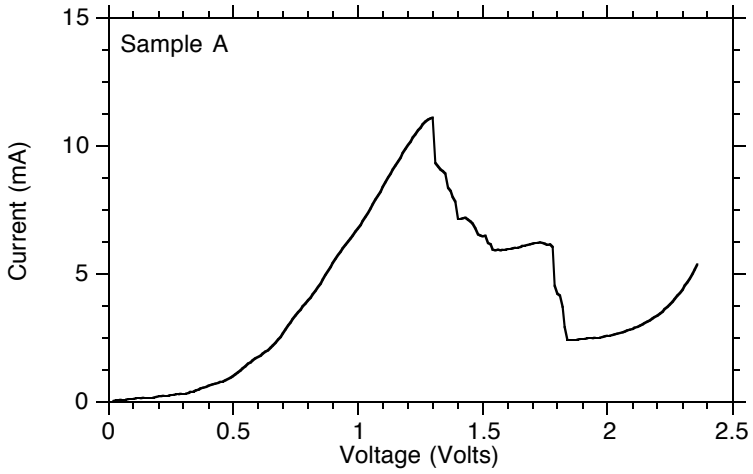

Figure 3.10: DC characteristics of a nominally 1.5 μm^2 area SRTD on sample A which had 6ML barriers and 350 Å undoped space-charger layer.

3.1.4 Results of DC Characterization

Large area SRTDs were fabricated to study the growth parameters and the layer structure design using the process described above. Samples with variations in layer structures as given in table 3.1 were grown by MBE. The DC characteristics obtained on the large area SRTDs allow determination of the presence or absence of NDR region, PVR, and the peak and valley voltages. The current densities J_p and J_v are determined within $\sim 2:1$ accuracy . A 0.5 μm expansion of each oxide via dimension was assumed to estimate the peak current density from the peak current of a device with a nominal area of 1.5 μm^2.

Initially, SRTDs were fabricated on samples A and B (table 3.1) which differed only in the thickness of the barriers. The undoped space-charge layer thickness was 350 Å, while the P-cap layer thickness was 100 Å. DC characteristics of the sample A (figure 3.10) indicated a V_p of 1.3 V and a V_v of 1.84 V. The PVR varied from 4.6 : 1 to 6.0 : 1 as the nominal device area varied from 1.5 μm^2 to 6.0 μm^2. For a nominally 1.5 μm^2 device, the peak and valley currents were 11.1 mA and 2.4 mA respectively. From this a peak current density of 3.7×10^5A/cm^2 was estimated for 6ML barrier thickness. When biased in the NDR region, devices with nominal areas >6.0 μm^2 were destroyed by excessive

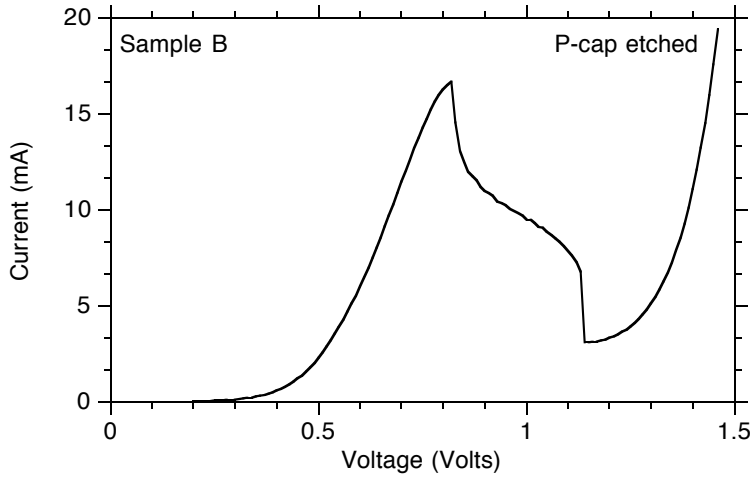

Figure 3.11: DC characteristics of a nominally 1.5 μm^2 area SRTD on sample B which had 5ML barriers and 350 Å undoped space-charger layer. The P-cap layer was etched within the active device.

power dissipation.

The DC characteristics of sample B indicated that even the smallest-area devices (1.5 μm^2) were destroyed at biases below the peak voltage due to the high current density. The NDR region was therefore not observed. A second set of devices were fabricated on sample B, where the P-cap layer was etched through the SiO_2 via immediately before the deposition of the Schottky contact metal. With the P-cap layer etched within the active device, V_p and V_v are reduced because of the thinner space-charge layer and the elimination of the P-doping. A nominally 1.5 μm^2 device on sample B (figure 3.11) with the P-cap etched showed a NDR region having V_p=0.82 V and V_v=1.14 V. The peak current was 16.6 mA, while the valley current was 3.1 mA. A peak current density of 5.5×10^5A/cm^2 was estimated for the 5ML barrier thickness. The PVR for these devices varied between 5.35 : 1 and 5.60 : 1 as the device area varied between 1.5 μm^2 and 6.0 μm^2. This variation is small when compared to the PVR variation on sample A.

In order to obtain a reasonable comparison between SRTDs with 5 and 6 ML barrier thicknesses, a second set of devices were fabricated on sample A with the P-cap etched. These devices had a similar current densities to the unetched

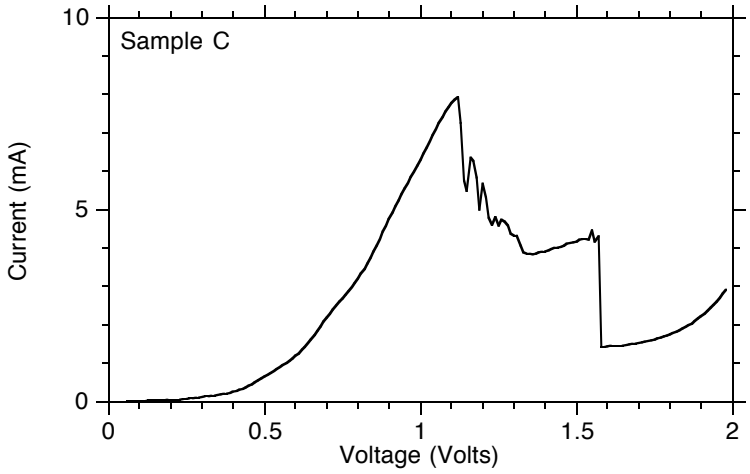

Figure 3.12: DC characteristics of a nominally 1.5 μm^2 area SRTD on sample C which had 6ML barriers and 250 Å undoped space-charger layer.

SRTDs on sample A, but the peak and valley voltages were reduced to 0.68 V and 1.02 V respectively. The PVR on these devices varied between 6.4 : 1 and 7.0 : 1 as the device area varied between 1.5 μm^2 and 6.0 μm^2.

Etching the P-cap reduces the RTD bias voltage and hence decreases the power dissipation in the device. Larger current densities can therefore be supported. However, selective etching of the P-cap is difficult when fabricating submicron devices. The etch rate through submicron openings cannot be monitored and the etch rate in submicron areas does not correlate well to the etch rates in larger open areas. The SRTDs were designed under the assumption that the P-cap would not be etched. The undoped space-charge layer thickness was reduced to 250 Å (samples C and D) to prevent device burnout at high current densities by lowering the peak and valley voltages.

The measured characteristics of devices with thinner 250 Å undoped space-charge layers and 100 Å P-cap layers will be shown here. On sample C with 6ML barriers, a nominally 1.5 μm^2 area device showed a NDR region (figure 3.12) at V_p=1.12 V and V_v=1.58 V. The peak current obtained was 7.9 mA. This corresponds to a peak current density of 2.6×10^5A/cm^2. This difference in the peak current density from the earlier 6ML barriers sample (sample A) is attributed to the variation in the oxide via dimensions rather than variations in

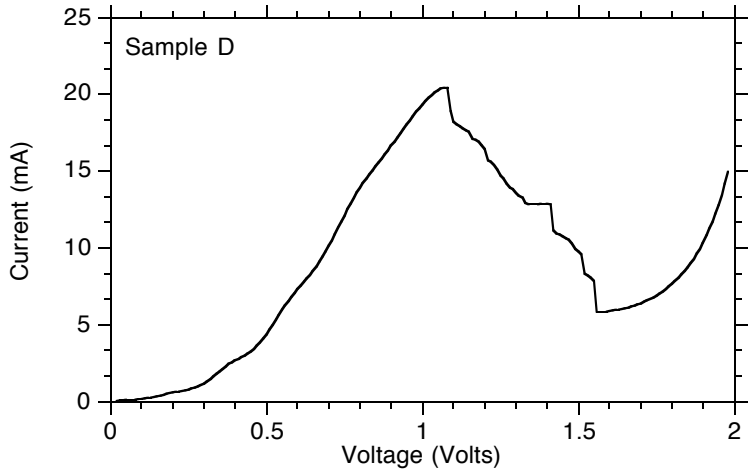

Figure 3.13: DC characteristics of a nominally 1.5 μm^2 area SRTD on sample D which had 5ML barriers and 250 Å undoped space-charger layer.

the material quality. On sample D with 5ML barriers, a nominally 1.5 μm^2 area device showed a NDR region (figure 3.13) at V_p=1.07 V and V_v=1.56 V with a peak current of 20.4 mA and a valley current of 5.85 mA. The PVR is 3.5 : 1, and the current density is approximately 6.8×10^5A/cm^2.

The peak negative conductance can also be estimated from these DC measurements by the empirical formula, $G_n = 2(\Delta I/\Delta V)$ where $\Delta I = I_p$-I_v and $\Delta V = V_v$-V_p. From this G_n=9.5 mS/μm^2 for the 6ML barriers and G_n=19 mS/μm^2 for the 5ML barriers. From these, given the 350 Å space-charge layer thickness, the R_nC time constant can be estimated as 315 fs for the 6ML barrier sample and 157 fs for the 5ML barrier sample. For an SRTD with 0.1 μm Schottky-collector contact, R_s and τ_{qw} can be estimated analytically. From this, an f_{max} of over 1.0 THz for 6ML barriers is projected , while a 2.0 THz f_{max} is projected for 5ML barriers. These parameters are sufficient for the project's goals, and the layer structure design and growth parameters of sample's C and D were selected for submicron SRTD fabrication.

To verify the necessity of the P-cap layer, SRTDs were also fabricated on a 6ML sample (sample E) having no P-cap layer. The PVR on devices from this sample decreased from 6.5 : 1 to 3.0 : 1 as nominal device area decreased from 12.0 μm^2 to 1.0 μm^2. These PVRs are significantly poorer than on the P-

cap devices. This implies that as the intrinsic device area is decreased, the DC characteristics become more susceptible to the parasitic leakage currents and the PVR is degraded. The PVR of devices on sample C varied from 7.0 : 1 to 5.3 : 1 as the nominal device area varied from 12.0 μm^2 to 1.0 μm^2. The P-cap layer has significant impact on the PVR of small devices. It was therefore concluded that the P-cap would be essential for deep submicron SRTD fabrication.

With the growth conditions and layer structure design determined, a large number of wafers of designs C and D were grown for the subsequent phase of the project, fabrication of 0.1 μm SRTDs.

3.2 Submicron SRTD Fabrication

The goal during this phase of the project was to develop a process for fabricating 0.1 μm InGaAs SRTDs having bandwidths over 2.0 THz. Earlier high f_{max} RTDs [7],[8] were whisker-contacted devices. Whisker contacted devices are not appropriate for array fabrication, and the f_{max} is somewhat low. Besides, RTD circuits consisting of more than one device are possible only if the devices are fabricated in an integrated circuit (IC) process that permits monolithic integration. An IC process was therefore developed that would eventually be utilized for monolithic SRTD circuits. Submicron InGaAs SRTDs with both 6ML and 5ML barriers were fabricated in this IC process. The key feature of this process is the electron beam lithography for fabricating the submicron Schottky-collector. The process development required substantial efforts, as discussed subsequently.

3.2.1 Device Structure

The 0.1 μm Schottky-collectors for the submicron InGaAs SRTDs were fabricated by a sophisticated e-beam lithography process developed at JPL specifically for this project. The devices are embedded in 50 Ω microwave pads for both DC and microwave characterization. The SRTDs themselves are located on the top of a mesas created for isolating individual devices on the wafer. The microwave pads are located at the bottom of the mesas on the semi-insulating substrate. These mesas are created by a wet etch for device isolation, as the planar proton-implant-isolation processes are not feasible with heavily doped, thick InGaAs layers. The biggest technological difficulty lies in connecting the 0.1 μm Schottky-collector on top of the mesa to the microwave pad at the bottom of the mesa.

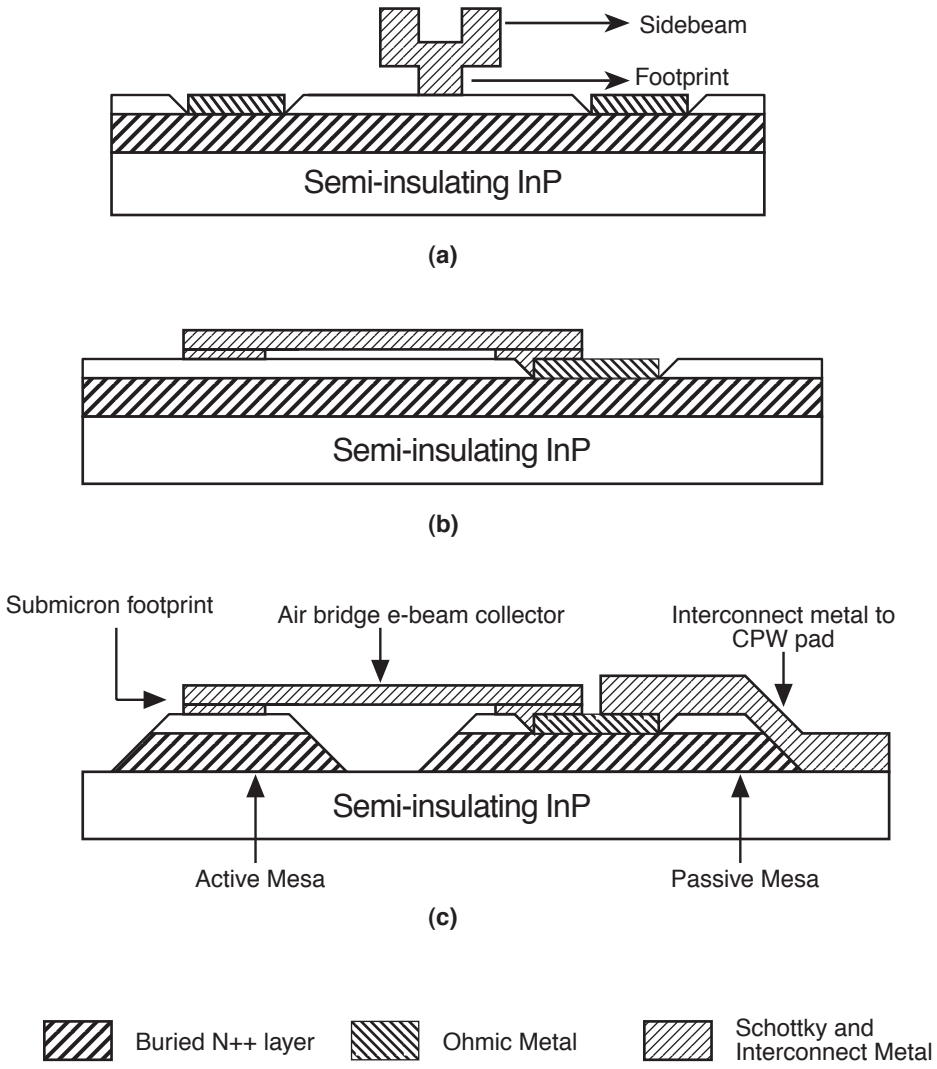

Figure 3.14: Cross-sectional views of the 0.1 μm InGaAs SRTD showing the various features of the airbridge e-beam finger. (a) The T-gate cross- section on the active mesa, (b) side view showing the flying e-beam finger before mesa definition, and (c) side view showing the device after completion of fabrication.

There are also some difficulties associated with a simple adaptation of the standard T-gate process to define the Schottky-collector. Since, the device area in such a situation is defined by the overlap of the mesa edge and the T-gate footprint, the $\sim$ 1-2 μm alignment tolerances between the two mask layers would give a similar magnitude of variation in the device stripe length. Since the required device stripe lengths are $\sim$ 3-4 μm, this would lead to a wide variation in the device characteristics. The wet etch processes used for mesa isolation to create the mesas also undercut along the exposed metal-semiconductor interfaces. The footprint of the T-gate would undercut, attacking the active device region, and giving rise to variations in the device characteristics. Such variability is highly undesirable in an integrated circuit fabrication. Efforts are therefore required to obtain reproducible and uniform device characteristics across the wafer.

A device structure (figure 3.14) was designed that would provide the required connections between the 0.1 μm Schottky-collectors and the microwave pads and also define the Schottky-collector stripe length accurately. The structure consists of an active mesa and a passive mesa. On top of the active mesa lies the active device whose contact area is defined by an airbridge e-beam finger. This airbridge e-beam finger spans across from the active mesa to the passive mesa. The footprint of the T-gate e-beam finger contacts the semiconductor active mesa only in regions where the Schottky-collector is required. The Schottky-collector area is thus accurately defined. On the passive mesa, the e-beam finger contacts Ohmic metal. The Ohmic pad metal is later connected through interconnect metal to microwave pads. The airbridge e-beam finger is thus anchored between the active mesa and the passive mesa only at its two ends and is elsewhere suspended above the semiconductor surface.

The interconnect metal runs over the outward-sloping edges of the active and passive mesas to contact the ohmic pads. Airbridge contacts to the mesas are not required which reduces the required mesa dimensions.

0.1 μm Schottky-collector devices with nominal contact area ranging from 0.05 μm^2 to 0.4 μm^2 were defined on the mask design. The expected capacitance of these devices is too small to be readily measured. Therefore, large area devices with contact areas of 1.7 μm^2 and 3.4 μm^2 were also included on the mask set. These large area devices would have a parasitic capacitance in the vicinity of 10-20 fF, which could be easily measured on a network analyzer.

3.2.2 Electron Beam Lithography

The key to fabricating the proposed device structure is the e-beam lithography process which creates the airbridge 0.1 μm Schottky-collector in a single lithography and metallization step. The process uses a trilayer resist consisting of PMMA/COPMMA/PMMA similar to a standard T-gate e-beam lithography process. The standard process was modified to meet the specifications for the airbridge Schottky-collector. A process developed by Tiberio et. al. [10] uses multiple scans at different electron doses to expose the footprint and the side-beams of the T-gate separately. This technique provides the flexibility to arbitrarily define the size of the footprint and the side beams. The process developed at JPL, airbridges creates airbridges by limiting the areas where the footprint penetrates the bottom resist layer. The collector is then anchored to the semiconductor only at locations where all the three layers of resist were developed away, with the remainder of the structure becoming an airbridge.

The e-beam lithography process development was done at JPL on a JEOL JBX 5DII e-beam lithography system running at 50 KV using aperture 2 in the 5^{th} lens with a beam current of 200 pA. The pattern is written as rectangles rather than lines. The bottom layer of the trilayer resist is polymethylmethacrylate (PMMA) which is a 496K molecular weight 2.5% solids in chlorobenzene. A premixed 4% solution was thinned using a premixed 1% solution to arrive at the 2.5% solution. A dynamic dispense speed of 500 rpm is followed by a 2 second spread speed of 1200 rpm and a final spin at 4000 rpm for 30 s. A one minute hot plate bake at 115 °C precedes the 170 °C hotplate cure bake. After cooling the sample, a layer of PMMA methacrylic acid copolymer (PMMA/MAA) (9%) is applied using the same spin speed and cure technique as for the first layer. A final layer of 950K 2% PMMA is applied and baked in a similar manner. Premixed 2% 950K PMMA is substituted for 1.5% 2300K PMMA that had to be mixed from a powder and chlorobenzene. Multiple doses are used for exposing the PMMA to generate the T-gate and the airbridge structure. A high dose of 290 μC/cm^2 is used to define the Schottky-collector footprint area. This penetrates all the way down to the semiconductor surface. Lighter doses of 70-80 μC/cm^2 are used to produce the sidebeams of the T-gate and the airbridge. A moderate dose of 90 μC/cm^2 is used to define the contact area to the Ohmic metal contact pad on the passive mesa.

Development of the trilayer PMMA resist is carried out in a multistep process. With the anodes oriented horizontally, the sample is dipped in chlorobenzene for 15 to 17 s, followed by a toluene rinse for 5 s and toluene spray for 10 s. This first part of development quickly dissolves the top layer of PMMA where it has

been exposed, but has only a slight effect on the intermediate copolymer layer. In the second part of the development, the exposed copolymer dissolves in a one to one mixture of isopropyl alcohol (IPA) and methanol agitated by a magnetic stirrer bar rotating at 100 rpm for 2 mins. This development stage undercuts the top PMMA layer. The final develop step uses a one to one mixture of methyl isobutyl ketone (MIBK) and IPA to dissolve the bottom exposed PMMA. Again a stirrer bar is used and the sample is exposed to the solution for 2 mins. IPA is used for final rinse followed by nitrogen blow dry.

To determine if the anodes are fully developed, the samples are inspected in a scanning electron microscope (SEM) at an accelerating voltage of 2 KV. An additional MIBK : IPA development is carried out if the initial development is found incomplete. In preparation for the anode metallization, the sample goes through a cleaning/etch step. Residual organics are removed through a 30 s oxygen plasma descum at 50 W and a pressure of 0.5 Torr. The etch sequence starts with a 10 s IPA : DI (1 : 10) dip to improve surface wetting, followed by 20 s dip in NH_4OH : H_2O (1 : 30). The sample is rinsed in DI and then immersed in buffered oxide etch (BOE) for 30 s to remove any surface oxides. After a DI rinse, the sample is etched for 15-20 s in H_2O_2 : Citric acid : DI (1 : 11 : 44). The etch is stopped by a DI rinse followed by an additional 20 s dip in NH_4OH : DI and nitrogen blow dry immediately before loading into the evaporator. The metallization consists of 300 Å of Ti, 300 Å of Pt and 3000 Å of Au. The metallization is lifted off in acetone in a hot water bath followed by a methanol soak and a DI water rinse. This completes the fabrication of the airbridge submicron Schottky-collector.

3.2.3 Device Fabrication

The complete submicron SRTD fabrication is achieved in a four mask layer process. The process flow is illustrated in figure 3.15. Fabrication begins with the formation of Ohmic contacts to the emitter N++ layer. After patterning the resist, a self-aligned recess wet etch to the emitter N++ layer is achieved using a H_3PO_4 :H_2O_2 :H_2O (3 : 1 : 50) etch. During the initial process runs, a significant undercut between the two emitter ohmic pads was observed. This was etching the semiconductor layers between the Ohmic pads where the Schottky-collector would be later defined. This undercut was correlated to poor adhesion of the photoresist mask protecting the Schottky-collector area. The poor adhesion was overcome by increasing the dehydration bake times and using a thinner resist. After the recess etch, Au-Ge-Ni contact metal is deposited. The Ohmic contacts

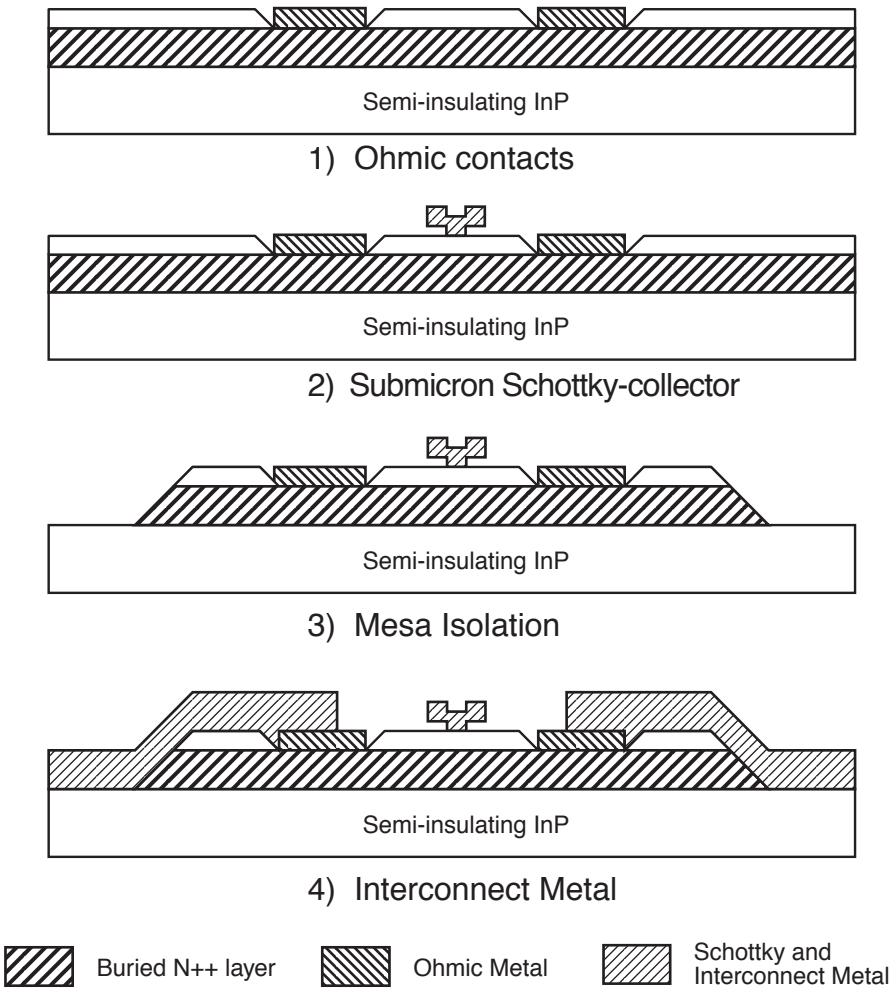

Figure 3.15: The four mask layer process for fabrication of $0.1\mu m$ InGaAs SRTDs (a) Emitter ohmics (b) 0.1 μm airbridge e-beam Schottky-collector (c) Mesa isolation and (d) Interconnect metal

were then annealed in a rapid thermal annealer at 360 °C for 10 s. The Ohmic contacts were tested by measuring the transmission line measurement (TLM) test structures. In the second mask layer, 0.1 μm Schottky- collectors are defined using the airbridge e-beam Schottky-collector process.

Isolation mesas were then created by a wet etch $H_3PO_4 : H_2O_2 : H_2O$ (3 : 1 : 50). During the isolation step, active and passive mesas are created. The semiconductor layers between the active and passive mesa beneath the airbridge e-beam finger is also etched away by the undercut thus isolating the active and passive mesas. This is monitored by measuring the device characteristics. Before the isolation step, the SRTD on top of the active mesa is shunted by a resistance through the emitter N++ layer. When all semiconductor material between the two mesas is removed, only the SRTD characteristics showing the NDR are observed. The isolation is also visually checked in a SEM to ensure that there are no conducting layers between the active and passive mesas. The time required to remove the material beneath the airbridge e-beam finger determines the total etching time which is typically twice as much as required for etching down till the semi-insulating substrate. Due to the long over etch times, the mesa edges undercut quite significantly. After the mesa isolation, the edges should be sloping outwards as this is necessary for step coverage of the interconnect metal in the next mask step. In the final mask step, Ti/Pt/Au interconnect metal is deposited. This provides interconnections to top of both the active and passive mesas of the device. The interconnect metal runs over the gently sloping edges of the mesa and connects with the ohmic metal to provide connections between the two terminals of the SRTD and the microwave pads on the semi-insulating InP substrate. The complete process flow is provided in Appendix C.

Figure 6.11 shows a scanning electron micrograph of a fabricated 0.1 μm^2 InGaAs SRTD. The airbridge e-beam finger between the two Ohmic pads on the active mesa shows the T-gate footprint contacting the semiconductor only where the notch in the metal is seen. This notch defines the actual contact area of the device. The e-beam finger then airbridges over the semiconductor surface to contact the Ohmic metal on the passive mesa (not shown in the SEM).

3.3 Measurements of Submicron SRTDs

With the process described above, 0.1 μm InGaAs SRTDs were fabricated with both 5ML and 6ML barriers. DC and microwave characteristics of the fabricated devices were obtained. From the measured DC and microwave characteristics, small signal models were developed which would be later utilized for circuit

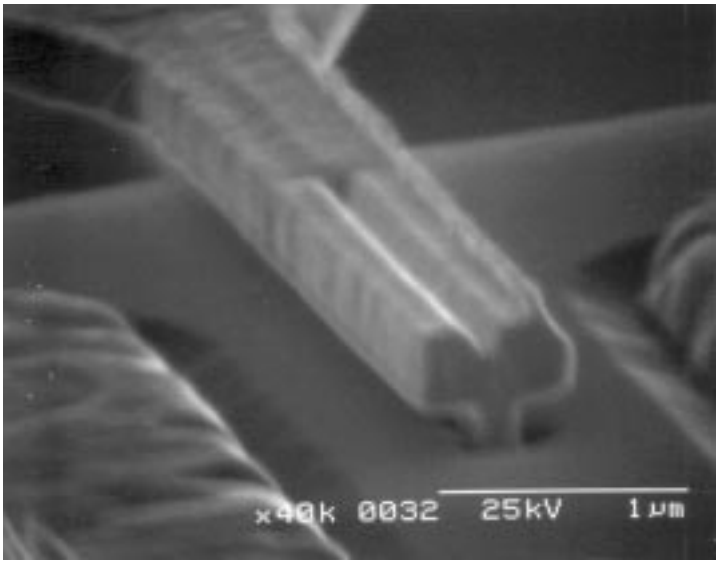

Figure 3.16: SEM photomicrograph of a fabricated 0.1 μm^2 InGaAs SRTD showing the 0.1 μm airbridge e-beam Schottky-collector between the two Ohmic pads.

design at submm-wave frequencies. However, these models cannot be verified at frequencies beyond 40 GHz due to the limited bandwidth of the available measurement instruments. The DC I-V characteristics were initially obtained to verify whether the devices had the NDR characteristics as expected. The devices were then stabilized in a 50 Ω system to obtain stable I-V characteristics in the NDR region. This would allow accurate characterization of the devices even in the NDR region. The device capacitances are then measured on a network analyzer at zero bias. To account for the spreading of the electric field beneath the Schottky-collector an effective width of 0.2 μm was assumed for the 0.1 μm Schottky-collector footprint. The effective area was calculated using the effective collector width before normalizing the device parameters to 1.0 μm^2 effective area device.

3.3.1 DC Measurements

From DC measurements, peak and valley voltages and currents were determined. Estimates for the peak negative conductance were obtained by the empirical relationship $G_n = 2(\Delta I/\Delta V)$. DC characteristics of 0.1 μm InGaAs SRTDs with 6ML barriers are summarized in table 3.2 for devices with different stripe lengths. The unstabilized measurements do not provide accurate measurements

Stripe length(μm)	V_p (V)	I_p (mA)	V_v (V)	I_v (mA)	PVR	J_p ($\times 10^5$ A/cm^2)	G_n (mS/μm^2)
0.5	1.14	0.19	1.49	0.10	1.89	1.91	5.14
1.0	1.08	0.39	1.49	0.19	2.02	1.96	4.83
2.0	1.05	0.81	1.45	0.38	2.13	2.01	5.33
4.0	1.03	1.62	1.46	0.75	2.17	2.03	5.09
17.0	1.05	7.15	1.45	3.16	2.26	2.10	5.87
34.0	1.05	14.26	1.45	6.30	2.26	2.10	5.85

Table 3.2: Summary of DC characteristics of 0.1 μm SRTDs with 6 ML barriers.

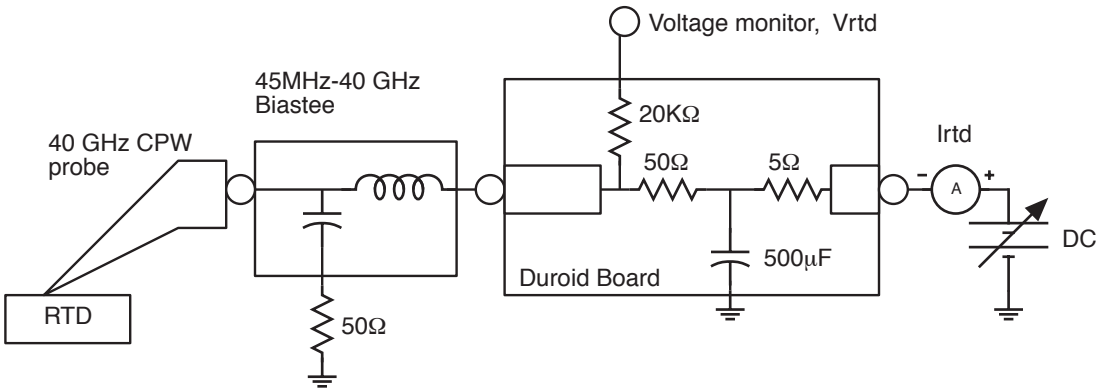

Figure 3.17: Biasing network to present a 50 Ω impedance to the SRTD from DC to 40 GHz for stabilizing the device in the NDR region.

in the NDR region as the devices are unstable due to oscillations in the bias circuit.

The devices can be stabilized in the NDR region using a network shown in figure 3.17. This allows for accurate characterization of the device even in the NDR region. Without this network, the biasing circuitry and the RTD form a parallel resonant circuit at some frequency below f_{max}, where parasitic oscillations will occur if the total conductance in the circuit is negative. The stabilizing biasing network ensures that the RTD is shunted with a conductance of approximately 20 mS from DC to at least 40 GHz. This implies that a device with a $G_n < 20$ mS will be stable at least from DC to 40 GHz. However, this is not strictly sufficient for stability as the biasing circuit could present uncontrolled

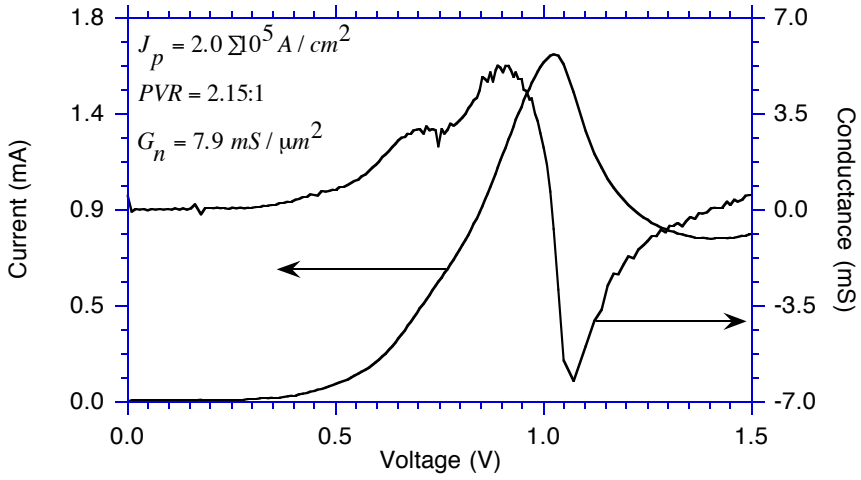

Figure 3.18: Stabilized DC characteristics of a 0.1 μm SRTD with 6ML barriers and 0.8 μm^2 effective area.

impedances to the SRTD at frequencies higher than 40 GHz. Typically, there is sufficient high frequency loss through the probes and cables at frequencies above 40 GHz that the device is presented with a $\sim$ 50 Ω impedance. The problem is usually with low frequency oscillations which are suppressed by the network if the device area is chosen appropriately. With this network, stabilized I-V measurements were obtained for SRTDs with peak $G_n < 5$ mS. The stabilized I-V characteristics for an SRTD with 6 ML barriers are shown in figure 3.18. This device has an effective area of 0.8 μm^2, a peak current density of 2×10^5 A/cm^2 at 1.03 V, a PVR of 2.15 and a measured peak G_n of 7.9 mS/μm^2.

DC characteristics of 0.1μm InGaAs SRTDs with 5 ML barriers are summarized in table 3.3 for devices with different stripe lengths. The stabilized I-V characteristics for an SRTD with 5 ML barriers are shown in figure 3.19. This device has an effective area of 0.4 μm^2, a peak current density of 5×10^5 A/cm^2 at 0.95 V, a PVR of 1.7 and a measured peak G_n of 19 mS/μm^2.

The emitter Ohmic contact resistance and the sheet resistance for the emitter N++ layer were obtained from transmission line measurements (TLM) data. The bulk resistivity of the emitter N++ layer was measured to be 2.2 $\Omega - \mu$m, while the contact resistance was measured to be 6.5 $\Omega - \mu$m. From these, a parasitic resistance R_s of 2.2 $\Omega - \mu$m^2 was calculated, after normalizing to a 1.0 μm^2

Length (μm)	V_p (V)	I_p (mA)	V_v (V)	I_v (mA)	PVR	J_p ($\times 10^5$ A/cm^2)	G_n (mS/μm^2)
0.5	1.05	0.43	1.36	0.30	1.42	4.26	8.13
1.0	1.03	0.98	1.38	0.60	1.63	4.88	10.78
2.0	1.00	2.01	1.38	1.19	1.70	5.04	10.91
4.0	0.95	4.16	1.31	2.37	1.76	5.20	12.47

Table 3.3: Summary of DC characteristics of 0.1 μm SRTDs with 5 ML barriers.

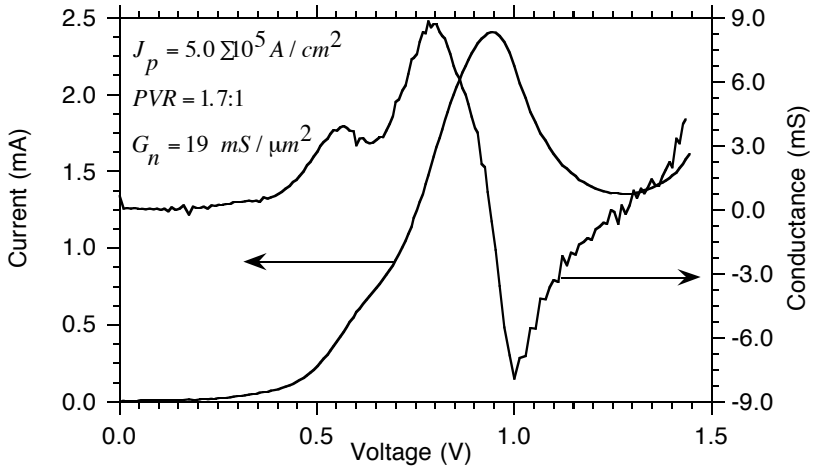

Figure 3.19: Stabilized DC characteristics of 0.1 μm InGaAs SRTD with 5ML barriers with 0.4 μm^2 effective area.

effective Schottky-contact area. From these DC measurements, G_n and R_s of the small signal model were obtained for 0.1 μm InGaAs SRTDs with both 5ML and 6ML barriers.

3.3.2 Microwave Measurements

The device capacitance was obtained from network analyzer microwave measurements to 40 GHz. The device capacitance is obtained from zero bias measurements on large area devices. These devices have sufficiently large capacitance to be measured from reflection measurements on a network analyzer. The DC characteristics of the large area devices (1.7 μm^2 and 3.4 μm^2) on the 6ML sample had been obtained earlier (table 3.2). From the measured DC characteristics, the current on large area devices scales with area from the small-area devices. Therefore, the capacitances should also scale with area. The capacitance measured on a large-area device can be used to obtain capacitance per unit area. From the measured S-parameters of large area devices, a capacitance per unit area of 3.0 fF/μm^2 was obtained.

Quantum-well lifetimes were calculated by Dr. Schulman of Hughes Research Laboratories using a two band model developed by Chow et. al. [15] for estimating the intrinsic time constants of InGaAs RTDs. The quantum-well lifetimes were calculated as 0.2 ps for the 6ML sample and 0.12 ps for the 5 ML sample. With these measured and calculated parameters, the complete small signal models were obtained for both 6ML and 5 ML samples when biased at the peak negative conductance point in the NDR region.

3.4 f_{max} Estimates

From the measured DC and microwave parameters and the calculated quantum-well lifetimes, small signal models (figure 2.3) were obtained for 0.1 μm InGaAs SRTDs with both 5ML and 6ML barriers. These are summarized in table 3.4. The small signal parameters can be used to obtain an estimate for f_{max} of the SRTD. The estimated f_{max} for a 0.1 μm SRTD with 6 ML barriers is 1.2 THz. The estimated f_{max} for a 0.1 μm SRTD with 5 ML barriers is 2.2 THz. These bandwidth numbers are estimates and must be experimentally verified. However, the bandwidth of these devices is so large that no significant variation is observed in the device small signal parameters over a DC-40 GHz bandwidth [26]. Hence it is not possible to obtain reliable f_{max} extrapolations from measurements to 40 GHz. This is in marked contrast to characterization of high

Sample	J_p (A/cm^2)	G_n ($mS/\mu m^2$)	C ($fF/\mu m^2$)	R_s ($\Omega - \mu m^2$)	τ_{qw} (ps)	f_{max} (THz)
6 ML	2.0	7.9	3.0	2.2	0.20	1.2
5 ML	5.0	19.0	3.0	2.2	0.12	2.2

Table 3.4: Small signal model parameters for 0.1 μm InGaAs SRTDs with 5 ML and 6 ML barriers, normalized to unit effective area.

f_{max} transistors (HEMTs and HBTs). The difficulty in accurately determining f_{max} is characteristic to all published RTD work. Experimental verification is possible by demonstration of submm- wave circuits designed on the basis of the small-signal models. This will be the next goal of the project. However, these estimated bandwidths are over 2 : 1 larger than those estimated for other RTDs reported to date.

The significant contribution of this part of the work is in deep submicron scaling of InGaAs RTDs and the resulting improvement in RTD bandwidth. Essential to obtaining high f_{max} in submicron scaling, is the introduction of Schottky-collector to the RTD. Because the SRTD must be both laterally scaled to ~ 0.1 μm and vertically scaled to ~ 350 Å dimensions, the process technology development is demanding. The next goal of the project is to use this technology for submm-wave oscillator circuits.

Chapter 4

Bias Stabilization

Demonstration of submm-wave oscillator circuits with the 0.1 μm InGaAs SRTD technology is the next phase of the project. However, there are significant difficulties in building RTD oscillators at any frequency. These problems arise from DC bistability or parasitic low frequency bias circuit oscillations. Several constraints are placed on the RTD parameters in order to suppress these undesired oscillations. These limit the maximum achievable RTD oscillator power. Since the goal is to generate significant power at submm-wave frequencies, solutions were developed that would eliminate the power limitations of RTD oscillators. A bias stabilization scheme was developed in this project, which solves the problem of DC bistability and parasitic bias circuit oscillations. The techniques was first demonstrated by a bias stabilized microwave RTD oscillator. Extending this technique to submm-wave SRTD oscillators requires on wafer bias stabilization. This is realized in the form of a graded bandgap AlInAs Schottky-diode. The various features of the bias stabilization technique are described in this chapter. The on wafer bias stabilization technique for submm-wave RTD oscillators was proposed by Prof. Herbert Kroemer at UCSB.

4.1 Problem

In this section, the difficulties associated with building submm-wave RTD oscillators are identified. When biased in the NDR region, RTDs provide negative differential resistance characteristics up to THz frequencies. An RTD will oscillate if the sum of the RTD and the terminating admittances has a negative real part. Oscillators could be therefore be designed at any frequency up to f_{max}, with the negative resistance element. However, due to the presence of

the negative resistance from DC to f_{max}, instability conditions can also exist at frequencies other than the design frequency. This leads to RTD oscillations in several undesired modes. The instability at DC is called DC bistability while the resonances in the bias circuit which result in RTD oscillations are referred to as parasitic bias circuit oscillations. DC bistability prevents the RTD from being biased in the NDR region, thus upsetting the bias conditions necessary for initiating oscillations at the design frequency. In the presence of parasitic bias circuit oscillations, the available energy from the RTD oscillator will be shared between the different oscillating modes thereby reducing the power in the desired mode. Further, the partitioning of power between the 2 oscillation frequencies is often chaotic [31]. Therefore, it is essential to suppress the parasitic oscillations. This can be achieved by ensuring that the RTD circuit is stable at all frequencies except at the design frequency of oscillation.

Several solutions have been proposed in the past to overcome DC bistability and parasitic bias circuit oscillations. In one proposed method, the RTD is biased in the PDR region and the oscillations are initiated by applying an RF signal to push the RTD into the NDR region. Examples of this kind of approach include RTD multivibrator oscillators [32] or RF excitation [33]. DC biasing of the RTD in the PDR region eliminates the problems associated with the negative resistance in the bias circuit. Even though DC bistability is overcome in these examples, the RTD circuit can be unstable at many frequencies other than the desired frequency of oscillation. In the presence of several unstable frequenices, mode competetion could exist between the different oscillating modes of the RTD. Due to the non-linear RTD I-V characteristics and in the presence of mode competetion, the voltage amplitude at one unstable frequency determines the RTD current and hence, its negative conductance at a different unstable frequency. If the voltage amplitude of one frequency is intentionally made larger than the others, then the negative conductance at other frequencies can be suppressed. This can be calculated for a cubic approximation to the RTD I-V characteristics. Assuming that the RTD circuit can support two competing modes of oscillation (at frequencies ω_{des} and ω_{undes}), the voltage across the RTD is $V_{des}\cos(\omega_{des}t) + V_{undes}\cos(\omega_{undes}t)$. If $V_{des} \gg V_{undes}$, then a large signal analysis gives an average negative conductance (averaged over one cycle) at ω_{des} as $G_n/2$, while the average negative conductance at ω_{undes} is zero. Thus, by setting an initial condition $V_{des} \gg V_{undes}$ through the application of an RF signal at ω_{des}, oscillations can be suppressed in the undesired mode. The system can then sustain steady state oscillations at ω_{des} because of the suppression of negative conductance at all other undesired frequenices. Thus, in the presence of

mode competetion, the mode with the largest signal will win and the RTD will sustain oscillations in this mode. However, if the system is ever disturbed from its steady state oscillations, there is no guarantee that it will self-restore to its desired oscillation frequency. Such schemes are not very desirable for submm-wave oscillator circuits because of the requirements of a very high frequency RF signal source and the necessity for reapplication of the RF signal in case of power supply interruptions to the RTD oscillator. Ideally, oscillations in any oscillator circuit should be initiated only at the design frequency by a simple application of DC bias to the circuit.

Kidner et. al. [12, 13] have studied the stability requirements of RTDs for suppressing both DC bistability and parasitic bias circuit oscillations. Design constraints were proposed on the maximum RTD area for suppressing DC bistability or the undesired parasitic bias circuit oscillations. Limiting the maximum area of the device places an upper bound on the maximum power achievable from the RTD. Due to these limitations, the output powers of RTD oscillators are considerably well below one mW. In this project, a bias stabilization scheme is developed which eliminates the constraints on the maximum device area as well as the need for external RF excitation. Before discussing the features of this scheme, the various limitations imposed by the stability requirements are studied for a typical RTD oscillator to emphasize the need for the proposed bias stabilization scheme.

4.2 Maximum RTD Output Power

In this section, expressions for maximum power achievable from an RTD oscillator are derived for a typical RTD oscillator (figure 4.1) in the absence of any limitations imposed by stability requirements [34]. The oscillator circuit consists of an RTD biased in the NDR region. The RTD is represented by a small signal equivalent circuit consisting of a negative conductance G_n. The RTD parasitics, resistance R_s and capacitance C_{rtd}, are neglected in this model and their effect will be included later. The RTD is shunted by a parallel resonant circuit consisting of L_{res} and C_{res}, that is resonant at the desired frequency of oscillation f_{osc}. A resistance G_{load} is connected in parallel to deliver the power to the load.

At the applied bias voltage, oscillations can begin if the net node admittance of the circuit has a negative real part. As the amplitude of the oscillations begin to grow the total instantaneous voltage (ac+dc) across the RTD changes. Eventually, the amplitude of oscillations reach a stable state when the effective average negative conductance is balanced by the load and losses in the circuit.

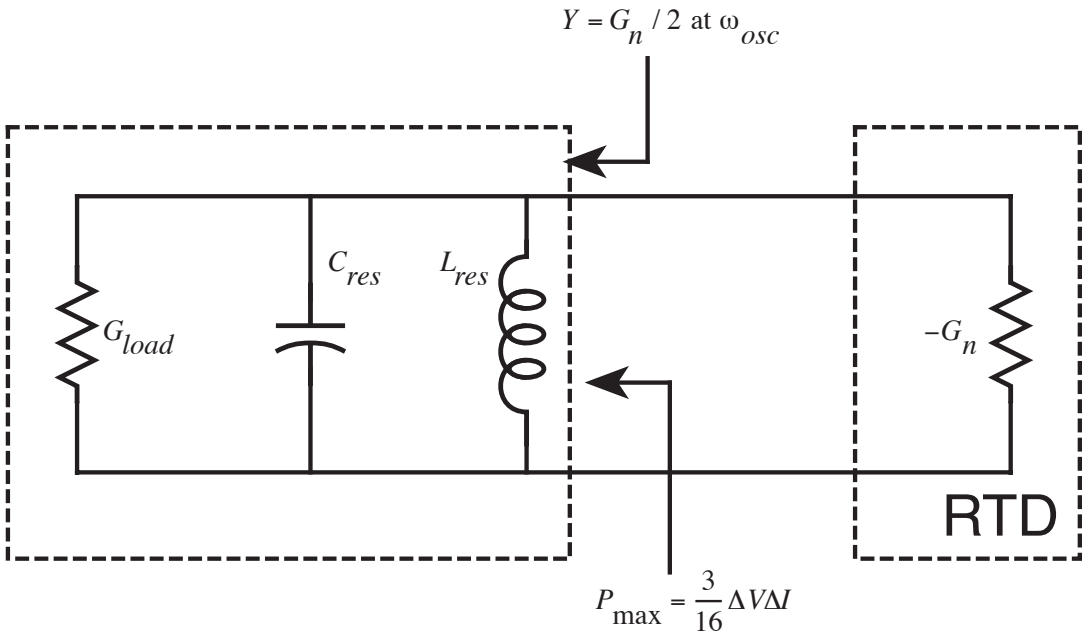

Figure 4.1: A general oscillator configuration consisting of an RTD biased in NDR region, shunted by a parallel resonant circuit and a load conductance.

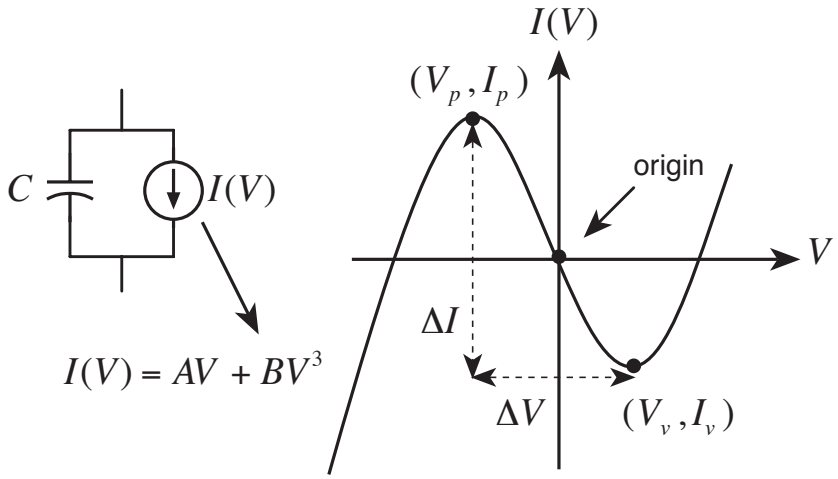

Figure 4.2: A large signal model for the RTD biased in the NDR region. The voltage controlled current source $I(V)$ is modeled by a cubic polynomial fit to the I-V characteristics. In a small signal model the voltage controlled current source $I(V)$ is replaced by a small signal negative conductance G_n.

This implies that the RTD voltage swing could be so large that the total instantaneous voltage across the RTD takes it into the PDR region. For such large swings, a small signal analysis of the RTD is no longer valid and a large signal model is necessary.

For a large signal analysis, the RTD is modeled as a voltage controlled current source $I(V)$ (figure 4.2). The nonlinear I-V characteristics of the RTD can be represented by a cubic polynomial fit to the RTD DC characteristics. Shifting the origin of the axis to the DC bias point for the sake of convenience, the I-V characteristics can be represented by a cubic polynomial $I(V) = AV + BV^3$ where A and B are constants. These constants can be related to ΔV and ΔI which represent the extent of the NDR region. By equating the slope of the I-V curve to zero at the peak and valley points, the constants A and B can be determined (equation 4.2). From this, the small signal negative conductance (at the origin) is given by $G_n = (3\Delta I)/(2\Delta V)$.

$$I(V) = AV + BV^3 \tag{4.1}$$

$$= -\frac{3\Delta I}{2\Delta V}V + \frac{2\Delta I}{\Delta V^3}V^3 \tag{4.2}$$

Due to the filter action of the parallel resonant circuit, the voltage across it is

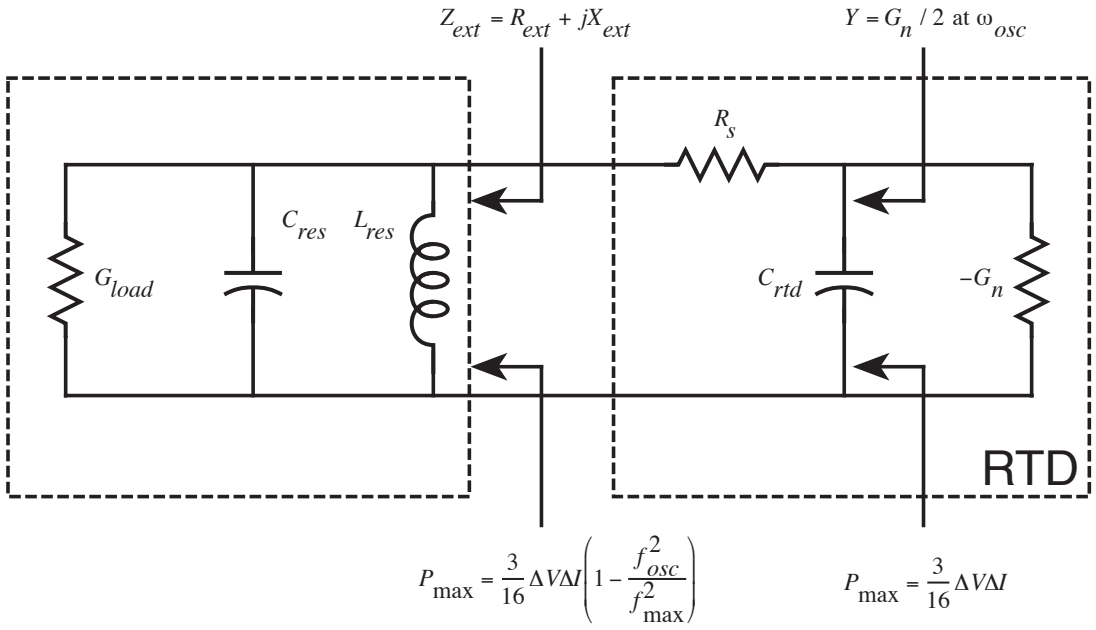

Figure 4.3: A general oscillator configuration consisting of an RTD and its parasitics, shunted by a parallel resonant circuit and a load conductance.

assumed to be essentially sinusoidally varying with time ($V_{osc}\cos(2\pi f_{osc}t)$), after steady state oscillations have been reached in the oscillator circuit. By equating the average power dissipated in the load during one cycle to the average generated ac power, peak oscillation amplitude V_{osc} can be determined. From this, the power delivered to the load is calculated as a function of the coefficients A, B and the load resistance G_{load}. An optimum value of the load resistance G_{load}, for maximum power transfer to the load can be then obtained. This optimum load resistance occurs for a value of $G_{load} = G_n/2$. Equivalently, under steady state oscillations and maximum output power condition, the average negative conductance of the RTD is $G_n/2$. At the optimum value of load resistance, the maximum output power P_{max}, delivered to the load is given by $P_{max} = A^2/6B$. From equation 4.2, substituting for the coefficients A and B, the maximum output power P_{max} reduces to $(3/16)\Delta I \Delta V$.

The RTD parasitics, R_s and C_{rtd} were neglected in the above RTD model. When the effect of RTD parasitics is included, the maximum output power decreases quadratically with frequency as given by equation 4.4. This equation is obtained by including the RTD parasitics in the RTD model of the typical oscillator configuration (figure 4.3). For this oscillator, the external load Z_{ext} should

be chosen such that $(Z_{ext}+R_s) \parallel (1/j\omega C_{rtd}) = 1/Y = 2/G_n$, for maximum power transfer to the load. This power is delivered to both R_s and R_{ext} in the ratio of $R_s : R_{ext}$. Under steady state oscillations, the lossy resistance is balanced by the average RTD negative resistance $G_n/2$. Therefore, equating the real part of loop impedance to zero gives the relationship, $R_{ext}+R_s = 2G_n/(G_n^2+4\omega_{osc}^2 C_{rtd})$. At $\omega_{osc} = \omega_{max}$, the net impedance across the RTD terminals has zero real part. This gives the relationship, $R_s = 2G_n/(G_n^2 + 4\omega_{max}^2 C_{rtd}0$. Therefore, the maximum output power P_{max} delivered to the external load is given by equation 4.3.

$$P_{max} = \frac{3}{16}\Delta I \Delta V \left(1 - \frac{G_n^2 + 4\omega_{osc}^2 C_{rtd}^2}{G_n^2 + 4\omega_{max}^2 C_{rtd}^2}\right) \tag{4.3}$$

Under the approximation, $2\omega_{osc}C_{rtd} > G_n$, equation 4.3 reduces to equation 4.4.

$$P_{max} = \frac{3}{16}\Delta I \Delta V \left(1 - \frac{f_{osc}^2}{f_{max}^2}\right) \tag{4.4}$$

The maximum output power is proportional to the ΔI. A device with larger area and hence a larger ΔI is required to obtain an increase in the output power. However, as will be seen in the next section, constraints are placed on the maximum allowable G_n of the RTD for obtaining stability conditions in the biasing circuit. Since G_n of the RTD is directly proportional to ΔI (RTD area), this also implies a limitation on ΔI. Hence, a limitation exists on the maximum output power of the RTD. Since the stability requirements place constraints on G_n, a direct relationship between G_n and P_{max} will be more intuitive. P_{max} is therefore reexpressed in terms of G_n as in equation 4.5.

$$P_{max} = \frac{1}{8}G_n \Delta V^2 \left(1 - \frac{f_{osc}^2}{f_{max}^2}\right) \tag{4.5}$$

4.3 Constraints On Maximum Power

In the previous section, the maximum power achievable from an RTD was derived as a function of G_n (area). In this section, the origins of DC bistability and parasitic bias circuit oscillations are explained. Conditions required for suppressing DC bistability and parasitic bias circuit oscillations are then derived. The

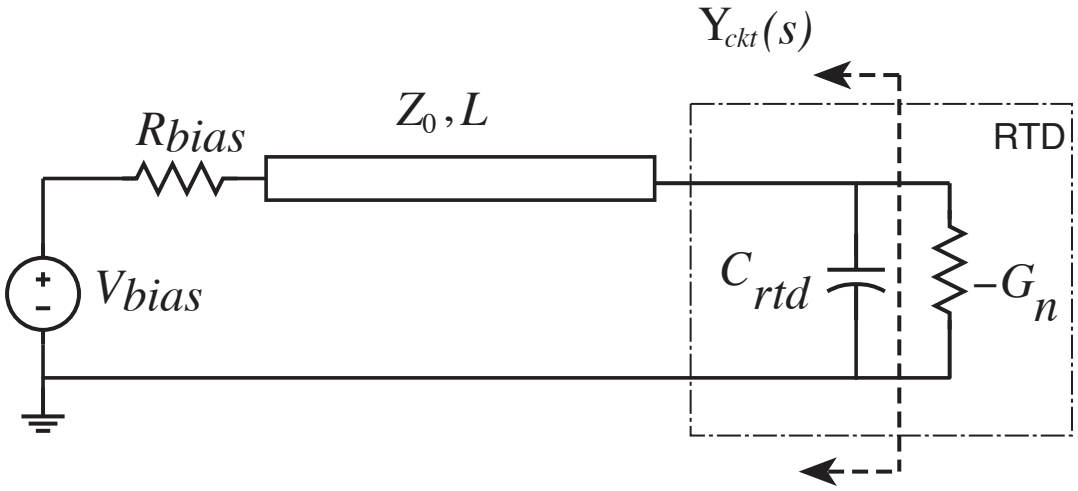

Figure 4.4: The biasing circuit of an RTD showing a voltage source of output resistance R_{bias} and the connecting wires modeled as a transmission lines of impedance Z_0 and length L. These along with the RTD parasitic capacitance C_{rtd}, present an admittance $Y_{ckt}(s)$ to the RTD negative conductance G_n.

stability conditions reduce to a maximum allowable G_n for the RTD. These conditions are then reduced to the maximum achievable power for an RTD oscillator with given biasing circuit elements.

The origins of DC bistability and parasitic bias circuit oscillations are explained with the help of a schematic (figure 4.4) showing the biasing circuit of an RTD to bias the device in the NDR region with an external voltage source of output resistance R_{bias}. The external voltage source is connected to the RTD by long wires which can be modeled as transmission lines of characteristic impedance Z_0 and length L. The velocity of propagation for electromagnetic waves in this transmission line is represented by v. The biasing circuit presents a variety of admittances at the RTD terminals depending on the values of R_{bias}, Z_0, L and v. The equivalent circuit consisting of the biasing circuit elements lumped with the RTD parasitic elements present an admittance $Y_{ckt}(s)$ to the RTD negative conductance G_n. Defining all the complex frequencies $s_i = \sigma_i + j\omega_i$ at which $Y_{ckt}(s) = G_n$, a necessary and sufficient condition for stability is that $\sigma_i < 0$. From this, a sufficient condition for stability is that the real part of the admittance $Y_{ckt}(j\omega)$, $G_{ckt}(j\omega) > G_n$ at the frequency ω. This implies that the net admittance $Y_{ckt}(j\omega) - G_n$, at the terminals of the RTD negative resistance should have a positive real part at all frequencies where stability is required. Therefore,

depending on the admittance presented by the biasing circuit to the RTD, DC bistability or parasitic bias circuit oscillations could arise.

4.3.1 DC Bistability

DC bistability is observed while biasing the RTD in the NDR region. This is illustrated with the help of figure 4.5. Since the RTD voltage is a multivalued function of the RTD current, the load line could intersect the RTD I-V characteristics at more than one point depending upon its slope. The central crossing is unstable and the DC bias point will not stay in the NDR region. The bias conditions are thereby upset. DC bistability is often observed experimentally while biasing the RTD in the NDR region with a voltage source of finite output resistance R_{bias}. If the load line intersects the RTD I-V curve at more than one point, the DC bias switches to the points in the PDR region. Therefore, the loadline should be such that it intersects the RTD I-V characteristics at only one point. This is ensured if the magnitude of the slope of the load line ($1/R_{bias}$) is larger than the magnitude of the slope of the RTD I-V characteristics at the bias voltage (G_n). This condition translates to $1/R_{bias} > G_n$. For a given R_{bias}, the maximum RTD conductance G_n that can be chosen is $1/R_{bias}$. Since G_n is proportional the RTD area, the requirement for DC stability also places a constraint on the RTD area. For DC stability, the maximum output power is therefore limited to $P_{max} = (\Delta V^2/8R_{bias})(1 - f_{osc}^2/f_{max}^2)$. Therefore, a voltage source with a very low output resistance R_{bias}, is necessary. Ideally, a voltage source with the zero output resistance is required to eliminate this constraint on G_n. However, typical external biasing voltage sources have a finite output resistance R_{bias}. Therefore, the constraints imposed by DC stability requirements are important.

4.3.2 Parasitic Bias Circuit Oscillations

DC stability alone is not sufficient, as the biasing circuit may be unstable at frequencies other than f_{osc}. These instabilities arise due to impedance transformation of R_{bias} through the connecting wires. These lead to parasitic bias circuit oscillations. These are often observed while measuring the DC characteristics of the RTD in the NDR region. Wiggles seen in the NDR region while obtaining DC characteristics are a signature of these parasitic bias circuit oscillations [13]. Therefore, adequate care is necessary to also ensure stability at all frequencies where the parasitic bias circuit oscillations need to be suppressed.

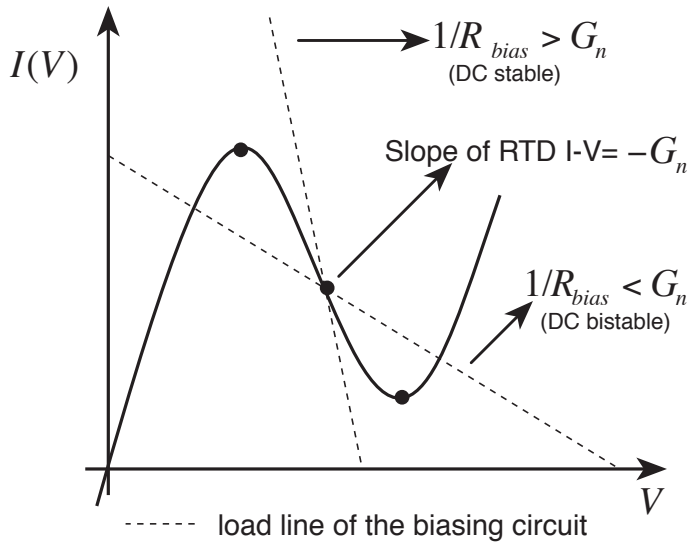

Figure 4.5: RTD I-V characteristics to illustrate bistability. If the load line corresponding to the external biasing voltage source intersects the RTD I-V characteristics at more than one point, DC bistability can occur.

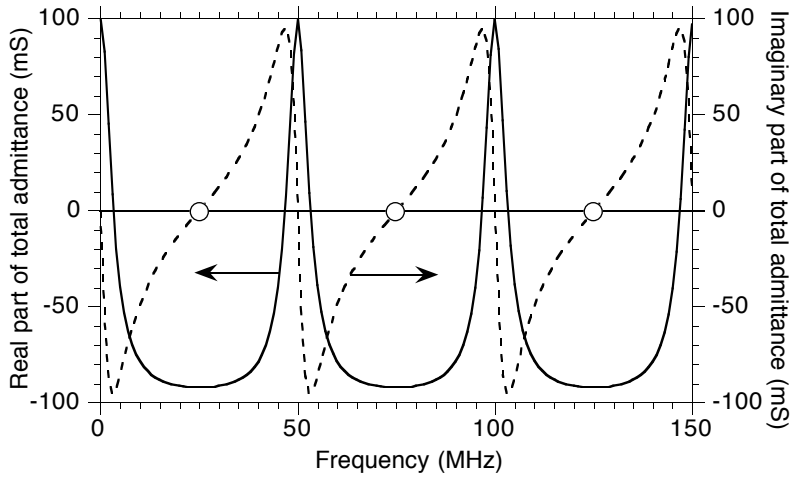

Figure 4.6: Real and imaginary parts of total admittance $Y_{ckt}(j\omega) - G_n$ at the RTD terminals for typical biasing circuit element values. Oscillations can occur at frequencies where the imaginary part goes to zero and the real part has a net negative value as indicated by circles on the graph.

Impedance transformation of R_{bias} occurs through the connecting wires which have been modeled as transmission lines of characteristic impedance Z_0 and length L. If $Z_0 < R_{bias}$, then the real part of admittance varies between a minimum value of $1/R_{bias}$ and a maximum value of R_{bias}/Z_0^2 at the RTD terminals. Here, the worst case for instability occurs when the real part of the admittance is $1/R_{bias}$. Therefore, the conditions for suppression of parasitic oscillations are the same as the requirement for DC stability, $1/R_{bias} > G_n$ which ensures that the total admittance at the RTD terminals has a net positive real part. For a given R_{bias}, the maximum allowed G_n is therefore $1/R_{bias}$. However, unlike the DC stability case, reducing R_{bias} to increase the maximum allowable G_n is not sufficient. A simultaneous reduction of the connecting wires transmission line impedance ($Z_0 < R_{bias}$) is also required. This is not a very practical solution as transmission lines of characteristic impedance $Z_0 < 20\ \Omega$ are difficult to realize. The maximum allowable G_n is therefore limited to Z_0, limiting P_{max} to $\Delta(V^2/8Z_0)(1 - f_{osc}^2/f_{max}^2)$

In a more practical situation, $Z_0 > R_{bias}$ and this presents a more difficult case. The real part of admittance presented to the RTD varies between a minimum value of R_{bias}/Z_0^2 and $1/R_{bias}$. In order to ensure a positive real part in the total admittance at the RTD terminals, the maximum allowable G_n should be limited to R_{bias}/Z_0^2. This limits $P_{max} = (\Delta V^2 R_{bias}/8Z_0^2)(1 - f_{osc}^2/f_{max}^2)$. Since $R_{bias} < Z_0$ for this case, this is the most severe upper bound on the maximum RTD output power.

This case is also illustrated in figure 4.6 where typical values are considered for plotting real and imaginary part of total admittance $(Y_{ckt}(j\omega) - G_n)$. A transmission line with impedance of 25 Ω, length of 1 m and a propagation velocity of 10^8 m/s are chosen with an RTD whose negative conductance G_n, is 200 mS and has a parasitic capacitance C_{rtd} of 20 fF. The RTD is biased with a voltage source of R_{bias} =3.33 Ω. For these bias circuit element values, DC stability is ensured. But the net admittance has negative real part at other frequencies due to impedance transformation. Conditions for oscillations are satisfied at frequencies where the imaginary part goes to zero and the real part has a net negative value. These frequencies are indicated by circles on the graph. Low frequency parasitic oscillations therefore can occur in the bias circuit. These resonances which occur when L is an odd multiple of $\lambda/4$ must be avoided if the parasitics oscillations need to be suppressed.

One way to avoid these resonances is to set $Z_0 = R_{bias}$. In this case, there is no impedance transformation as the RTD sees an impedance of $R_{bias}(= Z_0\ )$ at all frequencies. However, the lowest R_{bias} that could be chosen is limited by the

lowest practically realizable transmission line ($Z_0 = 20\ \Omega$). There is yet again the same upper limit on the maximum allowable G_n of the RTD and thus on output power. This limit is $P_{max} = (\Delta V^2/8Z_0)(1 - f_{osc}^2/f_{max}^2)$.

The other option is to shunt the RTD with a bias stabilizer of very low output impedance at a distance of $\approx \lambda_{osc}/4$ from the RTD. The bias stabilizer sets the DC bias voltage required to bias the RTD in the NDR region while its low output impedance isolates the RTD from the impedances of the external biasing circuit elements. The admittance seen at the RTD terminals is determined by the low value of output impedance of the bias stabilizer and not by the biasing circuit element values. The first condition for resonance occurs at approximately f_{osc}, when this low output impedance is transformed to a high impedance at the RTD terminals. Therefore, the lowest frequency at which oscillations can occur is f_{osc}. By this arrangement, the low frequency parasitic bias circuit oscillations are eliminated. Therefore, the constraints on maximum allowable G_n for suppressing DC bistability and parasitic bias circuit oscillations are eliminated. The output power of the RTD can be increased by arbitrarily choosing a large area RTD with a large G_n. The solution therefore is to provide a low-impedance bias stabilizer at a distance of $\lambda_{osc}/4$ from the RTD. At submm-wave frequencies, $\lambda_{osc}/4$ is of the order of 100 μm. The low-impedance bias stabilizer must be on the same wafer as the RTD. The proposed bias stabilization scheme demands a on-wafer low-impedance bias stabilizer.

4.4 Schottky-diode Bias Stabilizer

Several solutions are possible to obtain a on-wafer low-impedance bias stabilizer. The simplest and crudest solution is to shunt the RTD by a low value of resistance located at a distance $\lambda_{osc}/4$ from the RTD. The value of the resistance should be chosen ($< 1/G_n$) such that the conditions for suppression of DC bistability are satisfied. However, with such a scheme the stabilizer must draw a substantial DC current when biased at the voltages corresponding to the RTD NDR region (figure 4.7 (a)). This is highly undesirable for circuit efficiency. Therefore, a device with a low output resistance and yet drawing smaller current than a resistor is desired.

A forward biased Schottky-diode shunting the RTD at a distance of $\lambda_{osc}/4$ can function as a more efficient bias stabilizer. Since the Schottky-diode is connected in parallel with the RTD, the DC voltage across the RTD is fixed by the voltage across the Schottky-diode. An ideal Schottky-diode with no parasitic series resistance has I-V characteristics that have exponential dependence of current

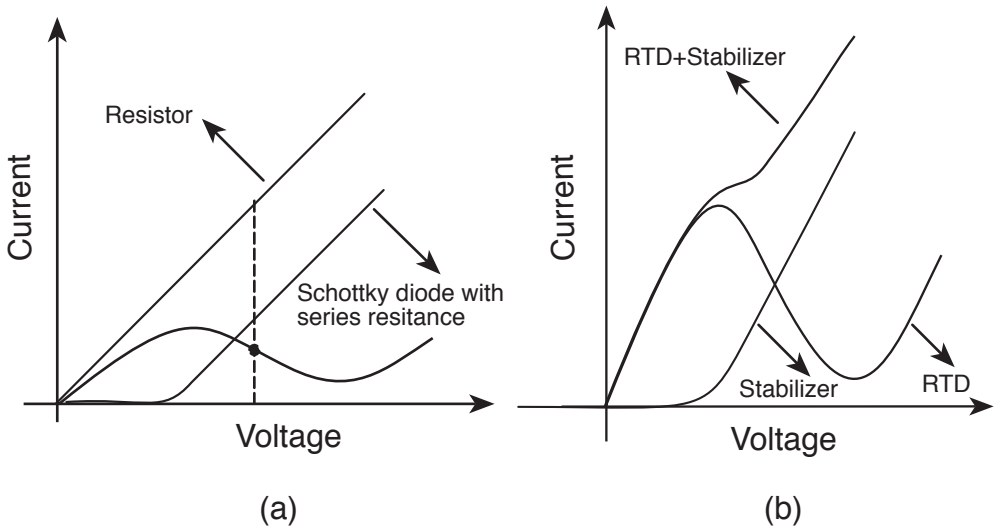

Figure 4.7: (a) A Schottky-diode with series resistance will draw less current than a resistance alone to satisfy conditions of DC stability. (b) The sum of the RTD current and the stabilizer diode current should not have any net NDR region if conditions of DC stability are satisfied over the entire NDR region of the RTD.

on applied voltage (equation 4.6).

$$I_{stab} = I_0(e^{V_{stab}/V_T} - 1) \tag{4.6}$$

Beyond the turn-on voltage, the current rises steeply. So, the voltage across the Schottky-diode is essentially clamped at its turn-on voltage. The slope of the I-V characteristics is $G_{stab} \approx I_{stab}/V_T$ where $V_T \approx 25$ mV at room temperature. This slope is the also the output conductance of the Schottky-diode bias stabilizer. By designing the stabilizer such that the turn-on voltage of the Schottky-diode is just below the peak voltage of the RTD, the conditions for stability can be established over the entire NDR region by choosing an appropriate bias stabilizer current such that $G_{stab} > G_n$ of the RTD over the entire NDR region.

The Schottky-diode bias regulator while highly desirable in the case of precise component tolerances, has several limitations in the presence of the component variability associated with a research integrated circuit process. Because of an exponential dependence of current on bias voltage, the stabilizer will draw a very large currents if the DC bias voltage is increased even by few 10's of mVs beyond the turn-on voltage. The turn-on voltages of the RTD and the Schottky-diode must be precisely matched. Additionally, in building oscillator arrays, many bias stabilizers will be connected in parallel. This results in thermal instability in current partitioning between parallel Schottky-diodes. The Schottky-diodes will be destroyed.

To avoid both current partitioning ("current hogging") problem and to obtain freedom to change the bias voltage in the NDR region, it is desirable to add some series resistance to the Schottky-diode bias stabilizer. The series resistance gives a finite slope to the I-V characteristics of the stabilizer (figure 4.7(a)). Due to the finite series resistance, the small signal conductance of the stabilizer depends on the value of this series resistance. Depending on the G_n of the RTD, the series resistance of the diode can be appropriately chosen. Therefore, the freedom to make G_n as large as possible exists. Therefore, a forward biased Schottky-diode with an appropriate series resistance can function as a on-wafer bias stabilizer. This consumes less current than just a shunt resistor alone.

The Schottky-diode should have a turn-on voltage that is just below the RTD peak voltage, and the current should be series-resistance dominated beyond the turn-on voltage. The series resistance should be chosen such that it is sufficiently low for RTD stability over the entire NDR region. Equivalently, the sum of the RTD current and the stabilizer current should not have a net NDR region. The shunt combination of the RTD and the stabilizer will then exhibit neither DC

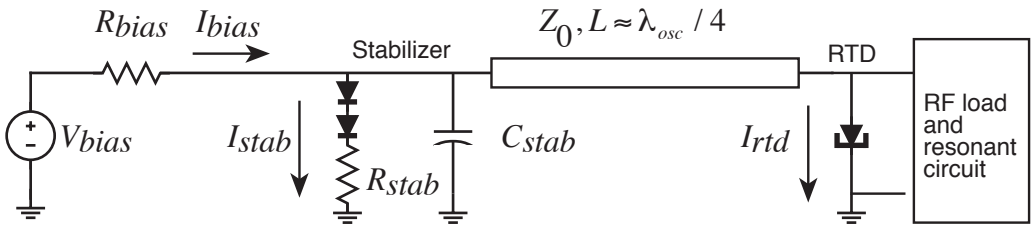

Figure 4.8: Proposed bias stabilization scheme for submm-wave RTD oscillators. The RTD is shunted by a low-impedance bias stabilizer located at a distance of $\lambda_{osc}/4$ from the RTD.

bistability nor parasitic bias circuit oscillations (figure 4.7(b)). The penalty for RTD bias stabilization is that the efficiency is decreased by the ratio $I_{rtd}/(I_{rtd} + I_{stab})$.

4.5 Bias Stabilization Implementation

The bias stabilization implementation is shown in figure 4.8. It consists of an RTD shunted by a low-impedance bias stabilizer placed within a distance of $\lambda_{osc}/4$ from the RTD. The bias stabilizer consists of one or more Schottky-diodes connected in series in addition to a series resistance R_{stab}. Multiple Schottky-diodes may be necessary if the peak voltage of the RTD is greater than twice the turn-on voltage of the Schottky-diode. The Schottky-diodes are connected in series to engineer the total turn-on voltage to be just less than the peak voltage of the RTD. If the dominant term in the output resistance of the bias stabilizer is the series resistance R_{stab}, then at DC, the output resistance of the external biasing circuit and the bias stabilizer seen at the RTD terminals is $R_{stab} \parallel R_{bias}$. DC stability is ensured if $1/R_{stab} > G_n$. A large capacitor C_{stab} also shunts the RTD with an ac short circuit at frequencies other than DC. This ensures that the bias stabilizer does not degrade the oscillator Q at f_{osc}. At f_{osc}, the low-impedance of the bias stabilizer is transformed to a high impedance at the RTD terminals and the RTD is decoupled from the bias stabilizer and the external biasing circuit. If a proper RF load is chosen such that instability conditions exist at f_{osc} in the RF load and the resonant circuit, then the oscillations can be ensured at f_{osc} in the RTD circuit.

At submm-wave frequencies, $\lambda_{osc}/4$ is of the order of 100 μm and hence the low-impedance bias stabilizer (Schottky-diodes and capacitor C_{stab}) must

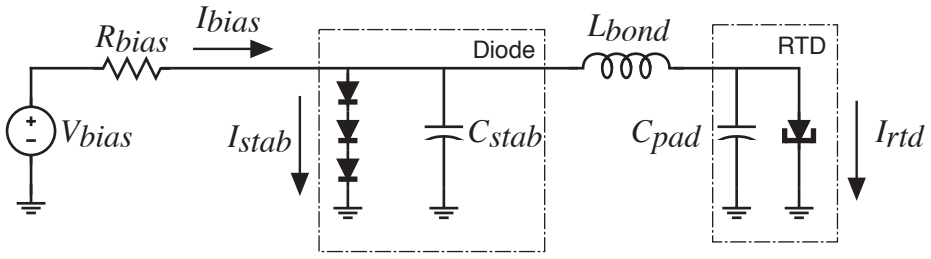

Figure 4.9: Circuit schematic of a microwave oscillator employing the bias stabilization scheme. A low-impedance bias stabilizer is located very close to the RTD which is decoupled from the RTD at the design frequency of oscillation.

be on the same wafer as the RTD. This requirement complicates the oscillator fabrication. The RTD area can be chosen independent of the external biasing circuit elements provided that the output conductance of the bias stabilizer is made larger than the RTD negative conductance, G_n for DC stability.

4.6 Hybrid Oscillator

In order to demonstrate the bias stabilization technique, a hybrid oscillator was constructed. The hybrid oscillator was designed, fabricated and tested at 6.9 GHz. The circuit is shown in figure 4.9. A GaAs SRTD [35] is ribbon bonded to 3 Schottky-diodes connected in series by a bondwire of 6 nH inductance. The 3 series-connected Schottky-diodes and the shunt capacitor C_{stab} function as a low-impedance bias stabilizer located close to the RTD. The parallel combination of the RTD and the diodes is DC stable, exhibiting only a very small net negative resistance region (figure 4.10). The RTD can be biased anywhere in the NDR region without bias circuit instability. Given the hybrid assembly, the RTD is shunted by a 35 fF bond pad capacitance C_{pad}. This forms a parallel resonant circuit with the bondwire inductance at a frequency f_{osc} given by equation 4.7.

At this resonant frequency, the low-impedance bias stabilizer is decoupled from the RTD. In order to ensure that oscillations occur, the conditions for instability need to be satisfied at the desired frequency f_{osc}. In this experiment, the RF load is a spectrum analyzer that is coupled to the RTD through a small capacitance formed by placing a microwave probe a few μm above the RTD. Oscillations were observed at 6.9 GHz (figure 4.11). The bias stabilization technique is thereby demonstrated.

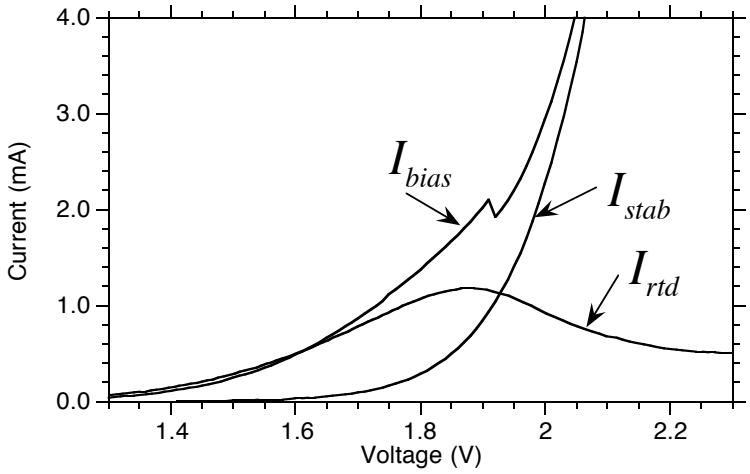

Figure 4.10: DC characteristics of the RTD, stabilizer (diodes) and their shunt combination after ribbon bonding. The total current shows very little negative resistance region indicating that the problem of DC bistability does not exist for the shunt combination.

$$f_{osc} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{bond} C_{pad}}} \tag{4.7}$$

4.7 On-Wafer Schottky-diode

The bias stabilization technique demands a on-wafer Schottky-diode bias stabilizer for submm-wave oscillators. In the GaAs SRTD process [26], a Schottky-diode is easily realized by etching away the space-charge region, barriers and quantum-well and subsequently depositing Schottky-contact metal onto the emitter layer. This would give a Schottky-diode with a turn-on voltage of approximately 0.7 V. Using 2 or 3 diodes in series, the Schottky-diode turn-on voltage could be engineered to be just below the peak voltage of the GaAs SRTD. Unfortunately, in the InGaAs SRTD process, a similar approach would give a Schottky-diode with a turn-on voltage of approximately 0.1−0.2 V. 5 to 7 series-connected Schottky-diodes would be required to obtain a turn-on voltage equal

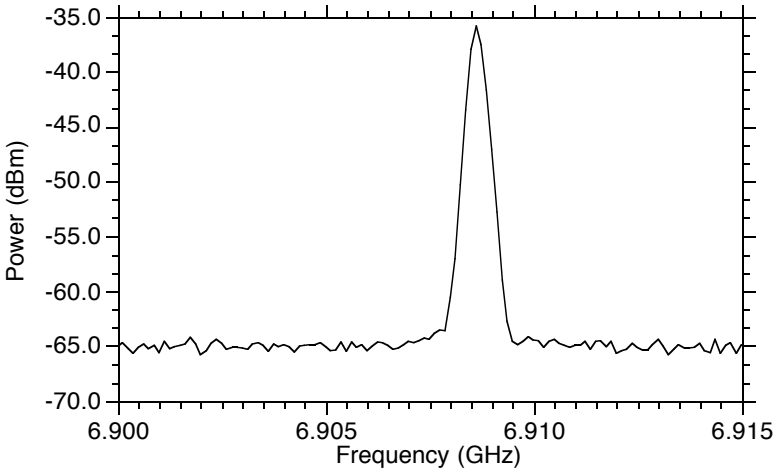

Figure 4.11: RF spectrum of the hybrid oscillator showing oscillations at 6.9 GHz close to the design f_{osc}.

to the $\approx$ 1.0 V peak voltage of the InGaAs SRTDs. The total nkT/qI_{stab} junction impedance would be large and mask layout of submm-wave oscillator would be difficult. A Schottky-diode with a larger turn-on voltage is required.

4.7.1 Graded bandgap AlInAs Schottky-diode

A Schottky-diode with a Schottky-contact to a large band-gap material (AlInAs) and a low series resistance ohmic contact to heavily doped InGaAs would give a Schottky-diode with a large turn-on voltage [36], [37] and a low series resistance. Such a scheme would require a transition from InGaAs to AlInAs in the MBE layer structure. Abrupt transition from InGaAs to AlInAs should be avoided as this would lead to barriers in the conduction band and a associated carrier trapping. The I-V characteristics of the Schottky-diode would be no longer exponential. This would yield poorer ideality factors and a lower turn-on voltage in the Schottky-diode, both of which are undesirable properties for the required Schottky-diode. A smooth transition by grading the InGaAs layers to AlInAs layers is required (figure 4.12).

The effective Schottky barrier height has been measured between 0.65 eV to 0.75 eV for different structures which use AlInAs for enhancing Schottky

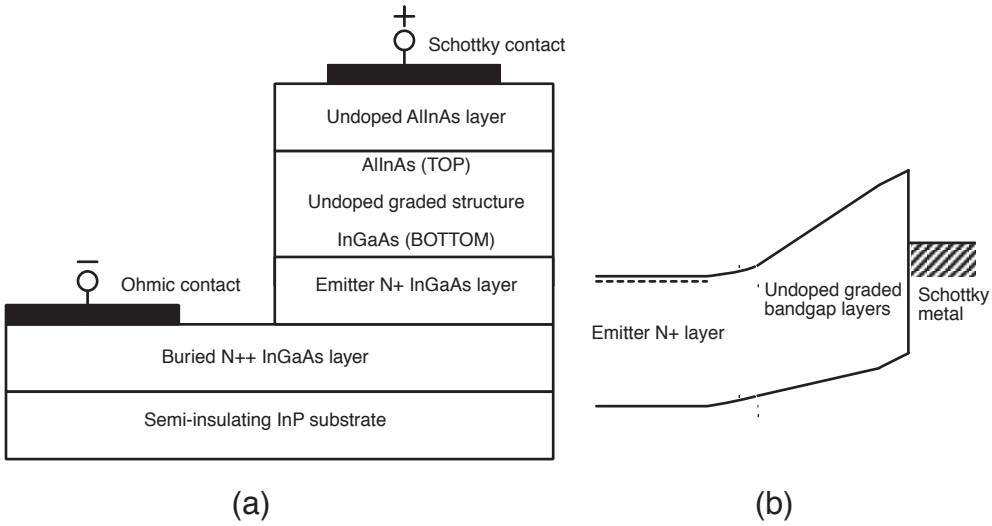

Figure 4.12: (a) Cross-section of a graded bandgap Schottky-diode and (b) band diagram showing the increased barrier height for electrons at the metal semiconductor interface with the large bandgap AlInAs at the surface.

barrier height [36] [37] [38]. Since the grading of composition from InGaAs to AlInAs is employed, the effective bandgap varies spatially between the two extreme values of 0.74 eV (InGaAs) and 1.47 eV (AlInAs). Similarly, the effective Schottky-barrier height can be considered to be spatially graded between 0.2 eV (InGaAs) and 0.82 eV (AlInAs). A layer structure design is therefore necessary incorporating these features.

4.7.2 Layer Structure Design

A layer structure design that allows fabrication of both devices on the same wafer is shown in figure 4.13. This layer structure was grown by MBE. Lattice matched compositions of $In_{0.53}Ga_{0.47}As$ and $Al_{0.48}In_{0.52}As$ were used for the InGaAs and AlInAs layers. The growth conditions for Schottky-diode layers are not as critical as for the SRTD layers which were described earlier.

The Schottky-diode layers were first grown on the semi-insulating InP substrate. The SRTD layers are then grown on top of the Schottky-diode layers. A 1000 Å AlInAs separation layer is grown between the SRTD and the Schottky-diode layers. This separation layer will be utilized during the wet etch process for exposing the Schottky-diode surface layers in regions where the bias stabilizer is required.

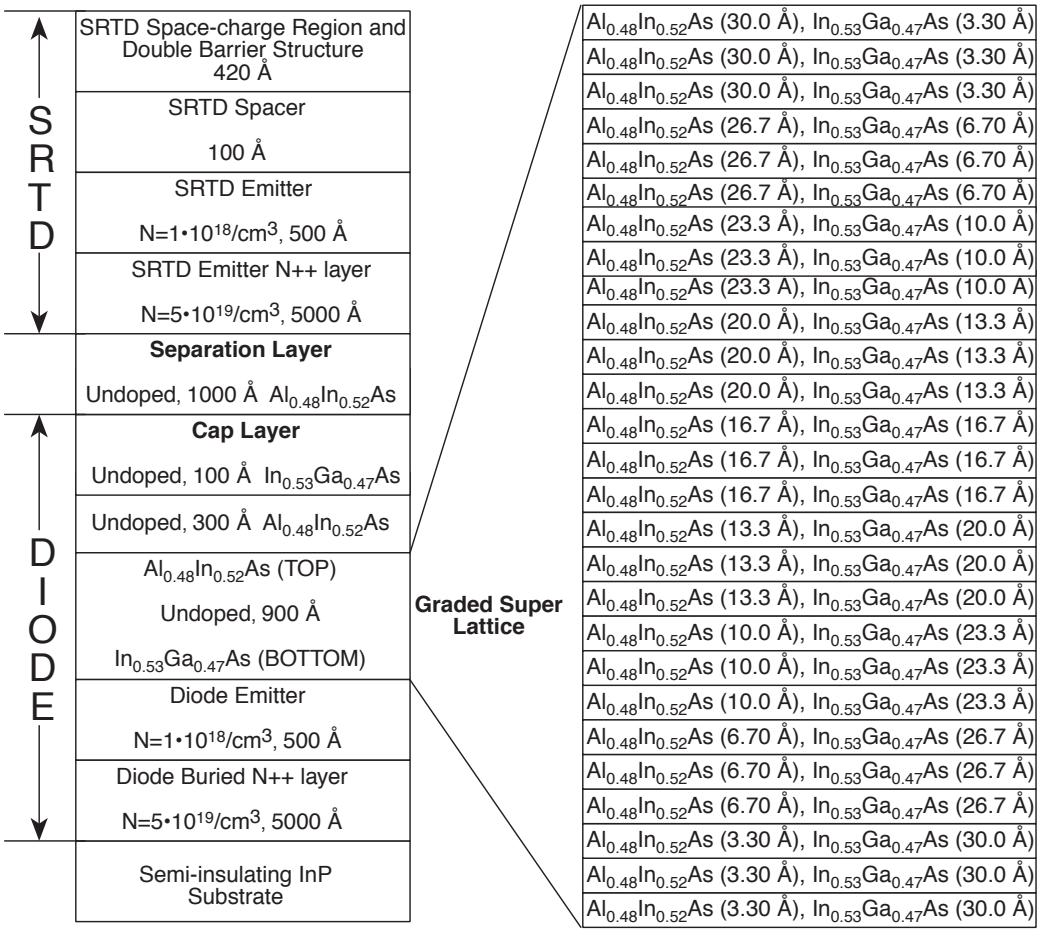

Figure 4.13: Layer structure for fabrication of both SRTD and Schottky-diode on same wafer. The layers for the two devices are separated by 1000 Å undoped AlInAs layer.

The Schottky-diode layers consist of a 5000 Å diode buried N++ layer for obtaining low-resistance access to the Schottky-diode cathode. Above this is a 500 Å emitter layer for the Schottky-diode. A 900 Å undoped graded superlattice structure that achieves smooth transition in composition from InGaAs to AlInAs is grown on top of the diode emitter layer. The design of the graded super lattice structure was developed starting with the designs of earlier workers [36],[37] as an initial structure. Initially, shorter grading distances and larger superlattice periods were used in the InGaAs to AlInAs transition. Schottky-diodes fabricated with such designs of graded super lattice structures yielded DC characteristics with negative resistance regions. The NDR regions are believed to arise due to tunneling through the minibands within the graded superlattice. Therefore, the grading distance was increased to 900 Å and the superlattice period was decreased to 100 Å. This eliminated the negative resistance characteristics.

The final design for the graded superlattice Schottky-diode (figure 4.13) consists of a digital alloy of InGaAs and AlInAs in a 9 period superlattice. Each period has 6 layers alternating between InGaAs and AlInAs. The thickness of each of the InGaAs (or AlInAs) layers in a particular period is the same. But across the periods, the thickness of the InGaAs layers varies from 30.0 Å to 3.3 Å, while the thickness of the AlInAs layers varies from 3.3 Å to the 30.0 Å in the opposite direction. This maintains a total thickness of each period to 100 Å giving a total thickness of 900 Å for the graded super lattice structure. The graded superlattice structure is capped with a 300 Å AlInAs layer and a 100 Å InGaAs layer. A 1000 Å AlInAs separation layer comes on top of the cap layers. In the absence of the cap layers and the separation layer, the wet etch to expose the Schottky-diode layers could reach the graded super lattice region. Depending on the monolayer on which the etch stops, the Schottky-barrier height could be different yielding different characteristics across the wafer. Therefore, the cap layers would ensure that the Schottky-contact is either to the AlInAs cap layer or to the InGaAs cap layer. The plan was to etch the SRTD layers and the AlInAs separation layer and stop on the InGaAs cap layer. The InGaAs cap layer will protect the underlying AlInAs layers from getting oxidized on exposure to air. Just before deposition of the Schottky-metal, the InGaAs cap layer could be etched away if necessary. The SRTD layers located above the 1000 Å AlInAs separation layer follow the designs of the SRTDs with 5ML barriers discussed earlier. The only modification is a thinner SRTD emitter N++ layer to keep the total thickness of the active layers approximately the same as in layer structure with just SRTDs. The MBE growth details are provided in Appendix D.

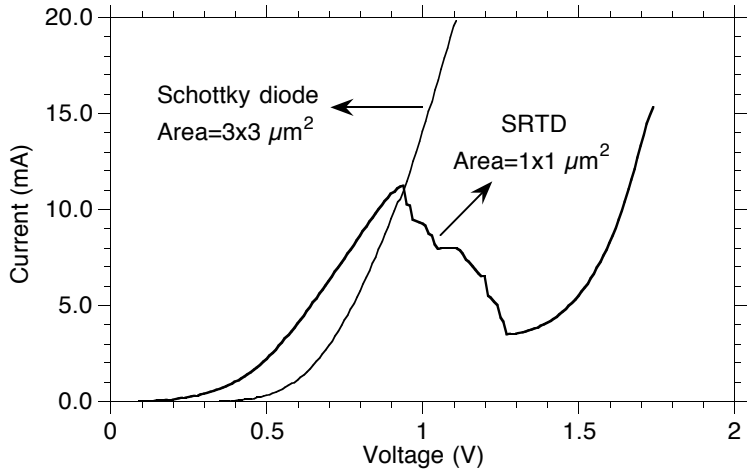

Figure 4.14: DC characteristics of InGaAs SRTD and graded bandgap AlInAs Schottky-diode fabricated on same wafer. The DC measurements of the Schottky-diode indicate that it has desired characteristics to function as a on-wafer bias stabilizer.

4.7.3 DC Characterization

Characterization of this layer structure was carried out by fabricating large area SRTDs and Schottky-diodes on the same wafer using the process described earlier for fabricating large area SRTDs. However, an additional step is required in this characterization, as the SRTD layers must be etched away in regions where the Schottky-diode is required. On one half of the wafer, the Schottky-diode layers were exposed by etching the SRTD layers using a combination of non-selective and selective etching. The details of this etching process will be described later in the fabrication of submm-wave oscillators. Both devices can be now fabricated in the simple 3 mask process used earlier to characterize the SRTD material. Au-Ge-Ni Ohmic contacts to both the N++ layers of the SRTD and the Schottky-diode are formed in the first mask step. The silicon dioxide via patterns define the Schottky contact areas for both the SRTD and the Schottky-diode. With the deposition of Schottky metal, anodes for both the SRTD and the Schottky-diode are defined. The DC characteristics are then obtained for both devices to evaluate the material.

The measured DC characteristics of a nominally 1.0 μm^2 SRTD and a 9.0 μm^2 Schottky-diode are shown in figure 4.14. The SRTD DC characteristics are same as before indicating that addition of the Schottky-diode layers beneath the SRTD has no significant effect on the observed NDR characteristics of the SRTD. The Schottky-diode has a turn-on voltage of ≈ 0.65 V. Two Schottky-diodes in series would give a turn-on voltage that is larger than peak voltage of the SRTD and this would not be feasible for the bias stabilizer. Therefore, a single Schottky-diode should be utilized for the on-wafer bias stabilizer. The graded bandgap AlInAs Schottky-diode has the required larger turn-on voltage and a low series resistance which together make it suitable to function as the on-wafer bias stabilizer. Since the desired DC characteristics were obtained with the layer structure shown in figure 4.13, several 2-inch wafers were grown to stockpile material for the next phase of the project which involves building submm-wave oscillators with the 0.1 μm InGaAs SRTDs.

In this chapter, an inherent problem of RTD oscillators with DC bistability and parasitic bias circuit oscillations was examined. In order to suppress these undesired oscillations, constraints are placed on the maximum RTD area which limit the maximum power from an RTD oscillator. A bias stabilization scheme was proposed which achieves stability at all frequencies below the desired frequency of oscillation without placing any constraints on the maximum RTD area. The proposed scheme was demonstrated with a hybrid microwave oscillator. To extend the bias stabilization principle to submm-wave frequencies a on-wafer bias stabilizer is required. A graded bandgap AlInAs Schottky-diode with 0.65 V turn-on voltage and low series resistance was designed, fabricated and tested. The stage is now set for demonstration of submm-wave oscillators with 0.1 μm InGaAs SRTDs incorporating the proposed bias stabilization technique.

Chapter 5

Circuit Design

Demonstration of submm-wave SRTD oscillators forms the final goal of this project. In this chapter, circuit design of monolithic submm-wave slot antenna coupled SRTD oscillators will be described. The design follows a simple one port negative resistance oscillator approach incorporating the on-wafer bias stabilization to suppress DC bistability and parasitic bias circuit oscillations. While connectors and cables are not available at submm-wave frequencies, power is easily radiated at these frequencies. Therefore, a slot antenna is incorporated into the oscillator circuit for coupling the oscillator output power. Since power from a single-element SRTD oscillator is small, array oscillators are designed. These consist of 2-dimensional arrays of the single-element oscillators, synchronized by the mutual coupling through an external cavity. Biasing of the array oscillators is simplified by the on-wafer bias stabilization technique described in chapter 4. Array oscillators should generate larger power levels than the single-element oscillators.

5.1 Slot Antenna Coupled Oscillator

The circuit schematic for a single-element slot antenna coupled SRTD oscillator incorporating the on-wafer bias stabilization scheme is shown in figure 5.1. It consists of a high f_{max}, 0.1 μm InGaAs SRTD loading the slot antenna at its center. To prevent DC shorting of the SRTD by the ends of a normal slot antenna, large capacitors C_{stab}, shunt the ends of the slot antenna providing a short circuit at RF but an open circuit at DC. The low impedance DC bias stabilizer consisting of a Schottky-diode in series with a resistance R_{stab}, is located at a distance $\approx \lambda_{osc}/4$ from the SRTD.

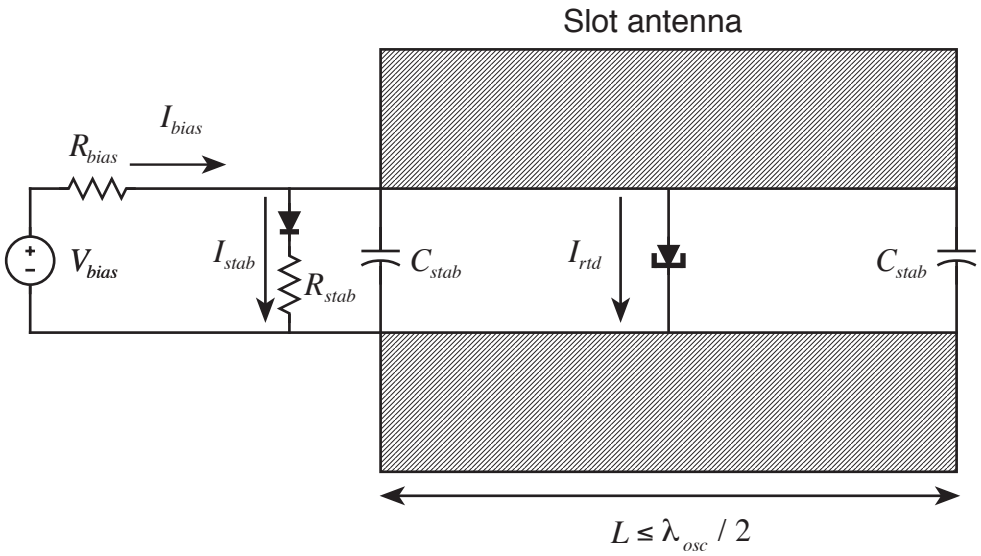

Figure 5.1: Circuit schematic for a single-element slot antenna coupled SRTD oscillator incorporating on-wafer bias stabilization.

By placing the DC bias stabilizer and the capacitors C_{stab} at a distance of $\lambda_{osc}/4$ from the SRTD, the first condition for oscillations occurs at a frequency close to f_{osc}. At frequencies below f_{osc}, the SRTD is shunted by a low impedance consisting of the DC bias stabilizer as well as the large capacitors C_{stab}. The DC bias stabilizer is designed for DC stability such that the DC characteristics of the shunt combination of the SRTD and the bias stabilizer (I_{bias}) has no net NDR region.

The slot antenna is resonant at the design frequency of oscillation f_{osc}. The slot antenna serves both as a resonating and a radiating element. The slot antenna is characterized by its radiation impedance which is the impedance as seen at the center of the slot antenna. This radiation impedance takes into account the interaction of the electromagnetic fields in the slot antenna with the thick substrate. At the resonant frequency, the radiation impedance has only a real part. At this frequency, the SRTD is shunted only by the real part of the radiation impedance of the slot. The combination of the slot antenna and the SRTD will oscillate at the resonant frequency if the net conductance (SRTD's negative conductance + slot antenna's radiation conductance) is negative. Since the SRTD has a finite capacitance, the slot antenna is detuned from its resonant length. The slot antenna is therefore slightly shorter than its resonant length of

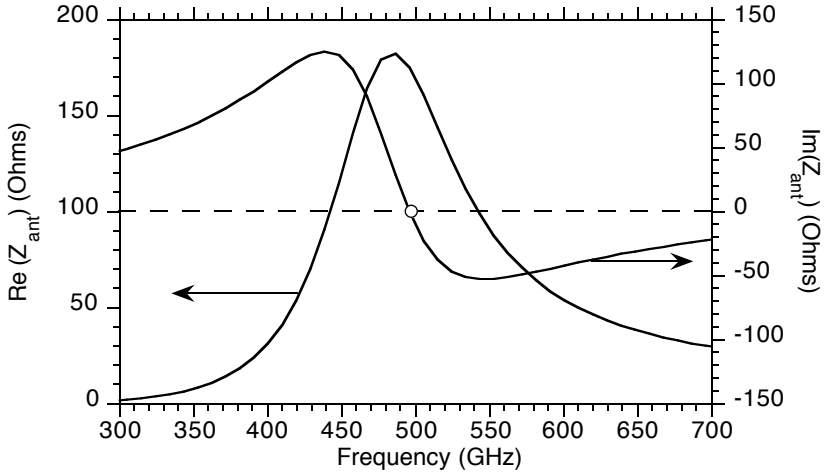

Figure 5.2: Real and imaginary parts of slot antenna impedance as a function of frequency. The rectangular slot dimensions are 114 μm and 5.8 μm. The unloaded slot antenna is resonant at 500 GHz.

$\lambda_{osc}/2$.

This oscillator circuit topology can be easily extended to arrays where the single-element oscillator of figure 5.1 is repeated in rows and columns. The arrays will generate larger power levels through quasi-optical power combining of individual single element oscillators [42]. These oscillator circuits require slot antennas, 0.1 μm InGaAs SRTDs, graded bandgap AlInAs Schottky-diodes, resistors, and capacitors. The slot antenna characteristics have not been discussed so far and hence will be described in detail in the following section.

5.2 Slot Antennas

Monolithic slot antennas can be easily fabricated by depositing metal onto the semi-insulating substrate. The slot antennas are characterized by a radiation impedance. At the resonant frequency, the radiation impedance is purely resistive, representing the losses associated with the radiated power. The slot antenna impedance characteristics were calculated by Dr. Huan-Shang Tsai in Prof. Robert York's research group at UCSB. The finite-difference time-domain (FDTD) and method of moments (MOM) numerical techniques were used [43].

The antenna impedance was calculated in the thick substrate approximation. As the oscillator array is to be placed on ~ 2.3 cm diameter index-matched lens, the approximation is viable. It should be noted that the impedance calculation neglects the reflections at the lens-air interface, and antenna-antenna array coupling effects are ignored. The latter approximation must clearly be revisited. Similar impedance characteristics of the slot antenna were obtained by both FDTD and MOM methods. The impedance characteristics of a slot antenna resonant at 500 GHz is shown in figure 5.2. The antenna is 108 μm long. The width to length ratio is 1 : 20 in all the simulations shown subsequently.

The unloaded slot antenna is resonant when the imaginary part of the antenna impedance is zero. For a slot antenna in free space, the resonance occurs when the slot length is $\lambda_0/2$, where λ_0 is the free space wavelength. For a slot antenna on a substrate, the resonance occurs when the antenna is again one-half of a guide wavelength. To a first approximation, the guide velocity is $c/\sqrt{\epsilon_{r,eff}}$, where c is the velocity of light in free space, while $\epsilon_{r,eff} = (\epsilon_{r,sub} + 1)/2$ is the average dielectric constant of air and the substrate [44]. For a InP substrate ($\epsilon_{r,sub} = 13$), this gives a resonant condition for a slot length of $\approx 0.19\lambda_0$. In strong agreement, the numerical calculation indicates resonance at $L \approx 0.18\lambda_0$.

The slot antenna impedance is purely real at the resonance. Using Booker's duality relationship [44], a first-order estimate can be obtained for the slot antenna radiation resistance. The dual of a slot antenna is the dipole antenna. For antennas suspended in air, Booker's relationship gives the product of impedances of a dipole and a slot to be $Z_{air}^2/4$, where Z_{air} is the impedance of free space. At resonance, the dipole antenna in free space has a 73 Ω resistance. Booker's relationship therefore predicts a 487 Ω radiation resistance for a resonant slot antenna in an $\epsilon_r = 1$ environment. In the presence of the substrate with $\epsilon_{r,sub} = 13$, the slot antenna radiation resistance at resonance is $(487\ \Omega)((1 + \epsilon_{r,sub})/2)^{-1/2} = 184\Omega$. The numerical simulations predict $\approx 180\ \Omega$ radiation resistance. This good agreement between theory and numerical model gives a high confidence in the simulations.

Since the SRTD oscillator circuit is in a shunt configuration, it is more appropriate to describe the slot antenna by its admittance, the reciprocal of the its impedance. From the numerical simulations, a numerical curve fit of the antenna's frequency-dependent admittance is developed (equations 5.1, and 5.2).

$$Re[Y_{ant}] = G_{ant} = 0.35e^{15.487Lf/c} \tag{5.1}$$

$$Im[Y_{ant}] = B_{ant} = -45.57 + 253.87(Lf/c) \tag{5.2}$$

Here, L is the slot length, f is the frequency and c is the velocity of light in free space. These fitted relationships will be now used for the oscillator design.

5.3 Oscillator Circuit Design

In the first design attempt, circuit topology approach was intentionally kept very simple, as the various device models were of unknown accuracy. The primary goal was to obtain the highest possible oscillation frequencies with the 0.1 μm InGaAs SRTD technology.

The various circuit elements of a single element slot antenna coupled RTD oscillator are the 0.1 μm SRTD, Schottky-diode, series resistor R_{stab}, slot antenna and the capacitors C_{stab} at the ends of the slot. Various constraints are imposed on these element values by layout and fabrication considerations. Therefore, oscillator circuits need to be designed accounting for these constraints. The circuit design for a slot antenna coupled oscillator requires choosing the correct device areas for the SRTD and the Schottky-diode, the dimensions of slot antenna, the capacitor and resistor values. Circuits were designed such that the circuit can oscillate only at the design frequency of oscillation, f_{osc}. The primary design conditions are DC stability and RF instability only at f_{osc}. At DC, the circuit consists of the shunt combination of the SRTD and the bias stabilizer. At RF, the equivalent circuit consists of the SRTD in the center of the slot antenna whose ends are shorted by the large capacitors C_{stab}.

To ensure DC stability, the DC characteristics of the shunt combination of the SRTD and the bias stabilizer (I_{bias}) should have no net negative differential resistance. The shunt combination can be then biased by an external circuit without concern for DC bistability or parasitic bias circuit oscillations. This can be ensured if the magnitude of the conductance of the bias stabilizer G_{stab}, is larger than the magnitude of the SRTD conductance, G_n. To permit biasing the SRTD anywhere within its NDR region, the condition $G_{stab} > G_n$, should be satisfied at all bias conditions.

At frequencies near f_{osc}, the oscillator equivalent circuit consists of the SRTD shunted by the antenna admittance Y_{ant}, under the assumption that the capacitors C_{stab} at the ends of the slot antenna can be approximated by ideal short circuits. The SRTD is replaced by its small-signal model. The exact conditions for oscillations are given in the equations 5.3, and 5.4, where Y_{rtd} is the SRTD admittance at its terminals. The frequency of oscillations is determined by equation 5.4, while equation 5.3 is the instability (oscillation) criterion.

$$Re[Y_{ant}] + Re[Y_{rtd}] < 0 \tag{5.3}$$

$$Im[Y_{ant}] + Im[Y_{rtd}] = 0 \tag{5.4}$$

Since the SRTD has an associated parasitic capacitance, $Im[Y_{rtd}] \neq 0$. The slot antenna must provide a significant inductive shunt susceptance to satisfy equation 5.4 at the design f_{osc}. The oscillation frequency is therefore below the slot antenna resonant frequency.

Following the above design procedure, single-element oscillators were designed with target oscillation frequencies in the range of 100 GHz to 1000 GHz in increments of 100 GHz. The design procedure started with specifying the SRTD junction area and then determining (equations 5.3, and 5.4) parameters for other circuit elements. The following subsections will describe first RF design and subsequently DC design.

5.3.1 SRTDs

Prior to oscillator design, the submicron InGaAs/AlAs SRTDs had been fabricated and characterized (chapter 3). While both SRTDs with 5 ML and 6 ML barriers had been characterized, oscillators were designed only with higher f_{max} 5 ML SRTDs. The small-signal model parameters of SRTDs with 5ML barriers as normalized to a unit effective SRTD area are $R_s = 2.2\ \Omega - \mu m^2$, $G_n = 19$ mS/μm^2, $C = 3.0$ fF/μm^2, and $\tau_{qw} = 0.12$ ps.

SRTDs with 5 ML barriers had a peak negative conductance of 19 mS/μm^2, while the slot antenna has a radiation conductance of 5.5 mS at the unloaded resonant frequency. Neglecting the detuning caused by the SRTD capacitance, the minimum SRTD area required to ensure RF instability is $\approx 0.3\ \mu$m^2. Given the 0.2 μm effective Schottky-collector width, the minimum SRTD stripe length required is then 1.5 μm. A minimum SRTD stripe length of 2.0 μm was chosen for circuit design.

Oscillations are ensured if the total circuit admittance has a net negative real part at the f_{osc}. To account for the model uncertainties in circuit design, G_n should exceed G_{ant} by a large margin. This implies choosing an SRTD stripe length much larger 1.5 μm. This low-risk oscillator design strategy carries a penalty. A larger SRTD area also implies a larger SRTD parasitic capacitance C_{rtd}, and hence a larger detuning of the slot antenna from its resonant frequency. At the antenna resonance, the slot antenna admittance is determined with high

Design	A (μm^2)	Length (μm)	G_n (mS)	C_{rtd} (fF)	L_{qw} (pH)	R_s (Ω)
SR2	0.4	2 .0	7.60	1.2	15.8	5.50
SR3	0.6	3.0	11.4	1.8	10.5	3.66
SR4	0.8	4.0	15.2	2.4	7.90	2.76
SR6	1.2	6.0	22.8	3.6	5.26	1.94
SR8	1.6	8.0	30.4	4.8	3.96	1.38

Table 5.1: Small-signal model parameters for the various 0.1 μm SRTDs in the device library. In this table, A represents the effective area which is twice the SRTD junction area.

confidence from simple theoretical relationships. This does not hold true at frequencies far from resonance. Operating too far way from unloaded slot antenna resonant frequency would require accurate numerical models for the slot antenna. The circuit designs would depend critically on the antenna models and this should be avoided as the antenna models have not been experimentally verified at these frequencies. In view of these considerations, a maximum SRTD stripe length of 8.0 μm was chosen.

A library of devices (table 5.1) with stripe lengths of 2.0, 3.0, 4.0, 6.0 and 8.0 μms were thus chosen for SRTD oscillator design. For 0.1 μm InGaAs SRTDs having 5 ML barriers, devices with stripe lengths $>$ 4.0 μm failed due to overheating. Hence, devices with stripe length 6.0 μm and 8.0 μm were realized by connecting two 3.0 μm or 4.0 μm stripe length SRTDs in parallel. The small signal model parameters for the various devices were calculated by appropriately scaling the parameters of a unit effective area device.

5.3.2 Slot Antennas

The dimensions of the slot antenna must be determined for the various designs at different oscillation frequencies. The slot width is set at $L/20$, where L is the slot length. For these parameters, the real and imaginary parts of the slot antenna's admittance are given by equations 5.1, and 5.2. At RF, the oscillator equivalent circuit is shown in figure 5.3.

A design frequency of oscillation f_{osc}, is first chosen. An SRTD is then chosen from the library of devices (table 5.1). The SRTD admittance Y_{rtd} at f_{osc}, is then

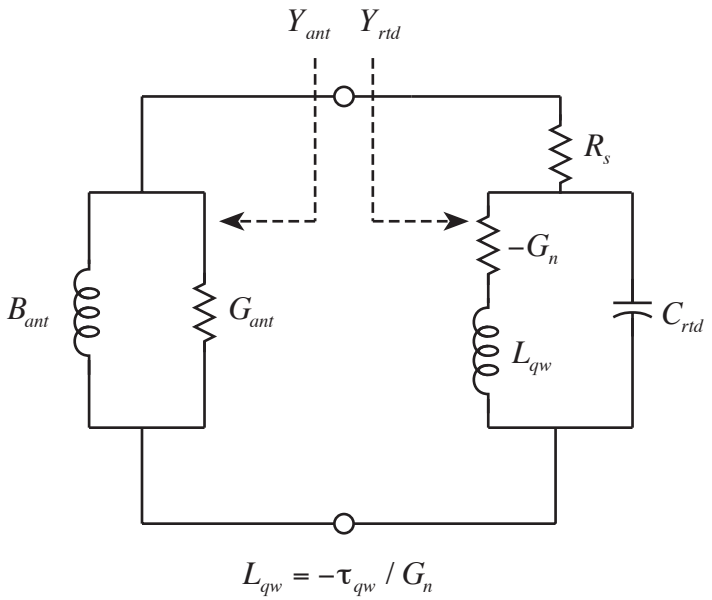

Figure 5.3: At RF, the SRTD is shunted by the slot antenna admittance. The conditions for oscillation depend on the net admittance of the SRTD and the slot antenna.

calculated for the chosen SRTD effective area. The conditions for oscillation at the design frequency are given by equations 5.3, 5.4. Setting the imaginary part of the total admittance (equation 5.4) to zero, the required slot length at the design frequency of oscillation is determined.

Since the SRTD has a parasitic capacitance C_{rtd}, the required slot length will be shorter than its unloaded resonant length. The parasitic capacitance C_{rtd} increases with the SRTD area. The required slot length therefore decreases as the SRTD area is increased. To ensure oscillations, the sum of the SRTD and antenna conductances is calculated (equation 5.3) to verify that it is negative. Increasing the SRTD area gives a design margin through a larger net negative conductance, but also increases the slot antenna detuning.

The design procedure is repeated at other design frequencies and for other SRTDs in the device library. To facilitate design, an Excel spreadsheet was created for automated design calculations. The spreadsheet was used to determine the required slot antenna length as a function of the SRTD junction area employed and as a function of the desired frequency of oscillation.

The results of the design procedure are summarized in table 5.2. More pragmatically, the set of designs can be viewed as a two-parameter bracketing, by

Target f_{osc} (GHz)	SR2 L (μm)	SR3 L (μm)	SR4 L (μm)	SR6 L (μm)	SR8 L (μm)
100	520	512	503	485	467
200	252	243	235	217	200
300	162	153	145	127	110
400	118	110	101	85	68
500	91	83	75	59	–
600	74	66	58	–	–
700	62	54	46	–	–
800	52	45	37	–	–
900	45	38	–	–	–
1000	40	33	–	–	–

Table 5.2: Required slot antenna length L, for different designs with varying SRTD areas and target oscillation frequencies.

the SRTD area and the slot length, of a basic oscillator design. This bracketing ensures that some of the circuits will oscillate, despite considerable uncertainties in the SRTD and slot antenna models, and the unknown effects of layout parasitics. The two-parameter bracketing accounts for all possible oscillator designs within the constraints imposed by fabrication and layout issues.

As the target oscillation frequencies increase, the slot length decreases. However, the total SRTD size inclusive of its active and passive mesas does not decrease. The SRTD dimensions therefore become a significant fraction of the slot antenna length. For the highest-frequency oscillators, the layout of the slot antenna coupled oscillator thus fails to conform to a simple slot antenna model. Significant layout parasitics then exist and the simple models used in circuit design may not be applicable. The two-parameter bracketing provides a complete coverage of all oscillator designs possible within the available technology and the stipulated circuit topology. As can be seen from table 5.2, the detuning of the slot length is very large at the higher frequencies and therefore some of the designs at higher frequencies with larger SRTD areas were discarded. The discarded designs are indicated by a $-$ in the table 5.2.

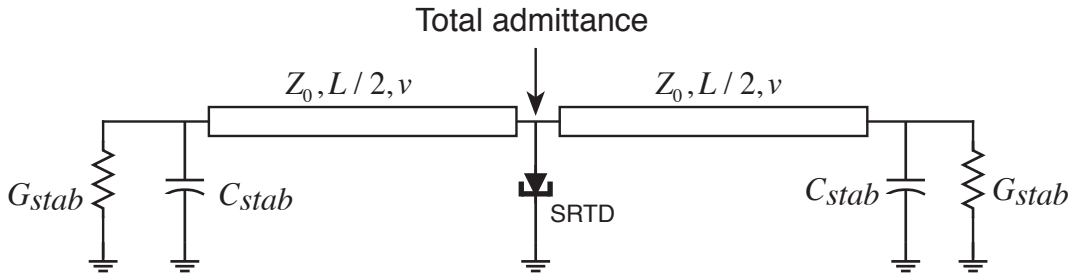

Figure 5.4: The effect of reducing the capacitance of C_{stab} is examined by modeling the slot antenna as two parallel transmission lines of impedance Z_0 and velocity of propagation v.

5.3.3 Capacitors

The capacitors at the ends of the slot antenna C_{stab} should have nearly zero impedance at f_{osc}. To simplify the design procedure, these capacitors were so treated during the initial circuit design. This approximation must be now examined.

Large capacitors will require large mask layout areas. Given a 0.6 fF/μm^2 capacitance per unit area for a standard 1000 Å silicon nitride MIM capacitor process, a 400 fF capacitor would be $\approx$ 26.0 μm $\times$ 26.0 μm. If this capacitor is chosen to terminate the ends of a 500 GHz slot antenna design, the two capacitors on either side occupy $\approx 2/3^{rds}$ of the $\approx$ 75 μm slot antenna length. Therefore, the capacitors cannot be treated as a lumped elements in the circuit design. Accurate circuit design would therefore require a 2-dimensional distributed model for the capacitor. The effect of reducing the capacitor dimensions was examined to determine the smallest value of capacitance that would work in the circuit without any performance degradation.

A slot antenna coupled oscillator with a slot length of 75 μm was chosen for this study. At frequencies close to the design frequency of oscillation, the slot antenna can be modeled approximately as two parallel shorted transmission lines of impedance Z_0, length $L/2$, and velocity of propagation v (figure 5.4). The effect of radiation resistance is not accounted in this simple model. The reactance at the center of the slot is the sum of the reactances of the two shorted transmission lines.

Before determining the effects of the capacitors C_{stab}, the unknown quantities Z_0 and v must be determined. This is done by equating the reactance and its derivative with respect to frequency, to the corresponding quantities of the slot

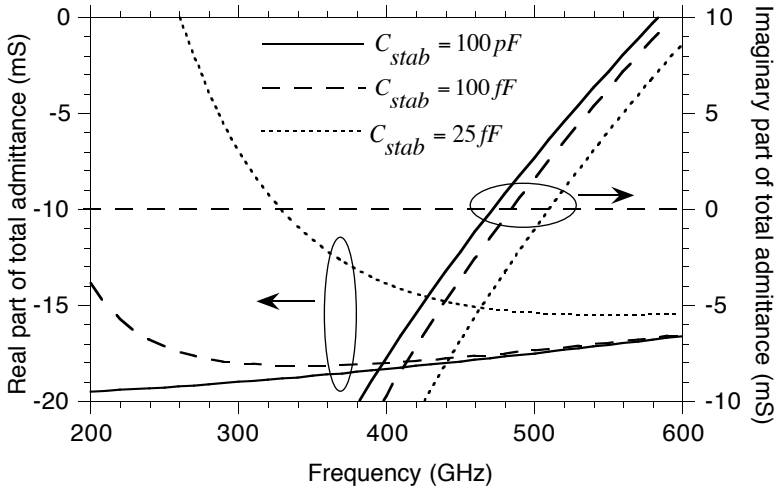

Figure 5.5: The real and imaginary parts of total admittance at the center of slot antenna inclusive of the SRTD admittance for different values of C_{stab}.

antenna as obtained by the numerical simulation. For the transmission line model, the relations are given below in equations 5.5, 5.6. For the 75 μm slot antenna at 500 GHz, the values of Z_0 and v were determined as 88.3 Ω and 1.15 $\times 10^8$ m/s.

$$Im[Y_{ant}] = -\frac{2}{Z_0} \cot \frac{\pi f L}{v} \tag{5.5}$$

$$\frac{\partial Im[Y_{ant}]}{\partial f} = \frac{2}{Z_0} \csc^2 \frac{\pi f L}{v} \tag{5.6}$$

The effect of a finite capacitance value for the capacitor C_{stab}, is then examined for this design by calculating the total admittance at the center of the slot antenna, inclusive of the SRTD's admittance. A SRTD with an effective area of 1.0 μm^2 is assumed to be loading the slot antenna at its center. Three capacitance values of C_{stab} are chosen (25 fF, 100 fF and 100 pF), where the 100 pF is closest to the ideal case. The effect of the DC bias stabilizer is included by the bias stabilizer conductance G_{stab}, on either side of the slot antenna. A plot of real and imaginary parts of the total admittance is shown in figure 5.5. From this analysis, it is clear that the resonant frequency increases as C_{stab} is

Target f_{osc} (GHz)	C_{stab} (fF)	Dimensions (μm$\times\mu$m)
100	540	30×30
200	291	22×22
300	195	18×18
400	135	15×15
500	101	13×13
600	86	12×12
700	73	11×11
800	60	10×10
900	60	10×10
1000	60	10×10

Table 5.3: Capacitance values and dimensions of the capacitor C_{stab}, at different target oscillation frequencies.

decreased. Further, the total net negative circuit conductance decreases as C_{stab} is decreased. This latter effect arises because G_{stab} now is partially loading the SRTD at f_{osc}. If this loading is very large, the oscillations will be suppressed. The loading effect also represents the power lost to G_{stab} at f_{osc}, with the oscillator power distributed between the radiation conductance and G_{stab}. Therefore, the loading effect of G_{stab} should be minimized. As can be seen from figure 5.5 for a 500 GHz oscillator, a value of 100 fF for C_{stab} is sufficient to minimize the loading effect of G_{stab}. The dimensions of this capacitor are 13.0 μm×13.0 μm. These capacitor dimensions are reasonable in view of the required 75 μm slot antenna length. The capacitor values for other design frequencies were scaled proportionally to give the same value of reactance at all oscillation frequencies. The capacitor values and dimensions of the MIM capacitors assuming a 0.6 fF/μm^2 are summarized in table 5.3.

5.3.4 Bias Stabilizers

The design of DC bias stabilizer for the slot antenna coupled SRTD oscillator will be described. Graded bandgap Schottky-diodes were characterized in chapter 4. The measured DC characteristics of these diodes will be used for designing the bias stabilizer. Connecting two Schottky-diodes in series would give

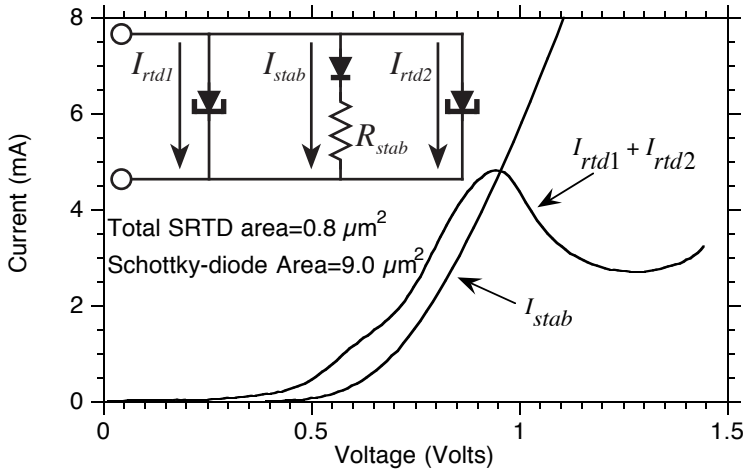

Figure 5.6: DC characteristics of SRTDs and Schottky-diode with 25 Ω series resistance. The bias stabilizer is shared by two neighboring SRTDs.

a turn-on voltage greater than the SRTD peak voltage. Hence, two Schottky-diodes connected in series cannot function as a bias stabilizer. Therefore a single Schottky-diode in series with a resistance R_{stab} is chosen as the bias stabilizer.

To minimize the layout parasitics, one bias stabilizer is shared by two neighboring SRTDs. The bias stabilizer design will be illustrated with an example. The DC characteristics of the two SRTDs (2 SR2 devices in parallel) and the bias stabilizer are shown in figure 5.6. The total current through the SRTDs is represented by $I_{rtd1} + I_{rtd2}$, while the current through the bias stabilizer is represented by I_{stab}. The total SRTD effective area is 0.8 μm^2. The measured DC characteristics of a 0.4 μm^2 SRTD are scaled by a factor of two to account for the two neighboring SRTDs connected in parallel. A Schottky-diode with 9.0 μm^2 area is chosen for the bias stabilizer. A 25 Ω series resistance R_{stab}, is added to the Schottky-diode to both prevent bias circuit thermal runaway and to allow biasing of the SRTD anywhere within its NDR region without drawing excessive stabilizer current (figure 5.6).

DC stability can be verified by measuring the I-V characteristics of the shunt combination of the SRTDs and the bias stabilizer. Since the SRTDs and the Schottky-diode were fabricated on different wafers and since the fabricated Schottky-diode did not include the series resistance R_{stab}, it was not possible

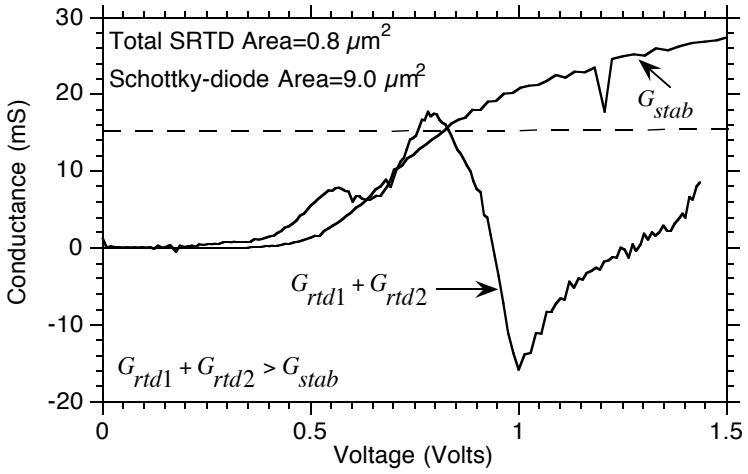

Figure 5.7: DC stability can be verified from the conductance of the bias stabilizer and the SRTDs. The shunt combination is DC stable if the conductance of the bias stabilizer lies above the dotted line.

to obtain the DC characteristics of the shunt combination. DC stability can alternately be verified from the conductances of the SRTDs and the bias stabilizer. The conductances were calculated by taking the derivative of current with respect to voltage (figure 5.7). The conductance of the SRTDs is represented by $G_{rtd1} + G_{rtd2}$, while the conductance of the bias stabilizer is represented by G_{stab}. The total peak negative conductance of the two SRTDs is 15.2 mS. In order to ensure that the bias stabilizer provides DC stability over the entire NDR region, the conductance of the bias stabilizer should be $>$ 15.2 mS. This is indicated by the dotted line on the graph. If the conductance of the bias stabilizer lies above this dotted line in the NDR region, then conditions of DC stability will be satisfied over the entire NDR region. As can be seen from the figure 5.7, DC stability is satisfied for this design. Some margin is allowed for device parameter variations.

Layout of this bias stabilizer is shown in figure 5.8. The designed value of series resistance R_{stab} for the bias stabilizer (figure 5.8) is 25 Ω while the Schottky contact area is 9.0 μm^2. The series resistance will be realized in the buried N++ layer of the Schottky-diode. The N++ layer sheet resistance is 4.4 $\Omega/\Box$, while its Ohmic contact resistance is 6.0 $\Omega - \mu$m. From these, the Ohmic to Schottky

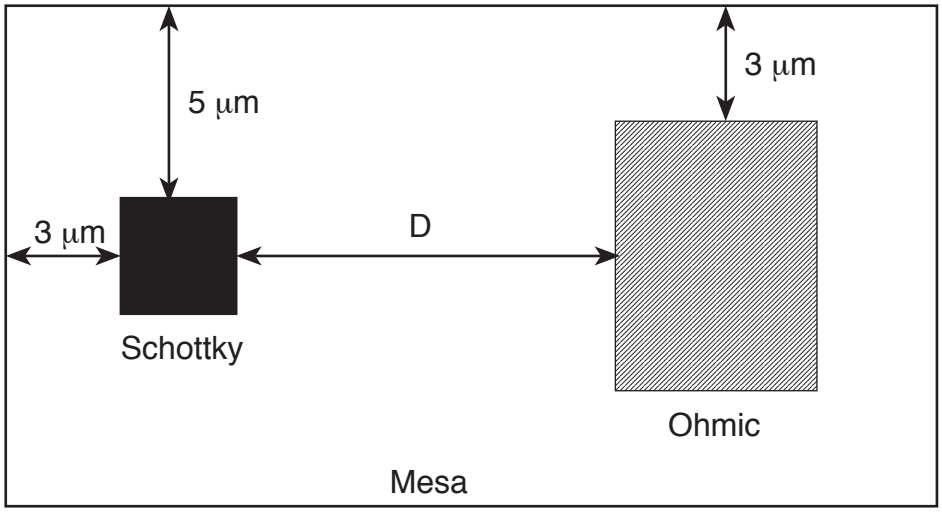

Figure 5.8: Layout of Schottky-diode bias stabilizer. The series resistance R_{stab}, of the bias stabilizer is realized in the buried N++ layer of the Schottky-diode by placing the Ohmic contact of the Schottky-diode at a distance D from the Schottky contact.

spacing D can be calculated. To account for the alignment tolerances during fabrication, the Ohmic pad is made larger than the Schottky pad by 2.0 μm on either side. The mesa edge is 3.0 μm from the Ohmic and Schottky pads to account for the excessive undercut of the mesa during the isolation wet etch and to accommodate alignment tolerances. Because of the larger mesa size and a larger Ohmic pad size, there will be current spreading in the mesa which will lower the overall value of the series resistance R_{stab}. From the sheet and the contact resistance values and assuming no current spreading, the required value of D is 16.0 μm. To account for the current spreading D is roughly increased by 1.5 squares to 20.5 μm. This should give a margin of $\pm$7.0 Ω on the required value of 25 Ω.

To ensure DC stability of SRTDs with larger areas than SR2 would require an appropriate scaling of the stabilizer resistance R_{stab}, and Schottky-diode junction area. If the dimension perpendicular to the current flow is scaled appropriately, then the series resistance R_{stab} will also scale accordingly. The various designs for the bias stabilizers for SRTDs with different area are shown in table 5.4.

These bias stabilizers were designed for SRTD effective areas varying from 0.4 μm^2 to 1.6 μm^2. In each case the bias stabilizer is shared between two neighboring SRTDs. For example, BS2 represents the DC bias stabilizer for two

Design	SRTD	Schottky-diode area (μm^2)	R_s (Ω)	D (μm)
BS2	SR2	9.0	25.0	20.5
BS3	SR3	13.5	16.7	20.5
BS4	SR4	18.0	12.5	20.5
BS6	SR6	27.0	8.33	20.5
BS8	SR8	36.0	6.25	20.5

Table 5.4: Bias stabilizer designs for various SRTDs in the device library. Each bias stabilizer provides DC stability for two SRTDs connected in parallel. The Schottky contact width for all the designs is 3.0 μm while the length changes according to the area of the Schottky-diode.

SR2 devices connected in parallel.

5.4 Oscillator Arrays

Single-element slot antenna coupled oscillators have been designed. For a given SRTD loading the center of the slot antenna, the required slot length, the DC bias stabilizer, and the capacitors C_{stab} have been determined for target oscillation frequencies ranging from 100 GHz to 1000 GHz. Since this was the first attempt at building submm-wave SRTD oscillators, the risk involved in building only large oscillator arrays was avoided. 2-element array oscillators consisting of 2 single-element slot antenna coupled SRTD oscillators and one DC bias stabilizer were therefore designed. All 37 designs from the table 5.2 were chosen for the 2-element array oscillators. Each of these 2-element array oscillators contains one corresponding bias stabilizer located between the two adjacent slot antennas. The nomenclature for the 2-element array designs is XXXGYU2×1 where XXX represents the target design frequency of oscillation, Y represents the SRTD stripe length and 2×1 represents the array size. For example, 100G2U2×1 indicates a 100 GHz 2-element array oscillator with a SRTD of stripe length 2.0 μm loading each of the slot antennas.

Array oscillators larger than 2 elements were also designed. These arrays would have larger output power levels due to the combining of the power outputs of the multiple oscillators. A systematic array oscillator design would require treatment of antenna-antenna coupling effects, and the loading effects of the

Design	Target f_{osc} (GHz)	SRTD	No of elements	X-sep (μm)	Y-sep (μm)
100G2U4×4	100	SR2	16	595	440
100G4U4×4	100	SR4	16	580	440
100G8U4×4	100	SR8	16	490	440
100G3U8×8	100	SR3	64	595	440
200G3U8×8	200	SR3	64	260	220
300G2U4×4	300	SR2	16	211	150
300G4U4×4	300	SR4	16	197	150
300G8U4×4	300	SR8	16	167	150
500G2U4×4	500	SR2	16	133	88
500G4U4×4	500	SR4	16	119	88
500G6U4×4	500	SR6	16	106	88
500G3U8×8	500	SR3	64	125	88
700G2U4×4	700	SR2	16	99	64
700G4U4×4	700	SR4	16	86	64
800G3U8×8	800	SR3	64	81	60
900G3U4×4	900	SR3	16	74	55
1000G2U4×4	1000	SR2	16	75	50
1000G2U8×8	1000	SR2	64	75	50

Table 5.5: Array designs with more than 2 elements at different target oscillation frequencies.

external resonant cavity. This was beyond the scope of this thesis. If these important effects are ignored, array development is simple. Given fabrication in an integrated circuit process, the additional effort required for building the larger arrays is only the additional mask layout effort required. Larger arrays consisting of either 16 elements or 64 elements were therefore designed in the 100 GHz-1000 GHz frequency range.

The single element oscillators designs were simply repeated in the X and Y dimensions on the plane of the wafer to obtain arrays. The spacing between the array elements is determined by the requirement of having only a single main lobe in the far-field radiation pattern of the array. This simply stipulates that the spacing between the adjacent elements is less than a wavelength in the substrate. The initial attempts at array oscillators are very simple first-order designs.

The minimum spacing between single elements in X-direction is fixed by the length of the slot antenna and the space required by the DC bias stabilizer. If the SRTD capacitance is negligible, giving the maximum possible slot length, the slot length is $(\lambda_0/2)((\epsilon_{r,sub}+1)/2)^{-1/2}$, where λ_0 is the free-space wavelength at f_{osc}. One-half the wavelength in the substrate is $(\lambda_0/2)(\epsilon_{r,sub})^{-1/2}$. Even without any capacitive detuning of the slot length, placing the antennas end to end ensures that the radiation pattern cannot show multiple diffraction lobes. In the Y-direction, the slot antennas are small, and the antennas can be very closely placed. The spacing in the Y direction was somewhat arbitrarily set (approximately) equal to the X-direction spacing.

It is clear from the above discussion that the array design is very crude. Yet, recalling the 2-parameter bracketing of the oscillator designs, there is a high confidence that some arrays will oscillate. The emphasis of this portion of the thesis was to demonstrate SRTD array oscillators to the highest possible frequencies. The various array designs are summarized in table 5.5. A very important design feature is that the entire array can be biased externally by two wires. The bias voltage across each SRTD is fixed by the voltage of the DC bias stabilizer. Individual bias leads for every array element are not required. The on-wafer bias stabilizer greatly simplifies array design and construction.

5.5 Mask Layout

The oscillator designs will be fabricated in a 8 mask layer process to be described in chapter 6. A sample mask layout of 2-element array oscillator is shown in figure 5.9. The slot length is arbitrarily defined as the distance between the

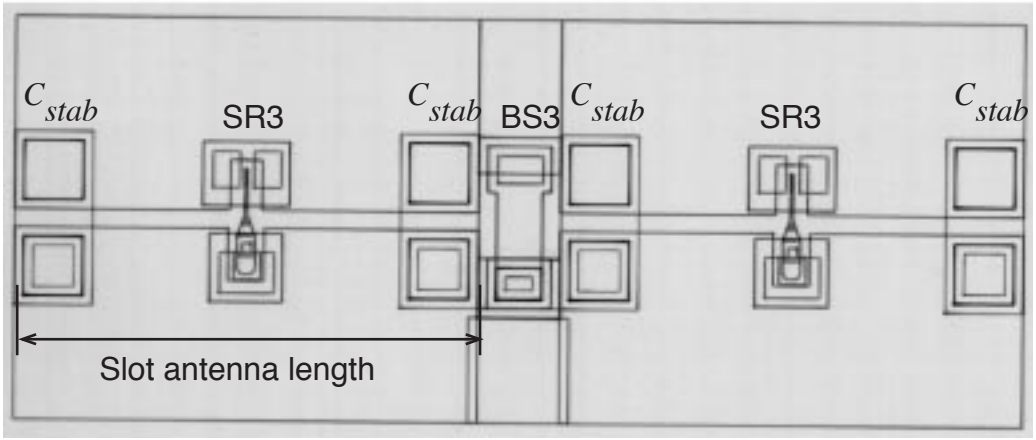

Figure 5.9: Sample mask layout of a 2-element slot antenna coupled array oscillator. The slot antennas are loaded by SRTDs (SR3) in the center. The ends of the slot antenna are shunted by MIM capacitors C_{stab}. DC stability is provided by the low impedance bias stabilizer (BS3) located between the 2 adjacent slot antennas.

outer edges of the capacitor. Since the capacitor dimensions are a significant fraction of the slot antenna dimensions, this may not be accurate. However, this definition of slot length is consistent in all the designs. The layouts for the larger arrays were obtained by repeating the single-element design layouts in the X and Y directions. A sample of mask layout for a 16 element array (4×4) is shown in figure 5.10.

DC biasing is provided through 100 μm×100 μm CPW pads of 150 μm pitch. Wiring between the CPW pads and the circuit is provided in the interconnect metal. Test structures for characterization of SRTDs, Schottky-diodes, N++ resistors, MIM capacitors, shunt combinations of SRTDs and the corresponding bias stabilizer designs were also laid out on the mask set. The test structures would help in verifying whether the process runs are successful in realizing the various elements of the circuit as designed. Since the most critical elements of these circuits are the submicron SRTDs, test structures were also provided to monitor the DC characteristics of these devices at the end of every mask step. The complete cell with all the designs and test structures had dimensions of 1.20 cm × 1.15 cm. On a 2-inch wafer this would give ≈ 9 cells, implying that a successful process run would give 9 circuits corresponding to each design. A different cell consisting of only the test structures was also created. This pattern would be used for characterizing the various process steps before embarking upon

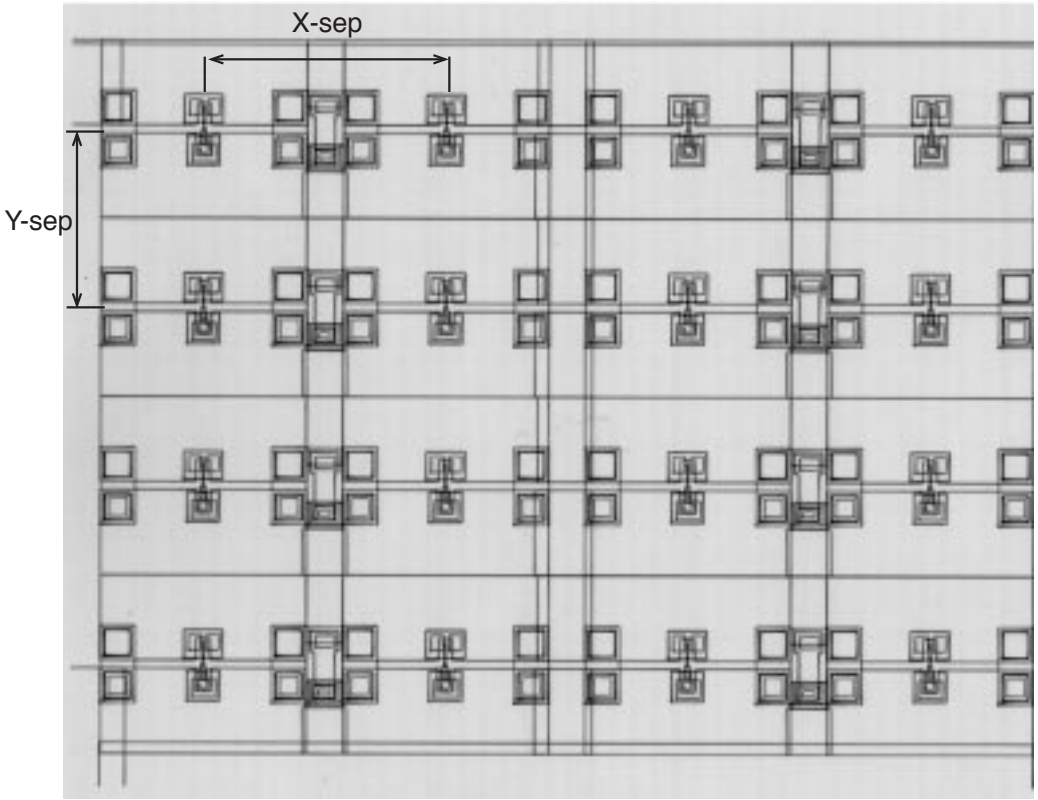

Figure 5.10: Sample mask layout of a 16-element array oscillator. The layout for array designs is obtained by simply repeating the single-element layout in the X and Y directions.

the circuit fabrication.

In this chapter, the circuit design approach for submm-wave slot antenna coupled oscillators was described. The values for various circuit elements were obtained for a simple one port negative resistance oscillator design incorporating on-wafer Schottky-diode bias stabilization. The bias stabilizer is designed such that it is shared by two neighboring SRTDs. A two-parameter bracketing of SRTD area and slot antenna length was also obtained for the single element oscillators. These single element array oscillators were then repeated as 2-element array designs. Some of the single-element oscillators were chosen for developing larger arrays. A mask layout incorporating all the designs was completed that would allow fabrication of the various array designs in a 8 mask layer process.

Chapter 6

Fabrication and Testing

In this chapter, fabrication and testing of the submm-wave SRTD oscillator arrays will be described. A 8 mask layer integrated circuit (IC) process was developed for monolithic integration of the various array elements. The IC fabrication was followed by extensive testing of the various designs to measure oscillation frequencies and output power levels. The lack of instrumentation at submm-wave frequencies makes testing of oscillator arrays difficult. A quasi-optical measurement system was set up for testing these oscillator arrays. Designs oscillating below 200 GHz were tested with a broad band bowtie-antenna-coupled Schottky-diode receiver operating as a harmonic mixer. Designs oscillating over 200 GHz were tested with a Fabry-Perot interferometer and a sensitive liquid Helium cooled Germanium (Ge) bolometer. Calibrated output power measurements with a thermo-acoustic power detector were obtained for a 300 GHz oscillator array. Calibrated power measurements of the higher-frequency oscillator array designs proved difficult as the output power levels were close to the threshold of the power detector.

6.1 Fabrication

Fabrication of submm-wave SRTD oscillator arrays incorporating on-wafer bias stabilization demands monolithic integration of 0.1 μm InGaAs SRTDs, graded bandgap AlInAs Schottky-diodes, slot antennas, N++ resistors and MIM capacitors. The MBE layer structure design for fabricating both SRTDs and Schottky-diodes on the same wafer was described in chapter 4. Monolithic integration of various array elements was achieved in a 8 mask layer process. The process was designed with the aim of minimizing the total number of mask layers to reduce

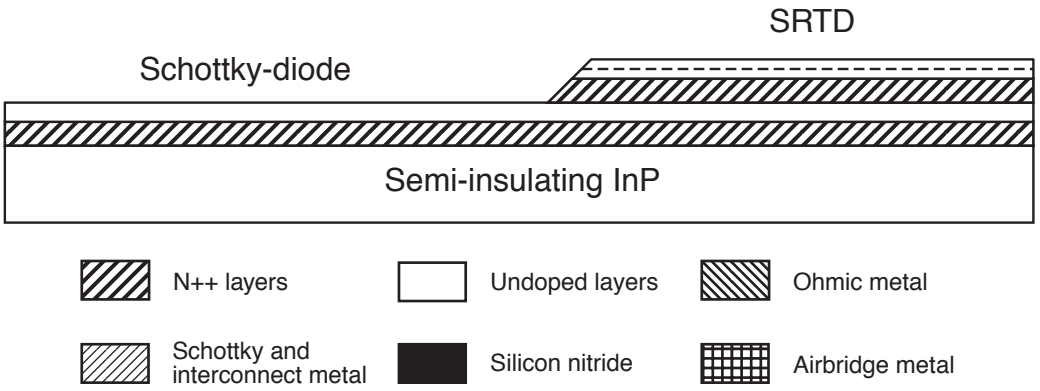

Figure 6.1: Cross-sectional view showing the etched regions of the Schottky-diode after the stabilizer etch.

processing risks. In this process, various features of the different array elements are simultaneously realized in each of the mask layers. Therefore, good process control to obtain accurate element values is constrained by conflicting processing requirements for the various array elements. In several mask steps, processing conditions for the primary requirement are chosen. Other array elements are designed around these process conditions. The complete process flow is provided in Appendix E. The main features of each process step will be described in the following subsections.

6.1.1 Stabilizer Etch

In the first mask step (figure 6.1), the SRTD layers lying above the Schottky-diode layers are removed by a wet etch in regions where the bias stabilizer is required. To obtain uniform characteristics of the Schottky-diode across the entire wafer, the wet etch must stop precisely on the Schottky-diode surface layers. A 1000 Å AlInAs separation layer was grown between the SRTD layers and the Schottky-diode layers for this purpose.

Initially, selective etchants ([39], [40]) that remove InGaAs layers and stop on the AlInAs separation layer were investigated. These etchants left black spots and rough surfaces in the etched regions. A phosphoric acid, non-selective etchant with a controlled and uniform etch rate was used instead to stop within the 1000 Å AlInAs separation layer. A selective etchant was then used to remove the remaining AlInAs layers and stop on the InGaAs cap layer of the Schottky-diode. Several problems were encountered with the non-uniformity of

the phosphoric acid wet etch during the initial fabrication attempts. This led to several process failures. After several experiments, processing conditions were obtained which achieved uniform etching across the 2-inch wafer.

The process begins with a standard photolithography step to protect the regions where the etching is not required. A non-selective etchant consisting of $H_3PO_4 : H_2O_2 : H_2O$ in a volumetric ratio of $3 : 1 : 50$ was used to etch the SRTD layers. This etch is stopped within the 1000 Å AlInAs separation layer. Suspending the wafer vertically in the etchant yielded non-uniform etching rates in small photoresist openings. To overcome this difficulty, the wafer was suspended horizontally in a large beaker of etchant consisting of $\approx$ 650 ml of etchant. A vigorous stirring of the etchant at $\approx$ 400 rpm improved the etch uniformity of this diffusion-limited etch. The sides of the Teflon basket holding the wafer were trimmed to ensure that the flow of the etchant was not blocked by the sides of the basket. With these conditions, a uniform etch rate was obtained in both small and large areas across the entire wafer. The etch was monitored through surface profiling of both small and large areas at regular intervals until the 1000 Å AlInAs layer is reached.

The non-selective etch is followed by a second wet etch which selectively removes the AlInAs layers and stops on the InGaAs layers. The etchant composition is derived from [41]. This etchant, commonly known as "A+B", consists of $HCl : H_2O : HBr : CH_3COOH$ in a volumetric ratio of $4 : 1 : 1 : 1$. Details of this etchant preparation are provided in Appendix E. The wafer is suspended horizontally in the A+B etchant. The etching process is accompanied by bubbling at the bottom of the wafer. This is a result of the substrate (InP) etching in HCl and the consequent release of highly toxic Phosphine gas. The A+B etchant removes the exposed AlInAs separation layer and stops on reaching the InGaAs cap layer of the Schottky-diode. The etch is monitored both by surface profiling and by visual examination under a microscope. The surface looks very rough during the etching process and becomes smooth upon reaching the InGaAs cap layer. Overetching is usually required to ensure that the etched surface regions become smooth across the entire wafer. The surface color of the etched regions is distinctly different from the unetched regions. A uniform surface color of all the etched regions across the wafer indicates that the etching has stopped on the InGaAs cap layer everywhere. Using the above conditions for the non-selective and selective etching, the stabilizer etch was successfully repeated in several process runs.

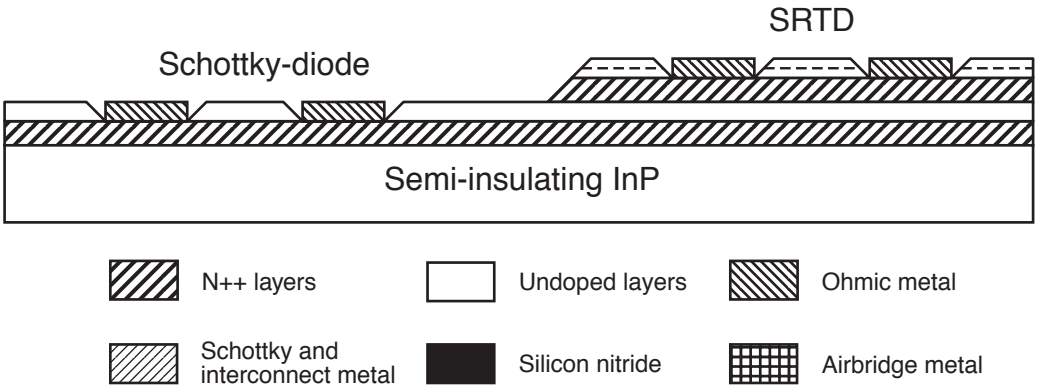

Figure 6.2: Cross-sectional view showing Ohmic contacts to the N++ layers of both the SRTD and the Schottky-diode.

6.1.2 Ohmic Contacts

In the second mask layer, Ohmic contacts to the N++ layers of both the SRTD and the Schottky-diode are achieved in a single step (figure 6.2). This process begins with a standard liftoff lithography step which creates openings in regions where the Ohmic contacts are required. This is followed by a recess etch to expose the N++ layers of both the SRTD and the Schottky-diode. A wet etch consisting of $H_3PO_4 : H_2O_2 : H_2O$ in a volumetric ratio of $3 : 1 : 50$ was used for the recess etch. The recess-etched layers of the Schottky-diode are ≈ 800 Å thicker than the recess etched layers of the SRTD. This implies that SRTD N++ layers are overetched by ≈ 800 Å. However, the etch rate is slightly faster in the graded bandgap AlInAs layers. Therefore, the N++ layers of both the SRTD and the Schottky-diode are reached in approximately the same etching time, thus avoiding an excess overetching of the SRTD Ohmic regions. Au/Ge/Ni metal is deposited in an e-beam evaporator immediately after the recess etch. After liftoff, the Ohmic metal is annealed in a rapid thermal annealer (RTA) at 360° C for 10 s. The Ohmic contacts are evaluated at this stage by measuring transmission line measurement (TLM) test structures. The surface morphology of the Ohmic contacts changes from smooth to rough after the thermal annealing. The alignment marks for e-beam lithography were also defined in this mask step. Occasionally, the rough edges of the Ohmic contact metal used for the alignment marks caused problems in e-beam alignment in the subsequent mask step. This could have been avoided by an additional mask layer to define the e-beam alignment marks separately, but at the cost of additional alignment

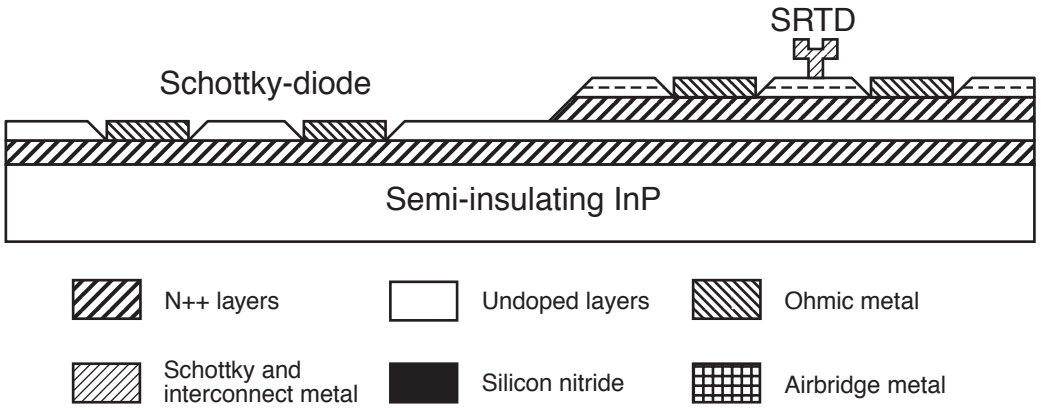

Figure 6.3: Cross-sectional view showing the 0.1 μm airbridge e-beam Schottky-collector of the SRTD after e-beam lithography.

tolerance.

6.1.3 Airbridge E-beam Lithography

In the third mask layer (figure 6.3), 0.1 μm Schottky-collectors for the SRTDs are defined using the airbridge e-beam lithography process. The details of this process were described earlier (chapter 3). The e-beam lithography process developed at JPL is the most critical process for the successful fabrication of submm-wave oscillator arrays. The throughput of the e-beam lithography step was not a problem despite the large number of e-beam fingers required for the fabrication of arrays. In order to facilitate easier alignment in the e-beam writer, the main cell on the mask layout was divided into 3 regions, each of which had separate e-beam alignment marks. The surface preparation just before deposition of Schottky-metal was found to be very critical for obtaining a good yield on the SRTDs. Details of the surface preparation are given in Appendix E.

6.1.4 Mesa Isolation

In this step, electrical isolation between devices is achieved by etching mesas (figure 6.4). The isolation between the active and passive mesas of the SRTD is also achieved in this step by overetching to remove the active semiconductor layers beneath the airbridge e-beam finger. Isolation between the active and the passive mesas for the SRTD requires the longest etching time and thus determines the overall etching time. The mesa height for the Schottky-diode is

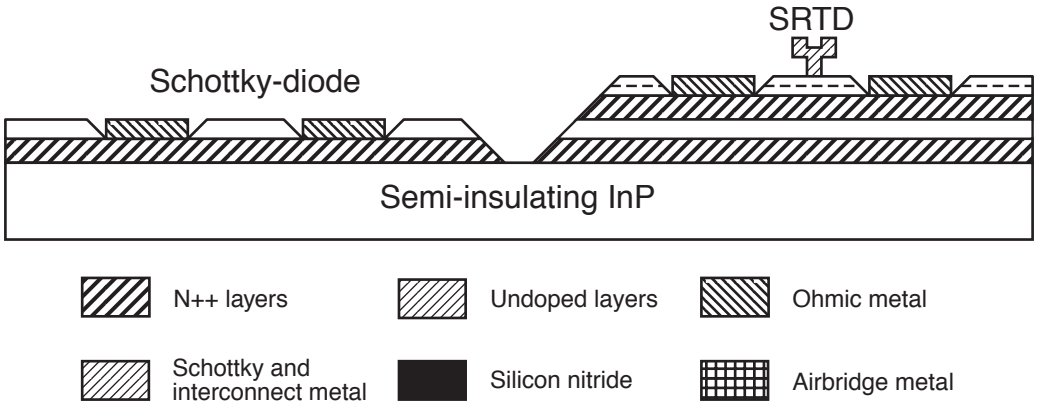

Figure 6.4: Cross-sectional view showing the devices after mesa isolation. The height of the mesa for the Schottky-diode is roughly one-half the height of the mesa for the SRTD.

approximately one-half the mesa height for the SRTD. This implies that the Schottky-diode mesa is undercut significantly during the long overetch. The mesa edges for the Schottky-diode define the value of the series resistance R_{stab} of the bias stabilizer. Therefore, it is important to monitor R_{stab} during the etch. Since the primary requirement during this mask step was the mesa isolation of various devices, the significant undercut of the Schottky-diode mesa was accommodated in the mask layout by increasing the size of the Schottky-diode mesa. Another important requirement of this process step is to obtain mesa edges that are gently sloping outward. This is required for step coverage of interconnect metal over the mesa edges in the subsequent process step. As can be seen from this discussion, several process requirements are imposed upon a single process step, which makes process control difficult. Good process control could have been achieved by additional mask layers.

During the process development for fabricating discrete SRTDs (chapter 3), a phosphoric acid etch was used successfully for mesa isolation. However, problems were encountered with the phosphoric acid etch during the mesa isolation step for array fabrication. The mesa edges of the SRTD and the Schottky-diode experience a significant undercut due to the overetch. During this overetch, the exposed AlInAs separation layer along the SRTD mesa edge undercuts more than the overlying InGaAs layers. This arises due to a slightly higher etch rate of AlInAs in the phosphoric acid etch. The SRTD mesa edges therefore do not slope gently outward and instead a mesa undercut profile with overhanging mesas is obtained. This creates a problem during step coverage of interconnect metal

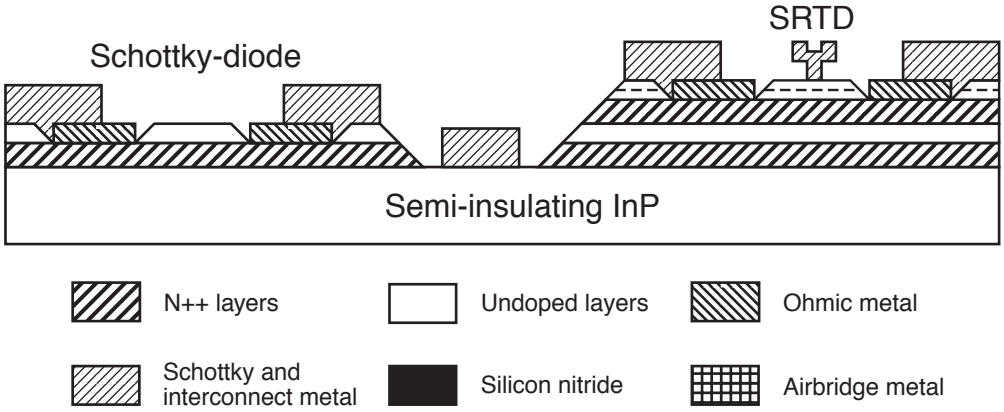

Figure 6.5: Cross- sectional view showing the devices after deposition of interconnect metal.

over the SRTD mesa. Breaks were observed in the interconnect metal running over the SRTD mesa. To overcome this problem, a citric acid etch that etches both InGaAs and AlInAs at roughly the same rate was instead used.

The process starts with standard AZ4210 lithography and a hard bake of the photoresist prior to the etching. The etchant, consisting of citric acid : H_2O : H_2O_2 : H_3PO_4 in a volumetric ratio of 11 : 44 : 1 : 0.2, etches both InGaAs and AlInAs at $\approx$ 450 Å/min. The total etching time to achieve electrical isolation of all circuit elements is $\approx$ 55 min. The etch is monitored by measuring the DC characteristics of the SRTD. The photoresist mask is removed after SEM inspection to ensure that all the SRTDs on the 2-inch wafer are isolated.

6.1.5 Interconnect Metal

Thick interconnect metal consisting of Ti/Pt/Au is deposited forming the slot antennas, the first level of interconnection between the Ohmic pads of the SRTD and the Schottky-diode, the Ohmic pad on the passive mesa of the SRTD and the bottom plate of the MIM capacitor (figure 6.5). The interconnect metal runs over the edges of the mesas to contact the Ohmic pads on top of the various mesas. Step coverage of metal over all the mesas is therefore important to ensure proper interconnections. To minimize the risk of metal breakage, the interconnect metal is made to cross over at least three edges of the mesa.

The process begins with a photolithography step that uses multi-layer resists. The bottom layers of the photoresist are OCG825 while the topmost layer is

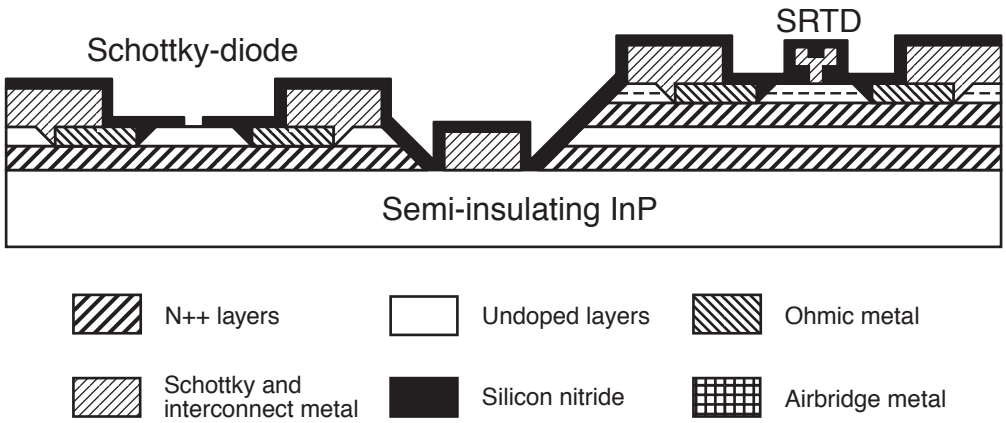

Figure 6.6: Cross- sectional view showing the devices after patterning the silicon nitride. The vias for Schottky-diode and to the bottom plate of the MIM capacitor are defined in this process step.

AZ4210. The significant undercut of the underlying OCG825 layers aid in liftoff of thick metal. A 1.5 μm thick interconnect metal is deposited. SEM inspection is required to ensure a good step coverage of interconnect metal over the mesas.

6.1.6 Silicon Nitride

A 1000 Å of silicon nitride (Si_3N_4) is deposited on wafer by PECVD in this process. The thin dielectric is necessary for the fabrication of MIM capacitors. The dielectric is then patterned by removing the Si_3N_4 in those regions where the vias are required (figure 6.6). Vias are required to access the bottom plate of the MIM capacitors and to expose the Schottky-diode surface layers, where the Schottky-contact of the Schottky-diode is desired. The dimensions of the Schottky-diode are defined by the size of the via. Initially, a wet etch in BHF was used to pattern the silicon nitride. This left a rough surface on the Schottky-diode regions. A Schottky-contact to this rough surface would yield irreproducible and poor Schottky-diode characteristics. A dry etch process consisting of $SF_6/Ar/O_2$ gases was used instead for etching the silicon nitride. The dry etch did not leave a rough surface on the Schottky-diode. The dry etch was monitored with a laser to stop the etching after all the exposed Si_3N_4 has been removed. Excessive overetching that could cause damage to the exposed Schottky-diode surface layers is thus avoided. The dry etch process also eliminates the undercut of the via making a more exact reproduction of the nominal

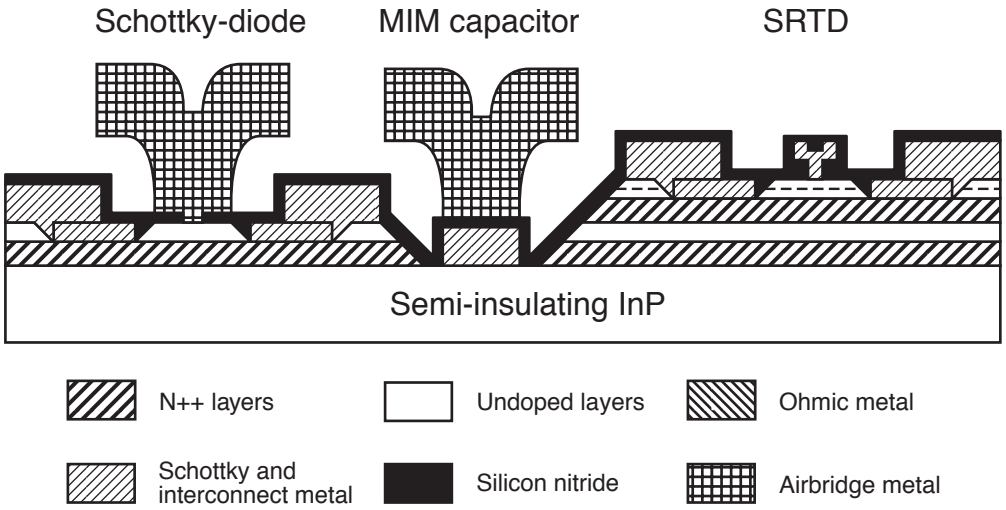

Figure 6.7: Cross- sectional view showing the devices after posts and airbridges. In these two last mask layers, the second level of interconnections, the top plate of the MIM capacitors and the Schottky-metal for the stabilizer are created.

dimensions onto the wafer. The photoresist mask is finally removed in acetone after ensuring that all the Si_3N_4 in the vias has been etched.

6.1.7 Posts and Airbridges

In the last two mask layers (figure 6.7), posts and airbridges are created which form the second layer of interconnection, the top plate of the MIM capacitor and the Schottky-contact for the Schottky-diode. The plated airbridge process uses sputtered Ti/Au for a flash layer. The quality of the sputtered metal for the Schottky-contact is questionable as the sputtering mechanism could damage the Schottky-diode surface. Further, the Schottky-metal deposition is normally done at very low pressures (7×10^{-7} Torr) to ensure clean Schottky metal-semiconductor interface. The desired low pressures cannot be achieved in the available sputtering system. Therefore, an airbridge process that uses evaporated metal was adapted for the array fabrication.

The first step in this process requires creating the posts for the airbridges. The wafer is coated with 2 layers of a deep UV sensitive resist (SF11) followed by a layer of AZ4210. The posts pattern is transferred from the mask to the deep UV sensitive resist (SF11) through a standard AZ4210 lithography step. After pattern transfer, the AZ4210 photoresist is removed in acetone. Acetone

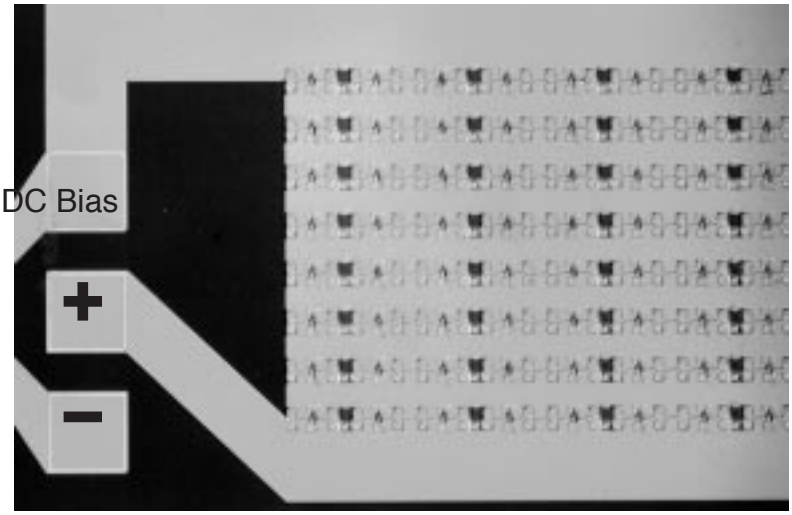

Figure 6.8: Photograph of a section of fabricated IC showing the complete circuit of a 64-element SRTD oscillator array. The on-wafer Schottky-diode bias stabilizer makes it feasible to bias the entire array with only two wires.

does not dissolve the bottom layers of SF11. The edges of the posts are then rounded by a reflow of SF11 at 200 °C for 10 min. This is necessary to ensure that airbridge metal flows smoothly over the post edges without breaking.

The wafer is then coated with multi-layer resists consisting of 3 layers of OCG825 and a top layer of AZ4210. A short flood expose and a toluene soak, after each coating of OCG825 prevents intermixing of the different layers of resist. The airbridge pattern is then transferred by exposure and development. The photoresist pattern is at least 7.0 μm thick in regions where both posts and airbridges are present and is at least 5.0 μm thick where only the airbridge is present. A thick metal (Ti/Pt/Au, $\approx$ 3.0 μm thick) is then deposited in the e-beam evaporator. Liftoff is achieved by soaking the wafer in acetone. Finally, the bottom layer of SF11 (post layer) is removed in hot 1165 photoresist remover at 100 °C. The yield of the evaporated airbridges was almost 100 %. This completes the fabrication of oscillator arrays.

6.2 Photographs

Photographs of the fabricated ICs at various magnifications showing the representative features of the oscillator arrays are shown in figures 6.8, 6.9, 6.10,

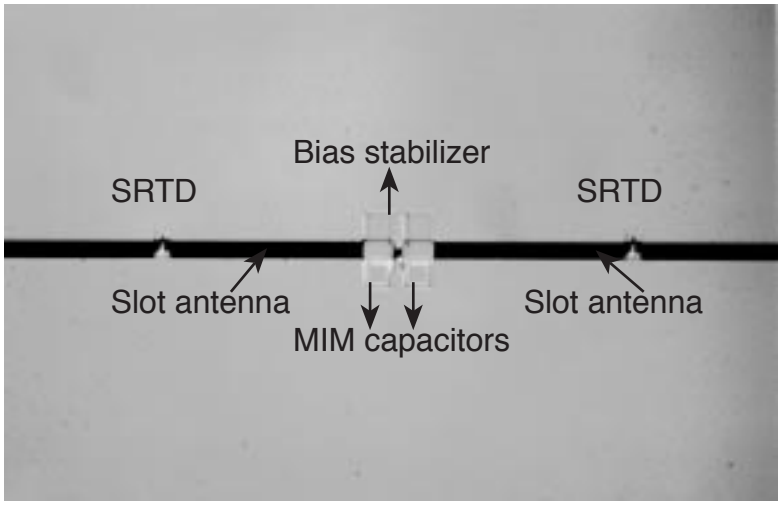

Figure 6.9: Photograph of a section of fabricated IC showing the features of a single element oscillator of the array. The 0.1 μm SRTD is located in the center of the slot antenna whose ends are shunted by MIM capacitors. The Schottky-diode bias stabilizer is shared by two neighboring SRTDs and is located between the two adjacent slot antennas.

6.11. The first photograph (figure 6.8) shows the complete circuit of a 64-element array. The array consists of periodic repetition of the single element oscillator in X and Y directions. This array consists of 64 slot antennas, 64 submicron SRTDs, 32 bias stabilizers and 128 Si_3N_4 MIM capacitors which emphasizes the monolithic integration capabilities of the IC process. Unlike earlier quasi-optical arrays [31], [45] which require bias connections to individual elements of the array, the DC biasing of the entire oscillator array here can be achieved through two wires in the interconnect metal. This simplified biasing is possible due to the on-wafer bias stabilizer which fixes the DC voltage across each SRTD.

A close up of the array is shown in figure 6.9, which shows the different elements of a single element oscillator in detail. The ends of the slot antenna are shunted by silicon nitride MIM capacitors. A 0.1 μm InGaAs SRTD is located in the center of each slot antenna. The bias stabilizer situated between the two adjacent slot antennas is shared by the two neighboring SRTDs. Figure 6.10 is a close up view of the 0.1 μm SRTD showing the active and the passive mesas and the airbridge submicron Schottky-collector spanning across from the passive mesa to the active mesa. The interconnect metal runs over three edges of the mesas to contact the Ohmic pads on top of the mesas. This provides the inter-

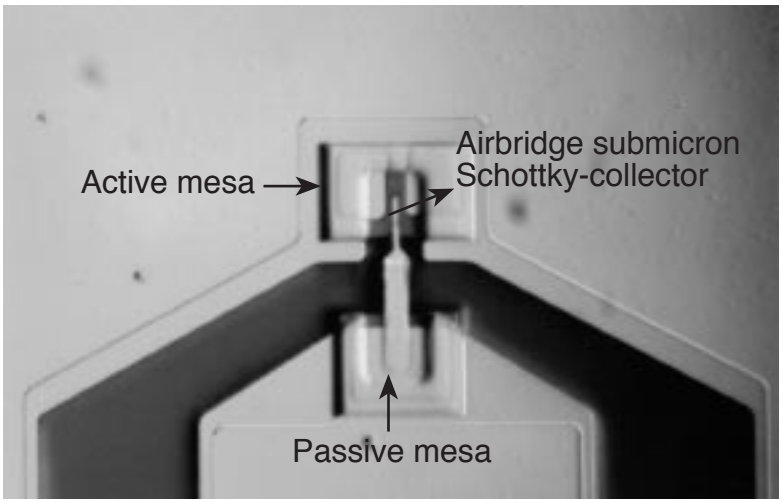

Figure 6.10: Photograph of a section of fabricated IC showing the SRTD. The 0.1 μm airbridge e-beam Schottky-collector spans from the active mesa to the passive mesa. The interconnect-metal runs over the edges of the mesas to contact the ohmic pads on top of the mesas.

connections between the two terminals of the SRTD and other circuit elements in the array. A SEM photograph (figure 6.11) of the 0.1 μm Schottky-collector is also included here. The SEM shows the airbridge submicron Schottky-collector where the SRTD junction area is defined accurately by the T-gate footprint. The various oscillator array designs differed in the number of array elements, SRTD stripe length, Schottky-diode area, size of the MIM capacitors, and slot antenna lengths. Therefore, the photographs shown here are representative of all the oscillator arrays on the wafer.

6.3 Preliminary Measurements

DC measurements of SRTDs, bias stabilizers and shunt combinations of SRTDs and their corresponding bias stabilizers were obtained initially. This is a quick and preliminary verification of the various device characteristics. DC measurements of SRTDs with varying stripe lengths are summarized in table 6.1. These are representative of the various SRTDs used in different circuits. The measured DC parameters are close to the design values. However, the yield of the SRTDs was nowhere near 100 % across the 2-inch wafer. The yield of the SRTDs was the limiting factor in the number of working circuits.

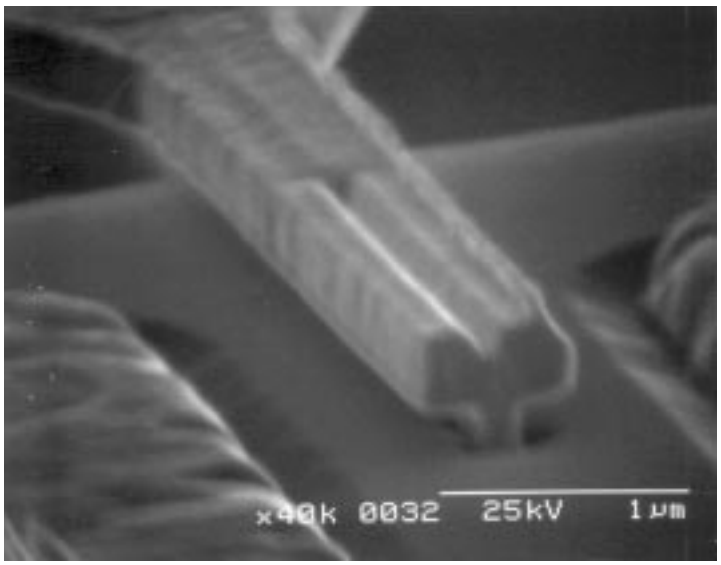

Figure 6.11: SEM photograph of the 0.1 μm SRTD showing the submicron Schottky-collector. The airbridge e-beam finger contacts the semiconductor only in the notch and is flying above the semiconductor elsewhere.

Design	Area (μm^2)	Length (μm)	V_p (V)	I_p (mA)	V_v (V)	I_v (mA)	G_n (mS)
SR2	0.4	2	1.02	2.02	1.32	1.15	5.8
SR3	0.6	3	1.03	2.63	1.31	1.64	9.4
SR4	0.8	4	0.98	3.67	1.29	2.25	9.2
SR6	1.2	6	1.01	5.32	1.32	3.19	13.7
SR8	1.6	8	0.98	5.88	1.31	3.58	13.9

Table 6.1: Measured DC parameters of 0.1μm SRTDs with different stripe lengths. Here, area represents the effective area of the SRTD assuming a 0.2 μm effective collector width.

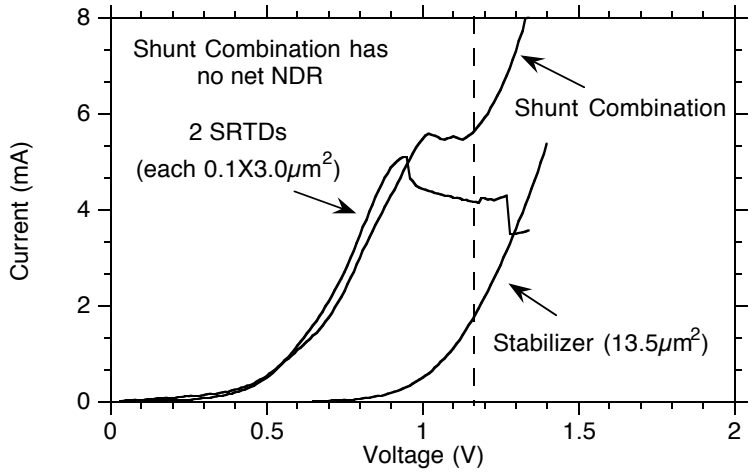

Figure 6.12: DC characteristics of individual SRTDs, individual Schottky-diode bias stabilizer and their shunt combination.

The DC characteristics of a test device consisting of a shunt combination of 2 SRTDs and a bias stabilizer were measured. This test device consists of a shunt combination of two SRTDs with 3.0 μm stripe length (2 SR3's in parallel) and the corresponding bias stabilizer BS3. As per the design, the DC characteristics of the shunt combination should have no net NDR region. The measured DC characteristics (figure 6.12) however show a small NDR region, indicating that the bias stabilizer is not stabilizing the SRTD over the entire NDR region. Shown on the same graph are the measured DC characteristics of the individual SRTDs and the bias stabilizer. The Schottky-diode turn-on voltage was slightly larger than the design value. This causes the slight NDR region in the DC characteristics of the shunt combination. Other bias stabilizer designs for SRTDs with longer stripe lengths, had very similar characteristics. The SRTD can be biased in its NDR region at voltages beyond the voltage corresponding to the dotted line. For such bias voltages, problems of DC bistability or parasitic bias circuit oscillations are eliminated for the shunt combination. At these bias voltages, the negative conductance of the SRTD is lower than its peak negative conductance and a consequent lowering of f_{max}. However, oscillations can be ensured if the magnitude of the SRTD negative conductance is greater than the slot antenna radiation conductance. The bracketing of SRTD area in the circuit

design provides sufficient margin to account for the lower negative conductance at these bias voltages. From the measured DC characteristics, it is clear that the oscillator arrays can be biased without the problems of DC bistability or parasitic bias circuit oscillations. This demonstrates the implementation of the on-wafer bias stabilization scheme. For every oscillator array, the voltage and current should scale appropriately with the number of array elements and the device areas.

The capacitance per unit area for the MIM capacitors was obtained from the capacitance measurements of a 100 μm$\times$100 μm capacitor. The measured value of 0.53 fF/μm^2 is very close to the designed value of 0.6 fF/μm^2. The capacitors used at the ends of the slot antenna are smaller in size than the 100 μm$\times$100 μm capacitor. The capacitance of the various C_{stab} designs were measured on a network analyzer to 40 GHz. The capacitance per unit area of these capacitors varied from 0.55 fF/μm^2 to 0.65 fF/μm^2, close to the design value. The yield of the MIM capacitors was 100%.

From these preliminary DC and microwave measurements, it was concluded that at least some of the oscillator circuits should function as designed. Therefore, entire attention was immediately diverted to the demonstration of the oscillator circuits, which requires measurement of oscillation frequencies and output power levels.

6.4 Quasi-Optical Oscillator

A quasi-optical oscillator was first constructed to efficiently radiate the oscillator array signals into free-space. Most of the power from the slot antenna coupled oscillator array is radiated from the antenna into the substrate. A significant portion of this incident power is reflected at the substrate-air interface due to total internal reflection as shown in figure 6.13 (a). Therefore, the slot antennas integrated on thick substrates suffer from power loss into the substrate modes [44]. The simplest solution (figure 6.13 (b)) to this problem is to mount the oscillator array on a silicon (Si) hemispherical or hyperhemispherical lens. Si has the roughly the same dielectric constant as the InP substrate. With the Si lens, the radiation from the oscillator array is incident upon the lens-air interface at angles close to normal. Total internal reflection is avoided, and the bulk of the power can escape. A Si hyper-hemispherical lens with a diameter of $\approx$ 2.3 cm was used for the construction of the quasi-optical oscillator.

Besides eliminating power loss into substrate modes, an additional feature is provided by the Si lens. Due to a mismatch of dielectric constants at the

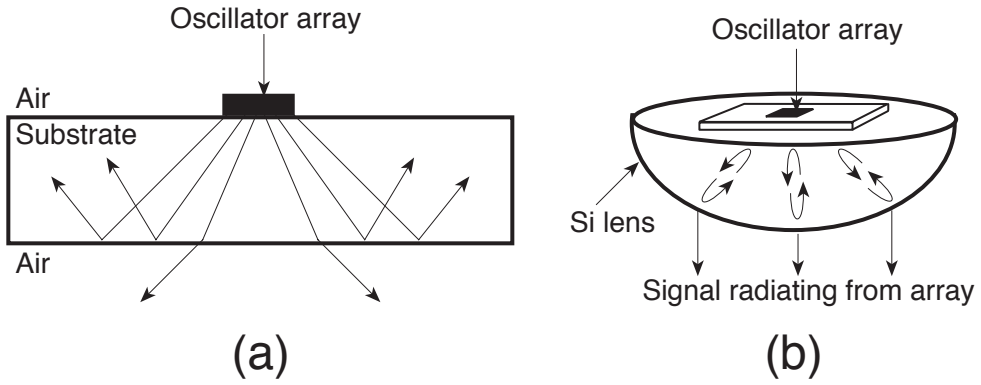

Figure 6.13: (a) Power from a slot antenna on a thick substrate is lost into substrate modes due to total internal reflection at the substrate-air interface. (b) To overcome this, a quasi-optical oscillator is formed by mounting the oscillator array on to a Si lens which also forms a resonant cavity of the oscillator.

lens-air interface, part of the incident signal power is transmitted through the lens into air, while the remaining is reflected back to the array. This gives rise to cavity modes within the lens. The resonant cavity is similar to that of a laser. The cavity mode spacing depends upon the cavity path length, in this case the lens diameter. The cavity mode spacing $\Delta f = v/2L$, where v is the velocity of propagation in the Si lens, and L is the length of the cavity. The cavity length is roughly 1.81 cm which gives a cavity mode spacing of 2.30 GHz.

Due to the poor Q of the on-wafer slot antenna at submm-wave frequencies, there is no guarantee that all the individual oscillators of an array are oscillating at the same frequency or in phase. Therefore, synchronization of array elements to the same frequency is required for quasi-optical power combining. Array synchronization is strongly influenced by the external cavity, and by near-field antenna-antenna coupling. These effects discussed in [42] are beyond the scope of this thesis. However, some rough observations can be made.

If many array modes are possible, mode competition (c.f. section 4.1) tends to force the array to oscillate at the mode having the highest cavity gain (the highest probability of oscillation). Unsynchronized or out-of-phase array elements correspond to partial excitation of higher order modes within the cavity. For a well-designed external cavity (e.g. in a laser) the higher-order cavity modes exhibit high diffraction losses. The resonant cavity formed by the Si lens thus favors the synchronization of array elements.

Ideally, the cavity should be designed such that only a single cavity mode

exists within the bandwidth of the on-wafer slot antenna. This would allow only one oscillation mode for the oscillator array. Clearly, the cavity employed in this thesis was chosen as a matter of convenience and not designed for good array synchronization. Despite this, the experimental data shows that strong synchronization was achieved.

6.5 Frequency Measurements

Due to the lack of instrumentation at the target design oscillation frequencies (100 GHz to 1000 GHz), measurement of oscillation frequencies and the output power levels proved difficult. A quasi-optical measurement system was assembled to measure the oscillation frequencies. The various parts of this set up were obtained from two previous research projects [46], [47]. Two approaches were used to test the various array designs on the wafer. For designs oscillating below 200 GHz, a broad band bowtie-antenna-coupled Schottky-diode operating as a harmonic mixer was used to detect the signals. Oscillators designed for frequencies beyond 200 GHz could not be tested with this set up due to the inability of the Schottky-diode harmonic mixer to detect the oscillator signals. This was attributed to the higher conversion losses associated with the higher harmonic mixing products. Therefore, a more sophisticated set up was required to test the higher frequency designs. Signals from designs oscillating above 300 GHz were detected with a sensitive liquid Helium cooled Germanium (Ge) bolometer. The frequency was determined by a scanning Fabry-Perot interferometer. With these two approaches, oscillation frequencies of various array designs were determined from 100 GHz to 650 GHz.

6.5.1 Schottky-Diode Harmonic Mixer

The Schottky-diode harmonic mixer set up consists of a mm-wave transmitter-receiver system as shown in figure 6.14. A photograph of the measurement set up is shown in figure 6.15. The RF signals from the quasi-optical oscillator array are focused onto a receiver IC mounted on a second Si lens through paraboloidal mirrors. The receiver IC consists of a broad band bowtie-antenna-coupled Schottky-diode placed on the receiver lens. The RF signal is coupled to the Schottky-diode through the bowtie-antenna. The bowtie-antenna coupled Schottky-diode (figure 6.16) was designed and fabricated by Dr. Uddalak Bhattacharya of UCSB. The GaAs Schottky-diode has a 0.1 μm$\times$1.0 μm Schottky-contact area while the depletion layer thickness in the semiconductor is $\approx$ 150 Å. The submicron

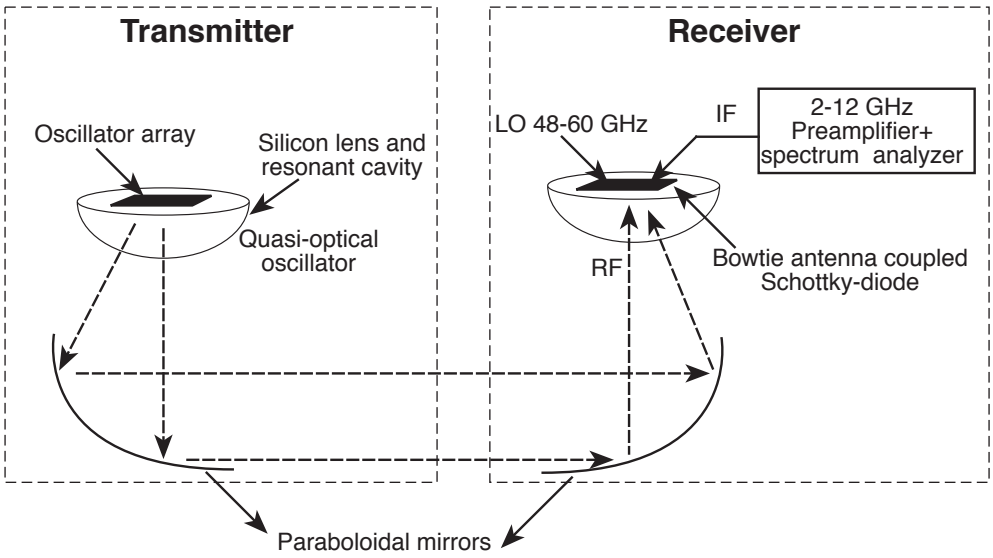

Figure 6.14: MM-wave transmitter-receiver system for testing oscillator arrays to 200 GHz. The receiver consists of a broad band bowtie-antenna-coupled Schottky-diode operating as a harmonic mixer.

Schottky-contact for the Schottky-diode was fabricated using the same airbridge e-beam lithography process developed at JPL for the SRTD project. Due to its extremely small dimensions and deep submicron scaling, the Schottky-diode has a $(2\pi R_s C)^{-1/2}$ cut off frequency of $\approx$ 20 THz. A bowtie-antenna is integrated with the Schottky-diode which has a lower cut off frequency of $\approx$ 100 GHz and an upper cut off frequency of $\approx$ 5.0 THz. The cutoff frequency as determined by Schottky-diode capacitance and the antenna radiation impedance is $\approx$ 4 THz. The broad band bowtie-antenna thus enables coupling of the RF signals from the quasi-optical oscillator to the Schottky-diode. A quasi-optical set up and a free electron laser pulse were utilized in an attempt to establish the frequency response of the bowtie-antenna coupled Schottky-diode. However, due to the difficulties in calibrating the frequency response of different parts of the quasi-optical set up, the exact frequency response of the bowtie-antenna-coupled Schottky-diode was never conclusively established. However, even weak coupling of the RF signals to the Schottky-diode is sufficient to operate the harmonic mixer for determining the oscillation frequencies. Since the bowtie-antenna-coupled Schottky-diode was readily available, the harmonic mixer approach was preferred in the first attempt to determine the oscillation frequency.

The Schottky-diode is operated as a harmonic mixer. The Schottky-diode

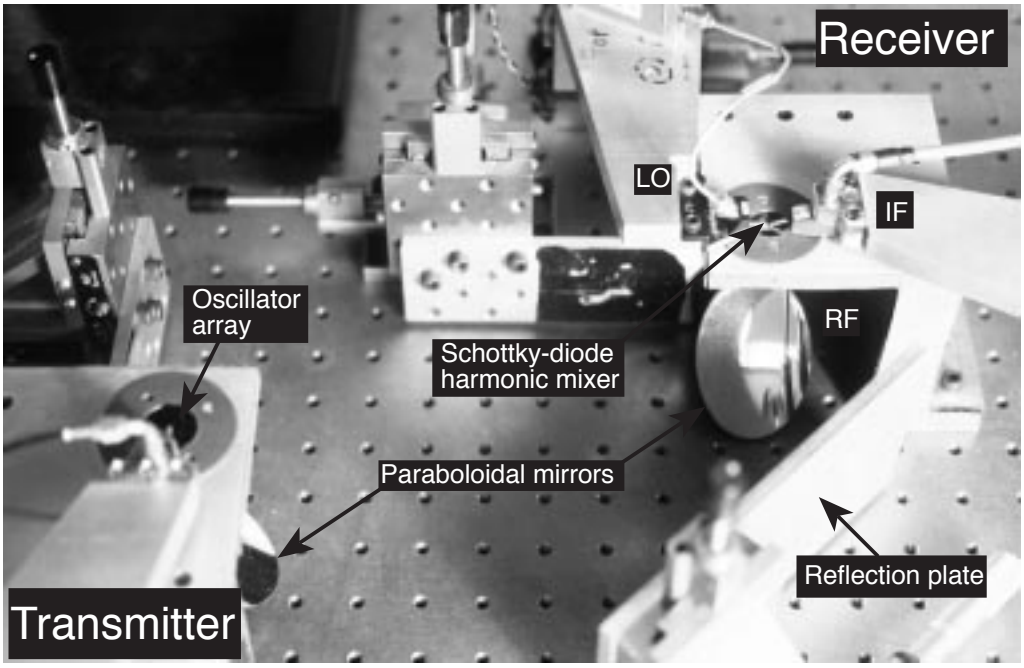

Figure 6.15: Photograph showing various parts of the mm-wave transmitter-receiver system for testing oscillators to 200 GHz.

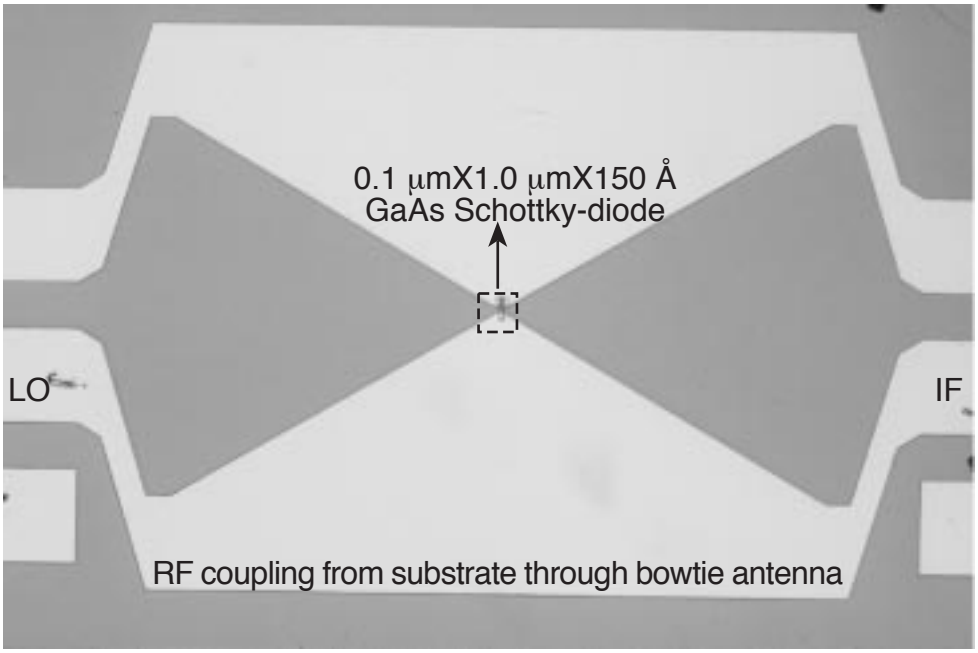

Figure 6.16: Bowtie-antenna-coupled Schottky- diode operated as a harmonic mixer. The LO signal (48-60 GHz) is fed to the Schottky-diode through CPW pads on the left, while the RF signal (> 100 GHz) is coupled to the Schottky-diode from the substrate through the bowtie-antenna. The downconverted IF signals (2-12 GHz) are detected by a preamplifier and a spectrum analyzer.

is switched on and off by a LO signal in the frequency range 48-60 GHz. The switching process generates harmonics of the LO signal which mix with the RF signals from the oscillator array. The harmonic mixing downconverts the RF signal to an IF frequency which lies within the bandwidth of the spectrum analyzer. To improve the detectability of weak signals, a preamplifier is provided in the IF signal path before the spectrum analyzer. IF signals can be detected if they lie within the 2-12 GHz bandwidth of the preamplifier and the spectrum analyzer. The IF frequency is related to the LO signal through equation 6.1, where n represents the corresponding harmonic of the LO signal that downconverts the RF signal to a 2-12 GHz frequency span.

$$f_{IF} =\mid nf_{LO} \pm f_{RF} \mid \tag{6.1}$$

The testing procedure begins with DC biasing of the Schottky-diode through a bias tee. The LO signal to the Schottky-diode is generated by a frequency quadrupler driven by a 12-15 GHz input signal. The LO signal thus has a frequency sweep between $48-60$ GHz. The output of the quadrupler also contains a weak signal at the input frequency (12-15 GHz). This signal is amplified by the preamplifier stage which has a bandwidth of 2-20 GHz. This causes an overloading of the spectrum analyzer due to a LO to IF feed through. To prevent overloading of the spectrum analyzer, a low pass filter at the preamplifier input limits the IF bandwidth to 12 GHz. The LO power is now slowly increased to a point where the Schottky-diode is driven strongly, conducting only for a small fraction of the cycle. This switching process generates several harmonics of the LO signal which have decreasing power with increasing harmonic number.

Any RF signal from the oscillator array can couple to the Schottky-diode through the broad band bowtie-antenna. This RF signal will mix with the various harmonics of the LO signal to generate signals at beat frequencies $nf_{LO} \pm f_{RF}$. The mixing process however, is associated with a conversion loss. The conversion loss increases with the decreasing power level at the corresponding harmonic. Due to lower power levels at higher harmonics, the conversion loss is higher for higher harmonic mixing products. The signals can be detected, if the IF signal level is greater than the noise floor of the spectrum analyzer.

Even without any RF signal present, signals were observed on the spectrum analyzer. These signals are at frequencies corresponding to $f_{LO}/12$ and $f_{LO}/6$. These correspond to the subharmonics of quadrupler input signal which are generated in the frequency synthesizer. These signals are amplified by the preamplifier stage. These signals however, are not very strong as to cause an overloading of the spectrum analyzer, but they should not be confused to be the

downconverted RF signals.

The DC voltage to the oscillator array is now increased such that the SRTDs are biased in the NDR region. If the array is oscillating, the RF signals will be radiated, incident on the receiver bowtie-antenna. Appearance of any new signals on the spectrum analyzer correspond to the downconverted RF signals. This is verified by placing an absorber between the two paraboloidal mirrors which results in the disappearance of these signals in the IF spectrum. The LO frequency is changed manually in the absence of any downconverted RF signals to find a LO frequency that would downconvert the RF signals to within the IF bandwidth. After signal detection, the paraboloidal mirrors are adjusted to increase the detected signal power level. The adjustment of mirrors is achieved through micropositioners which help in increasing the coupling of the RF signal to the bowtie-antenna. The frequency of the IF and LO signals are noted. The LO signal frequency is then perturbed by Δf_{LO}. The new LO and IF frequencies are also noted. From the magnitude and direction of the frequency shift in the IF signal, the RF frequency can be easily determined. The detected IF signal power on the spectrum analyzer is inclusive of the coupling losses in the quasi-optical system, conversion loss of the harmonic mixing process and the gain in the preamplifier stage. Therefore, estimation of the RF signal power requires a careful system calibration to obtain these various losses and gains in the system. This is difficult at mm-wave frequencies and therefore only rough estimates of the RF signal power can be obtained from these measurements.

6.5.2 Oscillations to 200 GHz

With the harmonic mixer set up, arrays oscillating at 100 GHz and 200 GHz were tested successfully. Higher frequency designs did not show any IF signals on the spectrum analyzer. This was attributed to the high conversion losses at the 6^{th} or higher harmonics of the LO. The results obtained with the 100 and 200 GHz designs will be discussed here.

A 100G8U2×1 oscillator array oscillated at $\approx$ 100 GHz. This 2-element array consists of a SRTDs with 8.0 μm stripe length loading each of the slot antennas. The DC bias conditions were 1.0 V and 20 mA. The DC bias remained at this value during the entire testing procedure which lasted several hours. This was possible due to the on-wafer bias stabilizer which stabilizes the SRTD to the external biasing circuit. DC bistability and parasitic bias circuit oscillations that usually tend to shift the biasing into the positive differential resistance region of the SRTD are thus avoided. The RF signals were observed with a LO

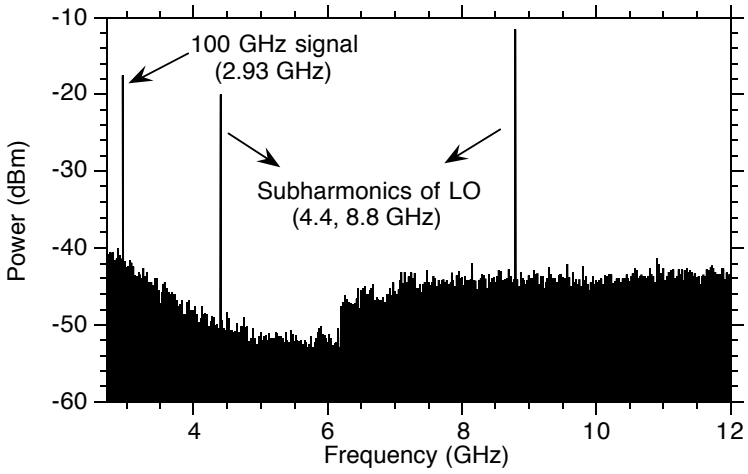

Figure 6.17: Full span of the IF spectrum of the 2-element array at 100 GHz. The subharmonics of the quadrupler input are observed at 4.4 GHz and 8.8 GHz.

signal frequency in the vicinity of 52 GHz. The full span of the IF spectrum for this measurement is shown in figure 6.17. The resolution bandwidth (RBW) and the video bandwidth (VBW) of the spectrum analyzer were both set to 300 KHz. The LO frequency was 52.8 GHz. The IF frequency shift was opposite to the LO frequency shift and the magnitude of the shift was twice the LO frequency shift. From this, it was concluded that the second harmonic of the LO signal was downconverting the RF signal to the IF bandwidth. The RF signal frequency was thus determined to be 109 GHz. The subharmonics of the quadrupler input (13.2 GHz) at frequencies 4.4 GHz and 8.8 GHz were also present in this spectrum. Spectral output with a reduced span (50 MHz) about the signal corresponding to the 109 GHz oscillations is shown in figure 6.18. The LO frequency of this measurement was 52.4 GHz. This signal also corresponds to the same RF frequency (109 GHz). The spectral output power is -36 dBm.

A 100G2U4×4 array design was then tested. This 16-element array consists of SRTDs with stripe length of 2.0 μm loading each of the slot antennas. The array was biased at 4.6 V and 10 mA. The LO frequency was 52.04 GHz. The full span of the IF spectrum is shown in figure 6.19. There were 3 IF signals that correspond to the array oscillations. These are at IF frequencies 3.40, 5.28 and 9.62 GHz. By changing the LO frequency, these were found to correspond to RF

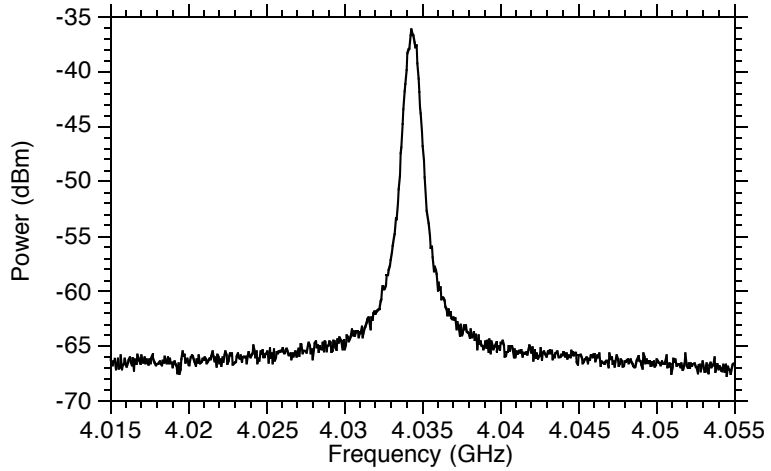

Figure 6.18: IF spectrum with a 50 MHz span about the 100 GHz downconverted RF signal. The RBW is 300 KHz, while the VBW is 300 KHz.

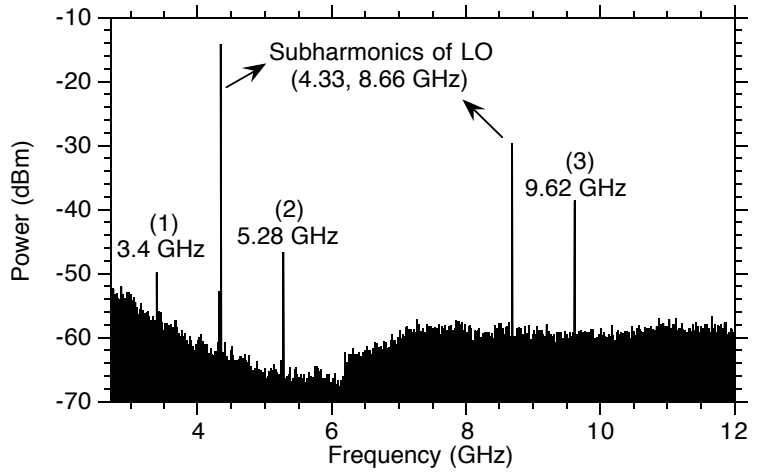

Figure 6.19: Full span of the IF spectrum of the 16-element array at 100 GHz showing 3 signals corresponding to 100 GHz RF oscillations. More than 90 % of the power is however concentrated in signal corresponding to 3.

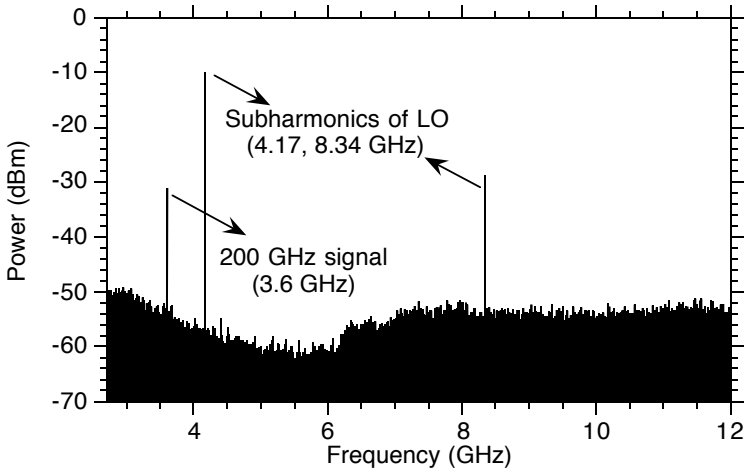

Figure 6.20: Full span of the IF spectrum of the 2-element array at 200 GHz. The subharmonics of the quadrupler input are present at 4.17 and 8.34 GHz

oscillations at 107.48, 98.8 and 94.46 GHz respectively. The IF signal powers at these frequencies were in the ratio of $2 : 12.5 : 200$ indicating that $\approx 90\%$ of the output power is in the dominant mode. An important observation is that the 3 modes are separated in frequency by exact multiples of 2.17 GHz, which seems to indicate strong resonances in the quasi-optical system at frequencies separated by 2.17 GHz. The observed RF frequencies separation is approximately equal to the 2.3 GHz estimated cavity mode spacing of the Si lens. In order to suppress the other two modes which have lesser power, a new cavity could be designed that has a mode separation >12 GHz.

A 200G8U2×1 oscillator array was also tested. This 2-element array designed for 200 GHz oscillations consists of SRTDs with stripe length of 8.0 μm loading each of the slot antennas. The array was biased at 1.1 V and 23.3 mA. The LO signal frequency was 50.0 GHz. The full span of the IF spectrum is shown in figure 6.20. The signal corresponding to the RF oscillations is downconverted to a frequency of 3.6 GHz. The RF frequency was determined by changing the LO frequency and measuring the magnitude and direction of shift of the down-converted IF frequency. The RF oscillations correspond to oscillation frequency of 196.4 GHz. The span of the spectrum analyzer was then reduced to 40 MHz about 3.6 GHz to obtain a zoomed view of the signal spectrum. This is shown

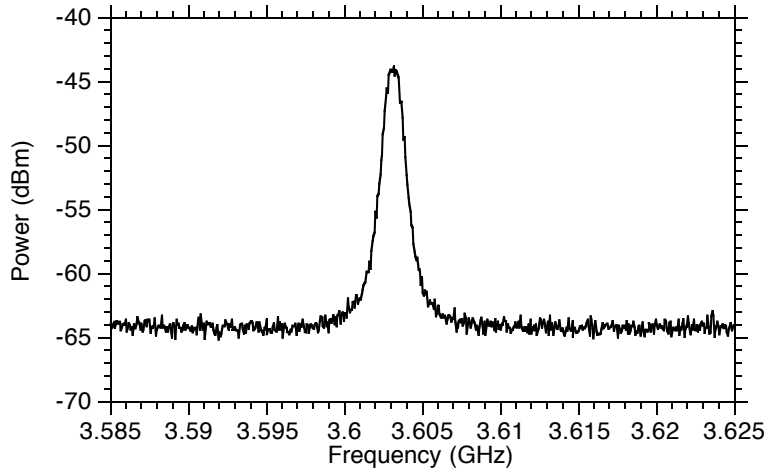

Figure 6.21: IF spectrum of the 2-element array at 200 GHz with a 40 MHz span. The RBW is 300 KHz, while the VBW is 300 KHz.

in figure 6.21. The output power of the downconverted RF signal is -43 dBm.

A 64-element array designed for oscillations at 200 GHz had a poor yield of SRTDs and therefore could not be tested. Designs at 300 GHz and higher did not show any signals in the IF spectrum for any LO frequency in the 48-60 GHz sweep. This was attributed to the high conversion loss associated with the 6^{th} or higher harmonics of the LO which can downconvert RF signals beyond 300 GHz to the IF bandwidth. Therefore, the measurement system could not be used to test higher frequency designs. A more sensitive detector is necessary to test the higher frequency designs.

6.5.3 Fabry-Perot and Bolometer

A schematic of the measurement set up for testing designs with oscillation frequencies $>$ 200 GHz is shown in figure 6.22. A photograph is shown in figure 6.23. The RF signals from the quasi-optical oscillator are focused onto a sensitive liquid Helium cooled Germanium (Ge) bolometer. A mechanical chopper at 150 Hz and a lockin amplifier are required for measuring the bolometer output signal. The bolometer also detects background radiation and therefore, a 0.5 mm thick fluorogold filter was placed in front of the bolometer to cutoff radiation

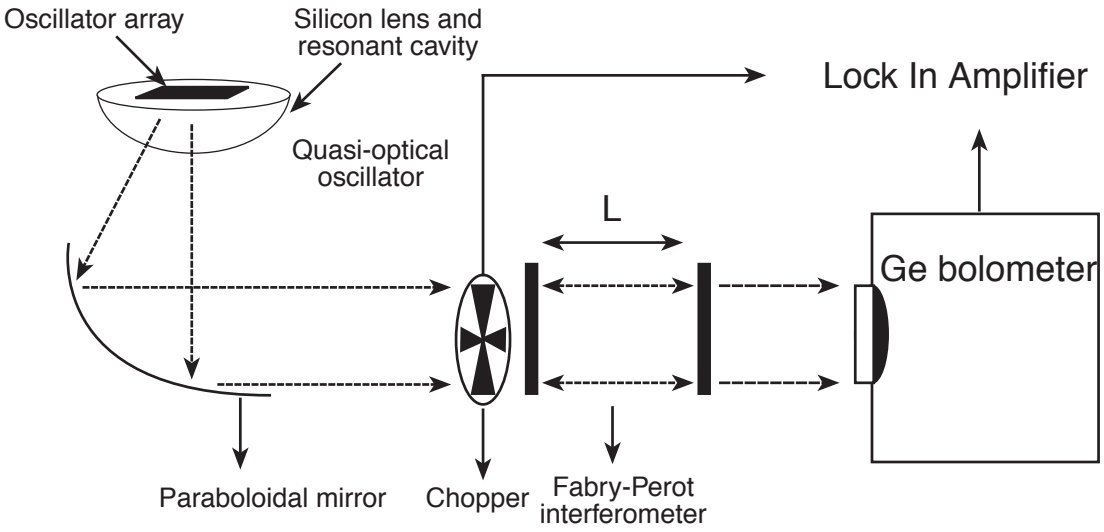

Figure 6.22: Fabry-Perot and Ge bolometer set up for detecting signals beyond 300 GHz.

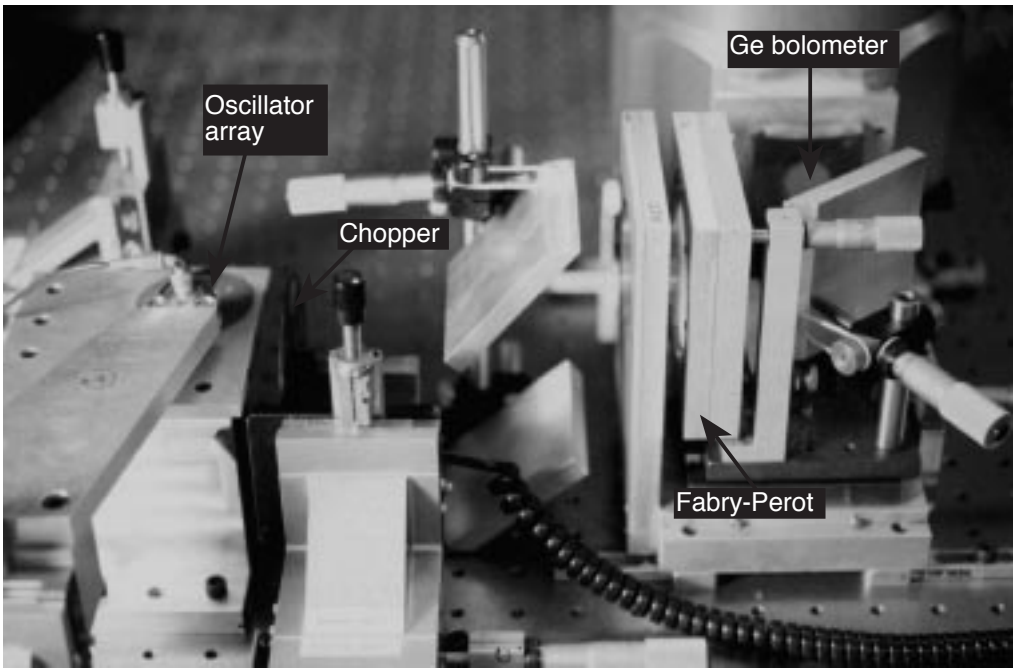

Figure 6.23: Photograph showing the various parts of the Fabry-Perot and Ge bolometer set up for detecting signals beyond 300 GHz.

with frequencies roughly > 700 GHz. With this set up, the bolometer can detect signals in the $300-700$ GHz frequency range. The Fabry-Perot placed in the beam path forms an external cavity that has peaks in transmission coefficient when the separation between its mirrors is a multiple of half a free-space wavelength. By varying the separation between the mirrors, peaks are observed in the bolometer output signal. The distance between two such consecutive peaks corresponds to half a free-space wavelength of the detected signal. Thus, the separation between the peaks allows determination of the free-space wavelength and hence the frequency of the oscillations.

The testing procedure begins with DC biasing of the oscillator array. The liquid Helium cooled Ge bolometer is set up as required. Initially, the Fabry-Perot mirrors are removed from the beam path to obtain a strong signal on the bolometer output. The Fabry-Perot cuts off a significant amount of the signal power even at its peak transmission. Alignment of system is then adjusted to obtain the strongest signal at the bolometer output. The Fabry-Perot mirrors are then placed in the beam path, the separation between the mirrors is changed manually by a micrometer, and the corresponding bolometer output is noted. Scanning the Fabry-Perot mirrors over roughly 2 free-space wavelengths gives at least 3 peaks in the bolometer output signal. The frequency of the oscillations is thus determined.

6.5.4 Oscillations to 650 GHz

With the bolometer and Fabry-Perot set up, oscillator arrays were tested from 300 GHz to 650 GHz. First, a 300G8U2×1 design was tested. This 2-element array, designed for 300 GHz oscillation, consists of SRTDs with 8.0 μm stripe length loading each of the slot antennas. The array was biased at 1.1 V and 25.0 mA. The bolometer output as a function of the separation between the mirrors is shown in figure 6.24. The separation between peaks in the transmitted signal is 0.49 mm which corresponds to a 310 GHz oscillation.

Next, a 300G4U4×4 array oscillator was tested. This 16-element array, also designed for 300 GHz oscillation, consists of SRTDs with 4.0 μm stripe length loading each of the slot antennas. The array was biased at 4.4 V and 17.9 mA. The peaks in the transmitted signal were separated by 0.525 mm, which corresponds to 290 GHz oscillations. Another 16-element array (300G8U4×4), designed for 300 GHz oscillation had SRTDs of 8.0 μm stripe length loading each of the slot antennas. This array was biased at 4.25 V and 38.6 mA. This array showed oscillations at 300 GHz with a peak separation of 0.5 mm in the

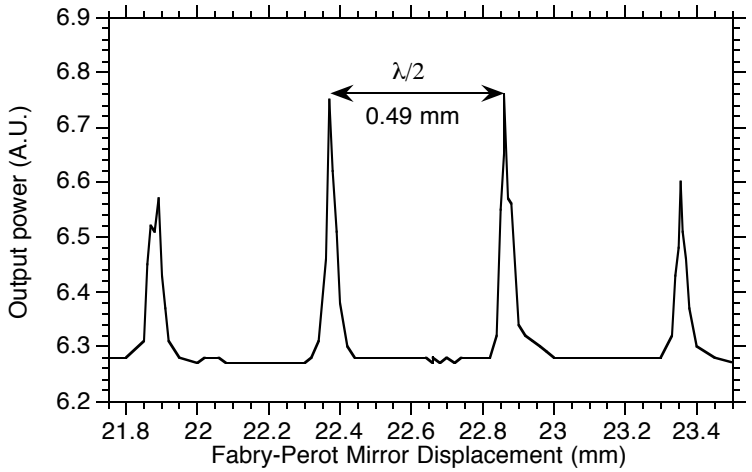

Figure 6.24: Bolometer output as a function of Fabry-Perot mirror displacement for the 2-element array at 300 GHz. The separation between the peaks is 0.49 mm which corresponds to 310 GHz oscillations.

bolometer output signal.

2-element arrays designed for oscillation frequencies above 300 GHz also showed signals on the bolometer output without the Fabry-Perot mirrors in the beam path. However, the signal levels dropped to the bolometer's threshold level with the introduction of the Fabry-Perot mirrors in the beam path. Therefore, oscillation frequencies of these 2-element arrays could not be determined conclusively. However, arrays with 16 or 64 elements at these design frequencies had larger signal levels and these were tested to determine oscillation frequencies beyond 300 GHz.

A 500G4U4×4 array design was tested. This 16-element array, designed for 500 GHz oscillation, consists of SRTDs with 4.0 μm stripe length loading each of the slot antennas. The array was biased at 4.3 V and 22.6 mA. Separation between the peaks in transmitted signal was measured as 0.32 mm, which corresponds to 470 GHz oscillation. Next, a 700G4U4×4 array design was tested. This 16-element array, designed for 700 GHz oscillation, consists of SRTDs with stripe length of 4.0 μm loading each of the slot antennas. The array was biased at 4.25 V and 19.6 mA. Peaks in transmitted signal were separated by 0.27 mm which corresponds to an oscillation frequency of 560 GHz.

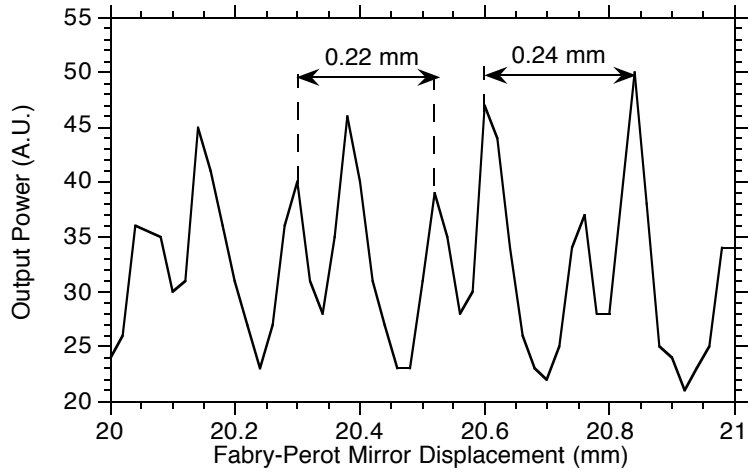

Figure 6.25: Bolometer output as a function of Fabry-Perot mirror displacement for the 64-element array at 800 GHz. Multiple peaks are observed in the bolometer output which corresponds to multimode oscillations.

Finally, a 800G3U8×8 array design was tested. This 64-element array, designed for 800 GHz oscillation, consists of SRTDs of 3.0 μm stripe length loading each of the slot antennas. The array was biased at 8.5 V and 33.4 mA. There were a multiple peaks in the transmitted signal (figure 6.25). These signals roughly corresponded to 650 GHz oscillations. The multiple peaks were attributed to the various array elements oscillating at adjacent cavity mode frequencies. This was also observed distinctly in the harmonic mixer set up when the 16-element 100 GHz oscillator array was tested. The signals show oscillations near 650 GHz, but in order to obtain a convincing measurement of oscillation frequency, the resonant cavity in the system (Si lens) was redesigned with the hope of locking these signals to a single frequency.

An $\approx$ 800 μm air gap was created between the Si lens and the oscillator array, thereby creating an additional cavity in the system. The Si lens and the air gap now form a hybrid cavity (figure 6.26 (b)). The hybrid cavity modes occur only when the cavity modes of the air gap and the Si lens cavity are matched, leading to a suppression of several cavity modes of the Si lens. This is explained qualitatively with simple transmission line models of the two cavities (figure 6.26). For normally incident plane waves, each dielectric in the cavity can

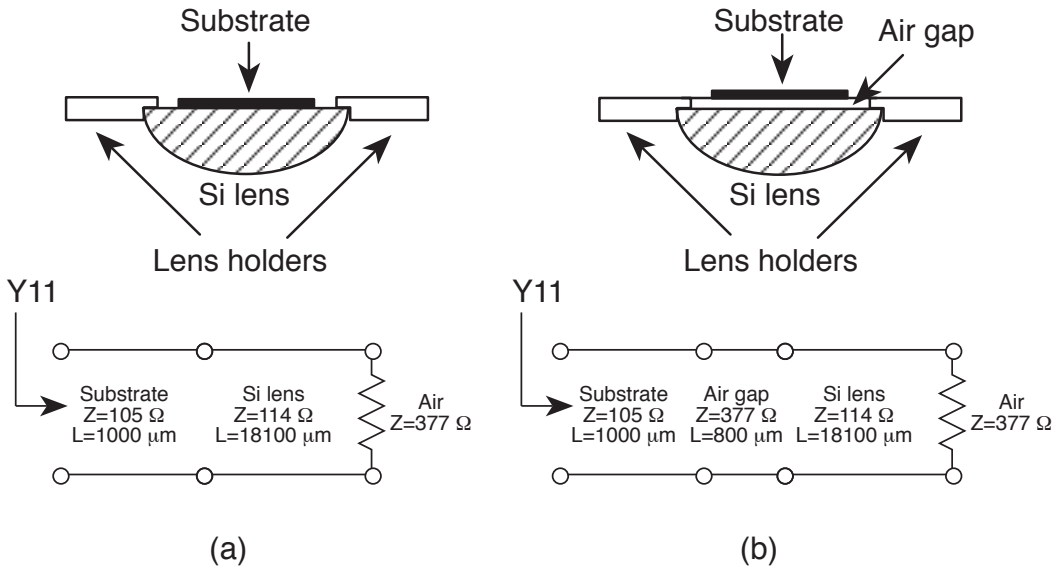

Figure 6.26: (a) Si lens resonant cavity, and (b) Hybrid cavity formed by creating an air gap. The cavities are modeled as transmission lines to obtain input admittance Y_{11} as a function of frequency.

be replaced by an equivalent transmission line of impedance $Z = 377\ \Omega/\sqrt{\epsilon_{r,sub}}$, and length L equal to the dielectric thickness. The total input admittance Y_{11} can be now calculated assuming a free-space load impedance of 377 Ω. For simplicity, the SRTD array is assumed to be a purely negative resistance (G_n) element in the vicinity of the resonant frequency of the slot antenna. With the cavity models included, the conditions for oscillation occur at frequencies where $Im[Y_{11}]$ goes to zero and $Re[Y_{11}] < G_n$. As can be seen from the plots of $Re[Y_{11}]$ (figure 6.27) and $Im[Y_{11}]$ (figure 6.28), cavity modes exist where the oscillation conditions can be satisified only at some frequencies. In the presence of several cavity modes, the probability of oscillation will be higher at that mode where the $Re[Y_{11}]$ reaches the lowest value as this corresponds to a mode with the highest gain. In the Si lens resonant cavity (without the air gap), there is no preference of one cavity mode over the other as can be seen by the periodicity of $Re[Y_{11}]$ and $Im[Y_{11}]$. Therefore, the different array elements could oscillate at any one of the cavity modes within the bandwidth limited by the Q of the on-wafer slot antenna. However, with the introduction of the air gap, the number of cavity modes is reduced as can be seen from figures 6.27, and 6.28. The plots of $Re[Y_{11}]$ and $Im[Y_{11}]$ for the hybrid cavity (with air gap) become skewed.

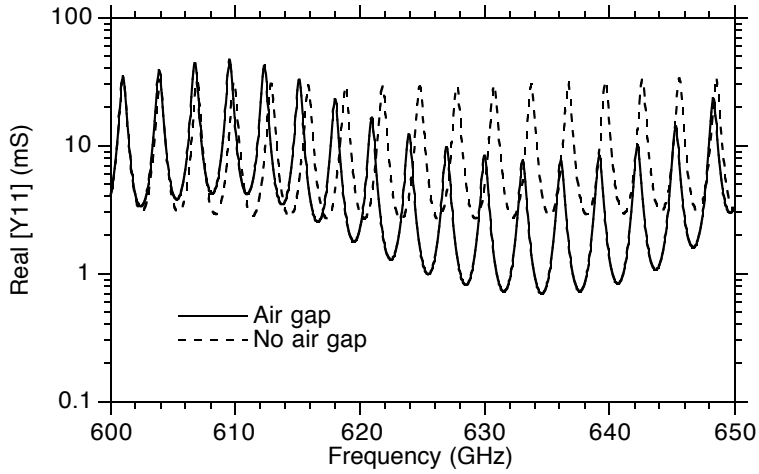

Figure 6.27: Real part of admittance calculated for transmission model of the two cavities. $Re[Y_{11}]$ for the hybrid cavity is skewed, favoring oscillations in the frequency range 630-640 GHz.

$Re[Y_{11}]$ reaches minimum values in the frequency range 630-640 GHz. Therefore, the probabilty of oscillation is higher in this frequency range. Simultaneously, $Im[Y_{11}]$ has reduced number of zero crossing points in this frequency range. Therefore, the number of cavity modes is reduced in the hybrid cavity leading to a more favorable situation for synchronization of array elements.

Scanning Fabry-Perot measurements were obtained with the hybrid cavity for the 800G3U8×8 array. Suppression of the multiple peaks in the bolometer output was achieved and a distinct peak to peak separation could be measured (figure 6.29). Peak to peak separation was measured as 0.23 mm which corresponds to an oscillation frequency of 650 GHz .

The bolometer output signal was observed to drop as the signal frequency increased. Also, the alignment of various parts became more critical as the signal frequency increased. Other oscillator array designs could not be tested either due to the poor yield of the SRTDs or due to the inability to detect signals beyond 700 GHz. The designs at 700 GHz and 800 GHz were found to oscillate at lower frequencies than designed. For designs beyond 500 GHz, the SRTD device size inclusive of all its pads and the MIM capacitor dimensions becomes a significant portion of the slot antenna length. The physical layout thus no longer conforms

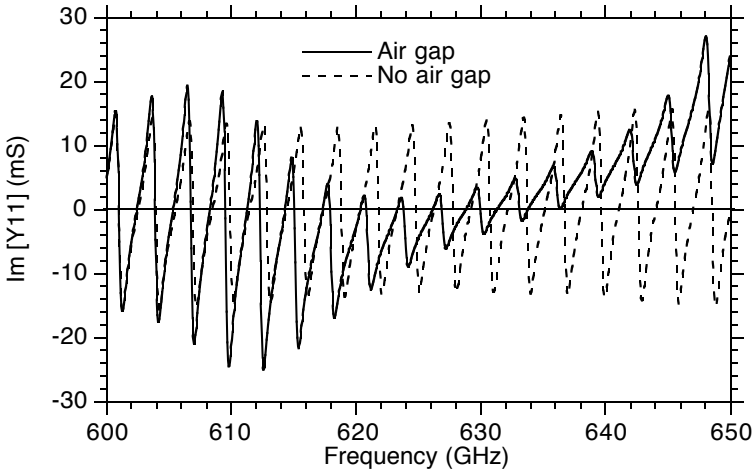

Figure 6.28: Imaginary part of admittance calculated for transmission model of the two cavities. $Im[Y_{11}]$ for the hybrid cavity is skewed, with reduced number of zero crossings in the frequency range 630-640 GHz.

well to a simple slot antenna. The parasitics associated with the SRTD mesas and the capacitor require a careful modeling, perhaps as distributed structures. This was not accounted during the various circuit designs as the intention in this first attempt at submmm-wave oscillators was to keep the oscillator design as simple as possible. A summary of the frequency measurements of all the oscillator array designs that were tested successfully is included in the table 6.2.

Thus, frequency measurements of the oscillator arrays successfully proved oscillation frequencies at 94, 109, 196, 290, 300, 310, 470, 560 and 650 GHz (table 6.2). These are record results in many respects. These are the first demonstration of monolithic slot antenna coupled RTD oscillators and monolithic RTD arrays. The oscillator arrays beyond 290 GHz represent the highest frequency monolithic oscillators built to date [3]. Only one waveguide oscillator at 712 GHz [8] is known to have a higher oscillation frequency than the 650 GHz oscillation frequency obtained here. Despite the simple models used in the circuit design, oscillator arrays to 500 GHz were very close to the design frequency. This is in contrast to previous results with 200 GHz HEMT oscillators [3] which were off by at least 50% in the oscillation frequencies.

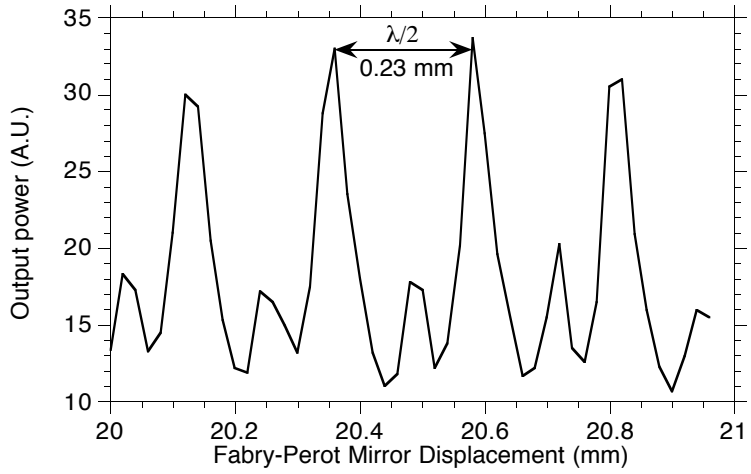

Figure 6.29: Bolometer output as a function of Fabry-Perot mirror displacement for the 64-element array at 800 GHz with a hybrid cavity. The hybrid cavity has fewer cavity modes favoring locking of the oscillations of different array elements to a single frequency.

Design	Design f_{osc} (GHz)	No. of array elements	SRTD area (μm^2)	V_{bias} (V)	I_{bias} (mA)	Osc. Freq (GHz)
100G8U2×1	100	2	1.6	1.00	20.0	109
100G2U4×4	100	16	3.2	4.60	10.0	94
200G8U2×1	200	2	1.6	1.10	23.3	196
300G8U2×1	300	2	1.6	1.10	25.0	310
300G4U4×4	300	16	6.4	4.40	17.9	290
300G8U4×4	300	16	12.8	4.25	38.6	300
500G4U4×4	500	16	6.4	4.30	22.6	470
700G4U4×4	700	16	6.4	4.25	19.6	560
800G3U8×8	800	64	19.2	8.50	33.4	650

Table 6.2: Summary of frequency measurements of various oscillator array designs

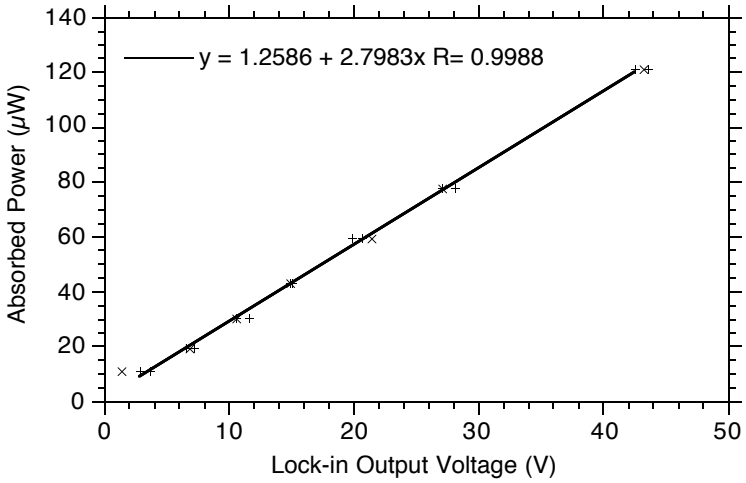

Figure 6.30: Calibration curve for the Thomas Keeting thermo acoustic power detector. The power absorbed in the resistive metal film is plotted against the lock-in output voltage.

6.6 Power measurements

Calibrated power measurements were necessary to establish the power levels of these oscillator arrays. A Thomas Keeting thermo-acousitic power detector was used for this purpose. The Thomas Keeting is a much less sensitive detector than the Ge bolometer, but a calibrated power measurement can be obtained. The thermo-acoustic power detector consists of a resistive metal film in an electromagnetically transparent acoustic chamber. The resistance of the metal film is 219 Ω. Thermal energy from the incident mm-wave radiation dissipated in this resistor leads to pressure variations in the acoustic chamber, causing acoustic vibrations. The energy in the acoustic vibrations are measured by a transducer, a lockin amplifier and a mechanical chopper. For calibration of the Thomas-Keeting, a voltage pulse is applied to the resistive film from a 50 Ω source. From the known values of the source and load resistances, the power dissipated in the resistor can be calculated. A calibration curve between the power absorbed by the resistive metal film and the corresponding lockin output voltage can be thus obtained (figure 6.30). When RF signals from the SRTD oscillator array are incident on Thomas Keeting at roughly the Brewster's angle, $\approx 50\%$ of the inci-

dent power is absorbed by the resistive film. From the measured lockin output voltage and the calibration curve, the power absorbed in the resistive film can be obtained.

With this measurement set up, power from a 300G4U4×4 oscillator array was measured. Earlier, oscillation frequency of 290 GHz was determined for this array. Lock- in output voltage was measured with and without DC bias on the oscillator array. The measurement without DC bias (zero bias) corresponds to the power absorbed from the background radiation, while the measurement with bias corresponds to the sum of the absorbed RF signal power and the power from the background radiation. From these measurements and the Thomas Keeting calibrated characteristics, a signal power of 28.0 μW was measured for the oscillator array. Also, 12 different calibrated power measurements were obtained at short intervals of time to determine a $\pm$ 2.0 μW variation in the 28.0 μW measured output power. Therefore, a 28.0 $\pm$ 2.0 μW was measured for the 300 GHz oscillator array. This corresponds to a 440 W/cm^2 output power density as normalized to the total SRTD junction area. It is important to point out that this power measurement is a strict and a conservative lower limit on the oscillator output power as the measured power level does not account for significant losses (reflection and diffraction) in the beam path. The actual power level of the 300 GHz oscillator array could be at least a factor of 2-3 higher. Power levels of the higher frequency oscillator arrays could not be determined as the signal levels were close to the threshold levels of the Thomas Keeting detector. However, a rough cross calibration between the sensitive bolometer readings and the calibrated thermo-acoustic detector readings for the 300 GHz array yields a rough estimate of 2.0 μW for the output power of the 650 GHz oscillator array. Direct electrical connection to the individual SRTDs of the submm-wave oscillator arrays was not possible in the various designs. Therefore, it is difficult to conclusively establish that every array element is oscillating and that power from individual oscillators is combining. However, except for the 100 GHz designs (where both the 2-element and the 16-element arrays have similar SRTD junction areas) the uncalibrated detected signal levels of the 16-element oscillator arrays are an order of magnitude larger than the 2-element arrays. In future designs, some arrays could be designed with separate bias connections to individual rows. Then, by measuring the uncalibrated detected signal levels as a function of the number of biased rows, it may be possible to conclusively prove quasi-optical power combining of larger arrays.

In this chapter, the fabrication and testing details of the submm-wave SRTD oscillator arrays was described. The SRTD oscillator arrays were fabricated in a

8 mask layer IC process that achieves monolithic integration of various array elements. A significant process development was required to overcome the various problems encountered during array fabrication. After successful array fabrication, extensive testing of the various oscillator circuits was required to establish oscillation frequencies and output power levels. A quasi-optical measurement system was set up for this purpose. Oscillations to 200 GHz were proved by detecting the signals with a broad band bowtie-antenna-coupled Schottky-diode operating as a harmonic mixer. Oscillations beyond 200 GHz were proved by a liquid Helium cooled Ge bolometer and a scanning Fabry-Perot interferometer. Oscillation frequencies for different array designs were determined as 94, 109, 196, 290, 300, 310, 470, 560 and 650 GHz. Also, a calibrated power measurement of 28.0 $\pm$ 2.0 μW was determined for a 300 GHz oscillator array. Power measurements of higher frequency designs could not be obtained as the signal levels were close to the detector's threshold.

Chapter 7

Conclusion

Monolithic submm-wave RTD oscillator arrays were demonstrated for the first time. The oscillator arrays incorporate 2.2 THz f_{max}, InGaAs Schottky-collector resonant tunnel diodes and on-wafer bias stabilization techniques, both developed in the course of this thesis. A 64-element array oscillated at 650 GHz. A calibrated power measurement indicated at least 28 μW signal for a 300 GHz oscillator array. In this chapter, the important goals achieved in this project are summarized. Improvements are suggested to reach the ultimate goal of 1.0 to 1.5 THz local oscillators for far infra-red heterodyne receivers.

7.1 Achievements

A new type of RTD known as Schottky-collector resonant tunnel diode was proposed. The SRTD modifies the electron collection mechanism in the device by replacing the Ohmic-collector of a conventional RTD by a direct Schottky-collector to the space-charge region. This leads to a dramatic reduction in the parasitic resistance of the device, first by elimination of top Ohmic contact resistance and then by reduction of periphery-dependent bottom Ohmic contact resistance through deep submicron scaling of the Schottky-collector. The reduced parasitic resistance in the device leads to large improvements in the RTD bandwidths. 0.1 μm SRTDs were fabricated in the InGaAs system. First, an MBE layer structure was designed through iterative cycles of growth and DC characterization of the material. A sophisticated airbridge e-beam lithography process was next developed at JPL for fabricating submicron SRTDs. From the measured DC and microwave parameters, the 0.1 μm SRTDs with 5ML AlAs barriers had an estimated f_{max} of 2.2 THz. Although such high f_{max} estimates

cannot be verified experimentally, these numbers represent at least a 2 : 1 improvement in the RTD bandwidths in the InGaAs material system, and 1.8 : 1 improvement over any prior RTD.

In the next phase of the project, a on-wafer bias stabilization technique was proposed to address the problems associated with DC bistability and parasitic bias circuit oscillations of submm-wave RTD oscillators. The bias stabilization technique requires a low-impedance bias stabilizer located within a distance of $\lambda_{osc}/4$ from the SRTD, where λ_{osc} is the wavelength corresponding to the oscillation frequency. With the bias stabilization technique, the problems associated with DC bistability and parasitic bias circuit oscillations are eliminated without any constraints on the maximum RTD area or output power. The bias stabilization technique was first demonstrated by constructing a hybrid microwave oscillator. The hybrid oscillator was realized by ribbon bonding a SRTD and a bias stabilizer Schotkky-diode. Oscillations were observed at 6.9 GHz without any problems of parasitic bias circuit oscillations or DC bistability. Implementation of bias stabilization at submm-wave frequencies demands an on-wafer bias stabilizer. For this, a graded band gap AlInAs Schottky-diode was integrated into the SRTD layer structure. MBE layer structure for fabricating both SRTDs and Schottky- diodes on the same wafer was designed through iterative cycles of growth and DC characterization of the material.

Slot antenna coupled submm-wave SRTD oscillators were then designed. These incorporate 0.1 μm InGaAs SRTDs and on-wafer Schottky-diode bias stabilizers. Oscillator arrays consisting of several single element oscillators were also designed to obtain significant power levels at submm-wave frequencies. The oscillator arrays were fabricated in a 8 mask layer IC process. The process achieved monolithic integration of 0.1 μm InGaAs SRTDs, graded bandgap AlInAs Schottky-diodes, slot antennas, MIM capacitors, N++ resistors and airbridges. Oscillator arrays were tested in a quasi-optical measurement system. For arrays oscillating below 200 GHz, a mm-wave transmitter receiver system consisting of Schottky-diode harmonic mixer was utilized. Higher frequency designs required a more sensitive detector. A Ge bolometer and a scanning Fabry-Perot interferometer were employed for testing designs oscillating above 200 GHz. With these two methods, oscillation frequencies were determined at 94, 109, 196, 290, 300, 310, 470, 560 and 650 GHz for different array designs. The oscillation frequencies below 500 GHz were close to the design values. For designs above 500 GHz, the dimensions of the SRTD mesas and MIM capacitors become significant portion of the slot antenna. The physical layout no longer conforms to a simple slot antenna design which explains the discrepancy between design

and measured oscillation frequencies beyond 500 GHz. Despite this, these results represent the highest oscillation frequencies for monolithic oscillators built to date.

Also, calibrated output power levels were measured with a thermo-acoustic detector. A 16-element array produced 28 ± 2 μW at 300 GHz. This represents a power density of 440 W/cm^2 as normalized to SRTD junction area. Both these represent record power levels for RTD oscillators in the vicinity of 300 GHz. Calibrated power measurements of higher frequency oscillator arrays could not be obtained as the signal levels were close to the detector's threshold.

7.2 Future Work

Several improvements are possible after the first successful demonstration of submm- wave SRTD oscillators. Firstly, improvements to the SRTD are necessary to prevent device burn out at the high operating current densities. The peak voltage of the SRTD needs to be reduced. A strained InAs quantum-well will lower the bound state energy level, thus reducing the voltage necessary to achieve resonance [27]. Next, a AlInAs heterobarrier cap could replace the P-cap layer for suppression of parasitic leakage currents. The AlInAs layer could be removed beneath the 0.1 μm Schottky-collecor through selective etching. This would lower the peak voltages in the SRTD. The P-cap etch could not be well controlled in this project and hence the SRTDs were fabricated with larger peak voltages. Higher current densities can also be attempted by thinning the barriers further which could improve the RTD bandwidths.

The first SRTD oscillators were, by intent, very simple unsophisticated designs. Given the significant variability of the SRTD parameters in an evolving technology, oscillators were designed with the criterion of maximizing the probability of oscillations, without regard to output power, spectral linewidths or efficiency. Future work could address these issues in detail.

In the first attempt at submm-wave SRTD oscillators, the slot antennas were used as both resonating as well as radiating elements. This results in a reduction of the slot antenna from its resonant length required to tune the SRTD capacitance. Operating away from slot antenna resonance reduces both its radiation conductance as well as its radiation efficiency. CPW inductive elements could be utilized to tune the SRTD capacitance which would allow operation of the slot antenna close to its resonance thus improving its efficiency.

Oscillation frequencies can be increased beyond 650 GHz by shrinking the dimensions of other array elements with respect to the slot antenna. The highest

oscillation frequency is currently limited by contact lithography mask design rules. The current design rules impose limits on the dimensions of various circuit elements leading to SRTD mesa and MIM capacitor sizes comparable to the slot antenna. Projection lithography will allow shrinkage of mask design rules due to tighter alignment tolerances. The physical layout of the slot antenna coupled oscillator would then conform to a simple slot antenna design up to 1.0 THz. Also, reducing the thickness of silicon nitride dielectric would yield larger capacitance per unit area leading to a shrinkage of capacitor dimensions.

Oscillator output powers can also be increased by increasing the number of array elements. Increasing the array size to at least 100×100 will increase the output power by over $100:1$. Larger arrays can produce more collimated radiation, facilitating coupling to an external confocal cavity, thereby enabling tuning of the oscillator. Anti reflection coating of the Si lens will improve coupling of the oscillator power to the external cavity. Phase noise improvements can also be obtained by larger arrays. Finally, the use of Schottky-diode varactors in the oscillator array will allow phase-locking. These measures should increase the output powers and reduce the spectral linewidths to $\approx$ 10-100 KHz.

These improvements should lead to the ultimate goal of robust solid state signal sources for far infra-red heterodyne receivers.

Appendix A

SRTD Layer Structure

Program for MBE growth of SRTD layer structure.

```
1 !SRTD STRUCTURE FOR M. REDDY
2 !6 ML ALAS BARRIERS, GROWTH RATE OF ALAS IS ML/SEC
3 !T SUB = 540 C BUFFER = 510 C TUNNEL REGION
4 EXPAND
5 !SI SET PT. FOR 1E19 CM-3
6 TEMPERATURE Si=1450.1
7 !BE SET PT. FOR 5E18 CM-3
8 TEMPERATURE Be=922.2
9 GROWTH RATE In,Ga=3.273
10 GROWTH RATE Al1=.5152
11 ROTATION 15
12 REPEAT 10
13 LAYER In,Ga THICKNESS=96 DOPE=Si
14 CLOSE
15 PYROSET=540
16 END REPEAT
17 CLOSE
18 REPEAT 4
19 LAYER In,Ga THICKNESS=455 DOPE=Si
20 CLOSE
21 PYROSET=540
22 END REPEAT
23 REPEAT 6
24 LAYER In,Ga THICKNESS=1203 DOPE=Si
```

```
25 CLOSE
26 PYROSET=540
27 END REPEAT
28 !SI SET PT. FOR 1E18 CM-3
29 TEMPERATURE Si=1354.4
30 REPEAT 3
31 PYROSET=510
32 DELAY 1 Minutes
33 CLOSE
34 END REPEAT
35 LAYER In,Ga THICKNESS=400 DOPE=Si
36 CLOSE
37 READ PYROMETER
38 ROTATION 25
39 !REDUCE SUBSTRATE DOWN TO 320 C (PYRO)
40 TEMPERATURE SUBSTRATE=460
41 DELAY 6 Minutes
42 CLOSE
43 LAYER In,Ga THICKNESS=100 DOPE=Si
44 LAYER In,Ga THICKNESS=100
45 CLOSE
46 !RESET SUBSTRATE TEMPERATURE TO 510 C (PYRO)
47 TEMPERATURE SUBSTRATE=530
48 DELAY 1 Minutes
49 CLOSE
50 TEMPERATURE SUBSTRATE=585
51 DELAY 1 Minutes
52 CLOSE
53 TEMPERATURE SUBSTRATE=625
54 DELAY 1 Minutes
55 CLOSE
56 PYROSET
57 DELAY 1 Minutes
58 CLOSE
59 LAYER Al1 THICKNESS=6
60 LAYER In,Ga THICKNESS=41
61 LAYER Al1 THICKNESS=6
62 REPEAT 2
```

```
63 LAYER In,Ga THICKNESS=125
64 CLOSE
65 PYROSET=510
66 ROTATION 15
67 END REPEAT
68 LAYER In,Ga THICKNESS=100 DOPE=Be
69 CLOSE
70 READ PYROMETER
71 TEMPERATURE SUBSTRATE=200
72 DELAY 7 Minutes
73 ROTATION 0
74 PRINTDATA
```

Appendix B

Material Characterization

Process flow for material characterization of SRTDs.

B.1 Self Aligned Emitter Ohmics

Mask Layer: Ohmics, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak for 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Recess Etch to N++ Layer**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant atleast 15 min. before the etching.
2. Etchant composition is $H_3PO_4 : H_2O_2 : H_2O :: 3 : 1 : 4$.
3. Use magnetic stirrer bar at 300-400 rpm to agitate solution.
4. Mix 15 ml of H_3PO_4 to 250 ml of water and stir well. Add 5 ml of H_2O_2 to the etchant and stir well.
5. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$ in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Blow dry with N_2.
10. Etch in $H_3PO_4 : H_2O_2 : H_2O$ solution for 20 to 30 seconds.
Etch rate is $\approx$1000 Å/min.
11. Rinse in running DI for 3 min.
12. Blow dry with N_2.
13. Use Dektak to determine etch depth and rate.
14. Continue etching in steps of 30 sec to get to the N++ layer.

G **Metal Evaporation**

1. Load sample into E-beam evaporator immediately after the recess etch.
2. Place wafer in E-Beam mount.
3. Make sure the crystal monitor reads < 10; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ge	108	2-3	1.75
Au	102	2-3	1.45
Ge	63	2-3	1.75
Au	236	2-3	1.45
Ni	100	1-2	1.75
Au	1400	≈5	1.55

Note: If the thickness have not been quite right for the first 3 layers, adjust the thickness of the 4^{th} layer (Au) to get the correct stochiometric ratio of Ge:Au=1:1.977 for the first 4 layers.

H **Liftoff**

Important Note: DO NOT LET ACETONE DRY ON WAFER.

1. Suspend wafer with a teflon basket or 2-inch wafer holder in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff.
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse with METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

I **Rapid Thermal Annealing**

1. Prepare RTA by loading the program for 360° C, 10 sec anneal. Also make sure forming gas is flowing at the prescribed rate and pressure.
2. Run the program several times until the temperature stabilizes at 360° C, during the 10 sec period.
3. Load the wafer on Si wafer holder and run the program.
   Caution: After anneal and trial runs, turn off the forming gas and use a face mask before opening the chamber.

4. Rinse wafer in DI for 2 min.
5. Blow dry with N_2.
6. Inspect under microscope. You should be able to see the change in surface morphology.
7. Measure TLM pattern, should get $R_C \approx 12\Omega - \mu$m and $R_{SH} \approx 1 - 2\Omega/\Box$.
8. If you don't get typical values $\pm 50\%$, consider changing the program.

B.2 Silicon Dioxide Vias

Mask Layer: SiO_2 Vias, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Silicon dioxide Deposition**

1. Clean the PECVD chamber and deposit SiO_2 on the chamber walls using the program 30CLNSIO.

2. Load the PECVD with a dummy GaAs wafer. Run the program SIO10 to deposit 1000 Å of SiO_2. The surface of the wafer should be roughly blue in color.
3. Use ellipsometer to measure film thickness (≈1000 Å) and refractive index ≈ 1.49.
4. Repeat the deposition procedure on the real wafer, if the desired thickness and refractive index are obtained on the dummy wafer.

C **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. HMDS vapors are very harmful and the HMDS bottle should always be covered. Never breathe if you put your head under the hood.

1. Cool down after PECVD deposition for 10 min.
2. Expose wafer to HMDS vapors for 10 min. by placing a big beaker over the wafer and the HMDS bottle.
3. Wafer on spinner chuck with vacuum. Blow with N_2.
4. Apply AZ P4110 with syringe and filter to cover wafer.
5. Spin at 6 krpm for 30 sec.
6. Soft Bake in oven at 90° C for 30 min. in petri dish without cover.

D **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

E **Development**

1. Mix fresh developer, AZ 400K : DI :: 1:4
2. Develop for 60 sec.
3. Rinse in running DI water for 3 min.

4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.
6. Make sure that atleast some of the smallest features 1.0 μm$\times$1.0 μm and 1.0 μm$\times$1.5 μm have opened up.

F **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 25 sec.

G **SiO_2 BHF Etch**
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

1. Put wafer in straight Buffered HF (BHF) for 10 sec.
2. Rinse in running DI for 3 min.
3. Blow dry with N_2.
4. Inspect under microscope.
5. Etch again in 2 sec. intervals if necessary till SiO_2 is completely etched in all vias.

H **Photoresist Stripping**
Important Note: DO NOT LET ACE DRY ON WAFER.

1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes $\approx$ 2-5 min.).
2. Squirt ACE on wafer with squirt bottle.
3. Squirt rinse in METH followed by ISO.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. Examine under microscope to check whether smallest features have opened up and whether SiO_2 has been completely removed in all vias.

B.3 Schottky-Collector and Pad Metal

Mask Layer: Schottky, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.

2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Metal Evaporation**

1. Surface preparation by dipping in dilute NH_4OH:H_2O (1:10) for 20 sec.
2. Blow dry with N_2.
3. Load sample into E-beam evaporator immediately.
4. Place wafer in E-Beam mount.
5. Make sure the crystal monitor reads < 10; change if necessary.
6. Pump down to at least $7\times\ 10^{-7}$ Torr.
7. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.70
Pt	500	2-3	1.95
Au	3000	$\approx$ 10-15	1.55

G **Liftoff**
Important Note: DO NOT LET ACETONE DRY ON WAFER.

1. Suspend wafer with a teflon basket or 2-inch wafer holder in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff.
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse in METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

Appendix C

Submicron SRTDs

Process flow for fabrication of submicron SRTDs.

C.1 Self Aligned Emitter Ohmics

Mask Layer: Ohmics, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 60 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 secec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Recess Etch to N++ Layer**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant atleast 15 min. before the etching.
2. Etchant composition is $H_3PO_4 : H_2O_2 : H_2O :: 3 : 1 : 4$.
3. Use magnetic stirrer bar at 300-400 rpm to agitate solution.
4. Mix 15 ml of H_3PO_4 to 250 ml of water and stir well. Add 5 ml of H_2O_2 to the etchant and stir well.
5. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$ in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Etch in $H_3PO_4 : H_2O_2 : H_2O$ solution for 20 to 30 sec.
   Etch rate is $\approx$1000 Å/min.
10. Rinse in running DI for 3 min.
11. Blow dry with N_2.
12. Use Dektak to determine etch depth and rate.
13. Continue etching in steps of 30 sec to get to the N++ layer.

G **Metal Evaporation**

1. Load sample into E-beam evaporator immediately after the etch.
2. Place wafer in E-Beam mount.
3. Make sure the crystal monitor reads < 10; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/s.)	Approx. Vernier
Ge	108	2-3	1.75
Au	102	2-3	1.45
Ge	63	2-3	1.75
Au	236	2-3	1.45
Ni	100	1-2	1.75
Au	1400	≈5	1.55

Note: If the thickness have not been quite right for the first 3 layers, adjust the thickness of the 4^{th} layer (Au) to get the correct stochiometric ratio of Ge:Au=1:1.977 for the first 4 layers.

H **Liftoff**

Important Note: DO NOT LET ACETONE DRY ON WAFER.

1. Suspend wafer with a teflon basket or 2-inch wafer holder in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff.
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse with METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

I **Rapid Thermal Annealing**

1. Prepare RTA by loading the program for 360° C, 10 sec anneal. Also make sure forming gas is flowing at prescribed the rate and pressure.
2. Run the program several times until the temperature stabilizes at 360° C, during the 10 sec period.
3. Load the wafer on Si wafer holder and run the program.
   Caution: After anneal and trial runs, turn off the forming gas and use a face mask before opening the chamber.

4. Rinse wafer in DI for 2 min.
5. Inspect under microscope. You should be able to see the change in surface morphology.
6. Measure TLM pattern, should get $R_C \approx 12\Omega - \mu$m and $R_{SH} \approx 1 - 2\Omega/\Box$.
7. If you don't get typical values $\pm 50\%$, consider changing the program.

end list

C.2 Airbridge Submicron Schottky-Collector

Ebeam lithography at JPL

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **E-beam Trilayer Resist Application**

1. Inspect the ohmics to determine whether adjustments are necessary to account for roughness or variation from designed dimensions.
2. Surface clean in HCl : DI :: 1:100 for 30 sec.

3. Blow dry with N_2 for 30 sec.
4. Spin coat first layer of PMMA (496K, 2.5% solids in cholorbenzene). A premixed 4% solution is thinned using a premixed 1% solution to arrive at the 2.5% solution.
5. A dynamic dispense speed of 500 rpm, followed by sond spread speed of 1200 rpm for 2 s followed by a final spin speed of 4000 rpm for 30 sec.
6. Bake on hot plate at 115° C for 60 sec.
7. Cure on hot plate at 170° C for 15 min.
8. Cool down the sample for 10 min.
9. Spin coat the sond layer consisting of PMMA methacrylic acid coploymer (PMMA/MAA, 9%) using the same spin, bake and cure conditions as the first layer (Steps 5 to 8).
10. Spin coat a final layer of PMMA (premixed, 950K, 2%) using the same spin, bake and cure conditions as the first layer (Steps 5 to 8).

C **E-beam Exposure**

E-beam system: A JEOL JBX 5DII running at 50 KV using aperture 2 in the 5th lens with a beam current of 200 pA. The pattern is written as rectangles rather than lines and uses a step size of 10.

1. High dose of ≈290 μC/cm^2 for defining the Schottky-collector foot print.
2. Lighter dose of ≈70-80 μC/cm^2 to define the T- structure and the air bridge.
3. Moderate dose of ≈90 μC/cm^2 to define the contact area to the ohmic-metal pad.

D **Development**

1. Sample dipped in Chlorobenzene for 15-17 s with the anodes oriented horizontally.
2. Toluene rinse for 5 sec followed by Toluene spray for 10 sec.
3. Steps 1 and 2 develop the top layer of PMMA.
4. Sample immersed for 2 min. in a 1:1 mixture of Isopropyl alcohol (IPA) and methanol agitated by a magnetic stirrer bar rotating at ≈100 rpm. This step dissolves the exposed copolymer layer and also undercuts the top layer of PMMA slightly.

5. Sample immersed for 2 min. in a 1:1 mixture of methyl isobutyl ketone (MIBK) and IPA agitated by a magnetic stirrer bar. This step dissolves the exposed regions of bottom layer of PMMA.
6. Rinse in IPA followed by a blow dry with N_2.
7. SEM inspection at an accelerating voltage of 2 KV. An addtional MIBK:IPA develop is done if development is incomplete.

E **Oxygen Plasma Photoresist Descum**

1. 500 mTorr of O_2.
2. Power = 50W at low frequency.
3. Run for 30 sec.

F **Surface Preparation**

1. 10 sec dip in IPA : DI :: 1 : 10 to improve surface wetting.
2. 20 sec dip in NH_4OH : H_2O :: 1 : 30.
3. Rinse in DI for 30 sec.
4. 30 sec dip in buffered oxide etch (BOE) to remove surface oxides.
5. Rinse in DI for 30 sec.
6. 15-20 sec etch in H_2O_2 : Citric Acid : DI :: 1 : 11 : 44.
7. Rinse in DI for 30 sec.
8. 20 sec dip in NH_4OH : H_2O :: 1 : 30.
9. Blow dry with N_2.

G **Metallization**
Important Note: LOAD EVAPORATOR IMMEDIATELY AFTER SURFACE PREPARATION.

1. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/s.)
Ti	300	1-2
Pt	300	1-2
Au	3000	3-7

H **Liftoff**
Important Note: DO NOT LET ACE DRY ON WAFER

1. Immerse in a beaker of ACE sitting in a hot bath at 60° C.
2. Rinse in METH.

3. Rinse in running DI water.
4. Blow dry with N_2.

C.3 Mesa Isolation

Mask Layer: Mesa, Light Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4210 with syringe and filter to cover wafer.
4. Spin at 5.5 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 12 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 90 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 secec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Hard Bake**

1. Hard bake in oven at 120° C for 30 min. in petri dish without cover.
2. This step hardens the resist and rounds off the edges of the photoresist.

G **Isolation Etch**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant atleast 15 min. before the etching.
2. Etchant composition is H_3PO_4 : H_2O_2 : H_2O : : 3 : 1 : 4.
3. Use magnetic stirrer bar at 300 -400 rpm to agitate solution throughout this step.
4. Mix 15 ml of H_3PO_4 to 250 ml of water and stir well. Add 5 ml of H_2O_2 to the etchant and stir well.

5. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$ in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Etch in $H_3PO_4 : H_2O_2 : H_2O$ solution for 60 sec.
   Etch rate is ≈1000 Å/min.
10. Rinse in running DI for 3 min.
11. Blow dry with N_2.
12. Use Dektak to determine etch depth and rate.
13. Continue etching till the semi-insulating InP layer is reached. This is observed by a color change of the wafer and the diasppearance of the MBE ring at the edges of the wafer.
14. Probe a few SRTDs and measure DC charactersitics to verify whether the isolation has been achieved between the active and passive mesas.
15. Overetching is almost always required to etch away the semiconductor beneath the airbridge submicron Schottky collector. The usual overetch time is ≈10-15 mins.
16. Repeat the etching and DC probing till the devices show isolation between active and passive mesas. Isolation etch is complete when the DC probing indicates that there is no current flow near about zero volt. At this point, the complete sweep of DC characteristics will show NDR region of the SRTDs.
17. SEM inspection to observe whether all the material has been etched between the active and passive mesas of all SRTDs across wafer.

H **Photoresist Stripping**
Important Note: DO NOT LET ACETONE DRY ON WAFER

1. Immerse wafer in a beaker of ACE with magnetic stirrer bar set at a high rpm.
2. Leave the wafer in ACE for at least 10 min.
3. Squirt rinse in METH followed by ISO.
4. Rinse in DI for 3 min.
5. Blow dry with N_2.

6. Examine under microscope. If any photoresit scum is visible go to the next step, other wise the isolation step is complete.
7. Immerse wafer in hot 1165 (photoresist stripper) at 100 ° C for 3-5 min.
8. Soak wafer in ISO for 5 min.
9. Rinse in DI for 3 min.
10. Blow dry with N_2.

C.4 Interconnect Metal

Mask Layer: Interconnect, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.

4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 secec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Metal Evaporation**

1. Surface preparation by dipping in dilute NH_4OH:H_2O (1:10) for 20 sec.
2. Blow dry with N_2.
3. Load sample into E-beam evaporator immediately.
4. Place wafer in E-Beam mount.
5. Lower the boom to get $\approx$ 3.0 times the evaporation rates.
6. Make sure the crystal monitor reads < 10; change if necessary.
7. Pump down to at least $7\times\ 10^{-7}$ Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	65	2-3	1.70
Pt	165	2-3	1.95
Au	4000	$\approx$ 10-15	1.55

G **Liftoff**

Important Note: DO NOT LET ACETONE DRY ON WAFER.

1. Suspend wafer with a teflon basket or 2-inch wafer holder in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff.
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse in METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.
8. SEM inspection to verify whether the step coverage of metal over the mesa eges has been achieved.

Appendix D

Oscillator Layer Structure

Program for MBE growth of oscillator layer structure.

Program A is used to determine the setpoint offset by initiating the growth of 4000 Å of the Schottky-diode N++ layer. Then the growth is interrrupted for 5 min. Program B is then run with the precisely determined setpoint offsets (from program A) and growth interruption times.

PROGRAM A

```
1 !SRTD STRUCTURE + STABILIZER DIODE FOR M. REDDY
2 !USING Al1 SOURCE AS ALUMINIUM SOURCE
3 !T SUB = 540 C BUFFER = 510 C TUNNEL REGION
4 !PART ONE FOR SUBSTRATE BUFFER AND OFFSET
DETERMINATION
5 EXPAND
6 !SI SET PT. FOR 1E19 CM-3
7 TEMPERATURE Si=1342.1
8 TEMPERATURE Be=800
9 GROWTH RATE In,Ga=3.455
10 GROWTH RATE Al1=.578
11 GROWTH RATE Al1,In=3.532
12 ROTATION 15
13 REPEAT 10
14 LAYER In,Ga THICKNESS=96 DOPE=Si
15 CLOSE
16 PYROSET=540
```

17 END REPEAT
18 CLOSE
19 REPEAT 4
20 LAYER In,Ga THICKNESS=455 DOPE=Si
21 CLOSE
22 PYROSET=540
23 END REPEAT
24 LAYER In,Ga THICKNESS=1220 DOPE=Si
25 CLOSE
26 PYROSET=540
27 PRINTDATA

PROGRAM B

1 !SRTD STRUCTURE + STABILIZER DIODE FOR M. REDDY
2 !USING Al1 SOURCE AS ALUMINIUM SOURCE
3 !5 ML ALAS BARRIERS, GROWTH RATE OF ALAS IS ML/SEC
4 !PART TWO AFTER SETTING TEMPERATURE OFFSETS
5 !T SUB = 540 C BUFFER = 510 C TUNNEL REGION
6 EXPAND
7 !SI SET PT. FOR 1E19 CM-3
8 TEMPERATURE Si=1342.1
9 TEMPERATURE Be=800
10 GROWTH RATE In,Ga=3.455
11 GROWTH RATE Al1=.578
12 GROWTH RATE Al1,In=3.532
13 ROTATION 15
14 LAYER In,Ga THICKNESS=1000 DOPE=Si
15 CLOSE
16 PYROSET=540
17 !SI SET PT. FOR 1E18 CM-3
18 TEMPERATURE Si=1268.7
19 REPEAT 3
20 PYROSET=540
21 DELAY 1 Minutes
22 CLOSE
23 END REPEAT
24 LAYER In,Ga THICKNESS=500 DOPE=Si
25 CLOSE
26 !SI SET PT. FOR 1E19 CM-3

```
27 TEMPERATURE Si=1342.1
28 REPEAT 3
29 LAYER Al1,In THICKNESS=3.3
30 LAYER In,Ga THICKNESS=30
31 END REPEAT
32 REPEAT 3
33 LAYER Al1,In THICKNESS=6.7
34 LAYER In,Ga THICKNESS=26.7
35 END REPEAT
36 REPEAT 3
37 LAYER Al1,In THICKNESS=10
38 LAYER In,Ga THICKNESS=23.3
39 END REPEAT
40 REPEAT 3
41 LAYER Al1,In THICKNESS=13.3
42 LAYER In,Ga THICKNESS=20
43 END REPEAT
44 REPEAT 3
45 LAYER Al1,In THICKNESS=16.7
46 LAYER In,Ga THICKNESS=16.7
47 END REPEAT
48 REPEAT 3
49 LAYER Al1,In THICKNESS=20
50 LAYER In,Ga THICKNESS=13.3
51 END REPEAT
52 REPEAT 3
53 LAYER Al1,In THICKNESS=23.3
54 LAYER In,Ga THICKNESS=10
55 END REPEAT
56 REPEAT 3
57 LAYER Al1,In THICKNESS=26.7
58 LAYER In,Ga THICKNESS=6.7
59 END REPEAT
60 REPEAT 3
61 LAYER Al1,In THICKNESS=30
62 LAYER In,Ga THICKNESS=3.3
63 END REPEAT
64 LAYER Al1,In THICKNESS=300
```

```
65 CLOSE
66 PYROSET=540
67 LAYER In,Ga THICKNESS=100
68 LAYER Al1,In THICKNESS=1000
69 REPEAT 4
70 LAYER In,Ga THICKNESS=455 DOPE=Si
71 CLOSE
72 PYROSET=540
73 END REPEAT
74 REPEAT 2
75 LAYER In,Ga THICKNESS=1590 DOPE=Si
76 CLOSE
77 PYROSET=540
78 END REPEAT
79 !SI SET PT. FOR 1E18 CM-3
80 TEMPERATURE Si=1268.7
81 REPEAT 3
82 PYROSET=510
83 DELAY 1 Minutes
84 CLOSE
85 END REPEAT
86 LAYER In,Ga THICKNESS=400 DOPE=Si
87 CLOSE
88 READ PYROMETER
89 ROTATION 25
90 !
91 !TARGET TEMP. SET PT. FOR 320 C (est pyro temp)
92 TEMPERATURE Substrate=356
93 !
94 DELAY 6 Minutes
95 CLOSE
96 LAYER In,Ga THICKNESS=100 DOPE=Si
97 LAYER In,Ga THICKNESS=100
98 CLOSE
99 !
100 !TARGET TEMP. SET PT. FOR 510 C (est pyro temp)
101 TEMPERATURE Substrate=431
102 !
```

```
103 DELAY 1 Minutes
104 CLOSE
105 !
106 TEMPERATURE Substrate=494
107 !
108 DELAY 1 Minutes
109 CLOSE
110 !
111 TEMPERATURE Substrate=530
112 !
113 DELAY 1 Minutes
114 CLOSE
115 PYROSET=510
116 DELAY 1 Minutes
117 CLOSE
118 LAYER Al1 THICKNESS=5
119 LAYER In,Ga THICKNESS=41
120 LAYER Al1 THICKNESS=5
121 REPEAT 2
122 LAYER In,Ga THICKNESS=125
123 CLOSE
124 END REPEAT
125 !GROWTH DELAY OF 9 MIN TO SET BE SET PT. FOR 5E19
CM-3 LEVEL
126 TEMPERATURE Be=927.7
127 REPEAT 3
128 PYROSET=510
129 CLOSE
130 DELAY 3 Minutes
131 END REPEAT
132 ROTATION 15
133 LAYER In,Ga THICKNESS=100 DOPE=Be
134 CLOSE
135 READ PYROMETER
136 TEMPERATURE Substrate=200
137 TEMPERATURE Be=800
138 DELAY 7 Minutes
139 ROTATION 0
```

140 POSITION 1
141 DELAY 10 Seconds
142 PRINTDATA

Appendix E

Oscillator Arrays

Process flow for fabrication of submm-wave oscillator arrays.

E.1 Stabilizer Etch

Mask Layer: Stabilizer Etch, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Mix fresh developer, AZ 400K : DI :: 1:4.
2. Develop for 60 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist is remaining, develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Hard Bake**

1. Hard bake in oven at 120° C for 30 min. in petri dish without cover.
2. This step hardens the resist and rounds off the edges of the photoresist.

G **Non-selective Etch To Separation Layer**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant atleast 15 min. before the etching.
2. Etchant composition is $H_3PO_4 : H_2O_2 : H_2O :: 3 : 1 : 4$.
3. Use magnetic stirrer bar at 300 -400 rpm to agitate solution.
4. Mix 36 ml of H_3PO_4 to 600 ml of water and stir well. Add 12 ml of H_2O_2 to the etchant and stir well.
5. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$ in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Blow dry with N_2.
10. Wet the wafer in DI before dipping into the etchant.
11. Suspend wafer into the etchant ($H_3PO_4 : H_2O_2 : H_2O$) horizontally using the modified teflon basket. The sides of the teflon basket have been trimmed to ensure smooth flow of the etchant over the wafer. Etch for 30 sec.
12. Rinse in DI for 3 min.
13. Blow dry with N_2.
14. Use Dektak to determine etch depth and rate in both small and large areas. Etching should be uniform across the entire wafer. Etch rate is $\approx$1000 Å/min.
15. Determine additional etch depth and time required to reach the top of AlInAs separation layer.
16. Wet the wafer in DI before dipping into the etchant.
17. Suspend wafer into the etchant ($H_3PO_4 : H_2O_2 : H_2O$) horizontally using the modified teflon basket. Etch for the required time in one shot to reach the top of AlInAs separation layer.
18. Rinse in DI for 3 min.
19. Blow dry with N_2.
20. Use Dektak to determine etch depth and rate in both small and large areas. Etching should be uniform across the entire wafer.

21. Determine additional etch depth and time required to reach the top of AlInAs separation layer in all openings across the wafer.
22. Repeat steps 16 to 20 for additional etch time in steps of 15 sec intervals if required.
23. At the end of the non-selective etching, the exposed surface of the etched areas should be the AlInAs separation layer all across the wafer.

H **Selective Etch To Cap Layer**

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant at least 15 min. before the etching.
2. Use magnetic stirrer bar to agitate etchant at 350-400 rpm during the etchant preparation.
3. Solution A is 1 : 1 mixture of HCl : H_2O. Mix 200 ml of HCl to 50 ml of water and stir well for 5 min. with a magnetic stirrer bar.
4. Solution B is a 1 : 1 mixture of acetic acid : HBr. In another beaker, mix a 125 ml of HBr to 125 ml of acetic acid and stir well for 5 min. with magnetic stirrer bar.
5. In a third beaker, mix 250 ml of Solution A to 250 ml of Solution B and stir well with a magentic stirrer bar. This is the A+B etchant.
6. Stop the stirring of the etchant just before suspending the wafer into the A+B etchant. Suspend wafer into the etchant horizontally using a teflon basket whose sides have been trimmed.
7. Etch for 2 min. in A+B etchant.
8. Rinse in DI for 3 min.
9. Blow dry with N_2.
10. Examine both small and large areas under a microscope.
11. Surface looks rough due to etching of AlInAs layer.
12. Repeat steps 6 to 10 till the surface becomes smooth in both small and large areas.
13. Use Dektak to determine etch depth in both small and large areas.

Etching should be uniform across the entire wafer and should have stopped on InGaAs cap layer.

14. At the end of the selective etching, the exposed surface of the etched areas should be the InGaAs cap layer all across the wafer. The color of the etched regions should be the same all across the wafer.

I **Photoresist Stripping**
Important Note: DO NOT LET ACETONE DRY ON WAFER

1. Immerse wafer in a beaker of ACE with magnetic stirrer bar set at a high rpm.
2. Leave the wafer in ACE for at least 10 min.
3. Squirt rinse in METH followed by ISO.
4. Rinse in DI for 3 min.
5. Blow dry with N_2.
6. Dektak small and large areas to verify whether etching has stopped uniformly on the InGaAs cap layer.

E.2 Self Aligned Ohmics

Mask Layer: Ohmics, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.

5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 60 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 8 s.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Recess Etch to N++ Layers**
Safety Note: Wear Silver Shield gloves or equivalent when handling

bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant atleast 15 min. before the etching.
2. Etchant composition is $H_3PO_4 : H_2O_2 : H_2O :: 3 : 1 : 4$.
3. Use magnetic stirrer bar at 300 -400 rpm to agitate solution.
4. Mix 15 ml of H_3PO_4 to 250 ml of water and stir well. Add 5 ml of H_2O_2 to the etchant and stir well.
5. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$ in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Etch in $H_3PO_4 : H_2O_2 : H_2O$ solution for 20 to 30 sec.
   Etch rate is $\approx$1000 Å/min.
10. Rinse in running DI for 3 min.
11. Blow dry with N_2.
12. Use Dektak to determine etch depth and rate.
13. Continue etching in steps of 30 sec to get to the N++ layers of both the SRTD and the Schottky-diode. A slight overetch of the SRTD ohmics is required for this purpose.

G **Metal Evaporation**

1. Load sample into E-beam evaporator immediately after the etch.
2. Place wafer in E-Beam mount.
3. Make sure the crystal monitor reads < 10; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/s.)	Approx. Vernier
Ge	108	2-3	1.75
Au	102	2-3	1.45
Ge	63	2-3	1.75
Au	236	2-3	1.45
Ni	100	1-2	1.75
Au	1400	$\approx$5	1.55

Note: If the thickness have not been quite right for the first 3 layers, adjust the thickness of the 4^{th} layer (Au) to get the correct

stochiometric ratio of Ge:Au=1:1.977 for the first 4 layers.

H **Liftoff**
Important Note: DO NOT LET ACETONE DRY ON WAFER.

1. Suspend wafer with a teflon basket or 2-inch wafer holder in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse with METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

I **Rapid Thermal Annealing**

1. Prepare RTA by loading the program for 360° C, 10 sec anneal. Also make sure forming gas is flowing at prescribed the rate and pressure.
2. Run the program several times until the temperature stabilizes at 360° C, during the 10 sec period.
3. Load the wafer on Si wafer holder and run the program.
   Caution: After anneal and trial runs, turn off the forming gas and use a face mask before opening the chamber.
4. Rinse wafer in DI for 2 min.
5. Inspect under microscope. You should be able to see the change in surface morphology.
6. Measure TLM pattern, should get $R_C \approx 12\Omega - \mu$m and $R_{SH} \approx 1 - 2\Omega/\Box$.
7. If you don't get typical values $\pm 50\%$, consider changing the program.

E.3 Airbridge Submicron Schottky-Collector

Ebeam lithography at JPL

A **Solvent Cleaning**

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **E-beam Trilayer Resist Application**

1. Inspect the ohmics to determine whether adjustments are necessary to account for roughness or variation from designed dimensions.
2. Surface clean in HCl : DI :: 1:100 for 30 sec.
3. Blow dry with N_2 for 30 sec.
4. Spin coat first layer of PMMA (496K, 2.5% solids in cholorbenzene). A premixed 4% solution is thinned using a premixed 1% solution to arrive at the 2.5% solution.
5. A dynamic dispense speed of 500 rpm, followed by sond spread speed of 1200 rpm for 2 s followed by a final spin speed of 4000 rpm for 30 sec.
6. Bake on hot plate at 115° C for 60 sec.
7. Cure on hot plate at 170° C for 15 min.
8. Cool down the sample for 10 min.

9. Spin coat the sond layer consisting of PMMA methacrylic acid coploymer (PMMA/MAA, 9%) using the same spin, bake and cure conditions as the first layer (Steps 5 to 8).
10. Spin coat a final layer of PMMA (premixed, 950K, 2%) using the same spin, bake and cure conditions as the first layer (Steps 5 to 8).

C **E-beam Exposure**

E-beam system: A JEOL JBX 5DII running at 50 KV using aperture 2 in the 5th lens with a beam current of 200 pA. The pattern is written as rectangles rather than lines and uses a step size of 10.

1. High dose of ≈290 μC/cm^2 for defining the Schottky-collector foot print.
2. Lighter dose of ≈70-80 μC/cm^2 to define the T- structure and the air bridge.
3. Moderate dose of ≈90 μC/cm^2 to define the contact area to the ohmic-metal pad.

D **Development**

1. Sample dipped in Chlorobenzene for 15-17 s with the anodes oriented horizontally.
2. Toluene rinse for 5 sec followed by Toluene spray for 10 sec.
3. Steps 1 and 2 develop the top layer of PMMA.
4. Sample immersed for 2 min. in a 1:1 mixture of Isopropyl alcohol (IPA) and methanol agitated by a magnetic stirrer bar rotating at ≈100 rpm. This step dissolves the exposed copolymer layer and also undercuts the top layer of PMMA slightly.
5. Sample immersed for 2 min. in a 1:1 mixture of methyl isobutyl ketone (MIBK) and IPA agitated by a magnetic stirrer bar. This step dissolves the exposed regions of bottom layer of PMMA.
6. Rinse in IPA followed by a blow dry with N_2.
7. SEM inspection at an accelerating voltage of 2 KV. An addtional MIBK:IPA develop is done if development is incomplete.

E **Oxygen Plasma Photoresist Descum**

1. 500 mTorr of O_2.

2. Power = 50W at low frequency.
3. Run for 30 sec.

F **Surface Preparation**

1. 10 sec dip in IPA : DI :: 1 : 10 to improve surface wetting.
2. 20 sec dip in NH_4OH : H_2O :: 1 : 30.
3. Rinse in DI for 30 sec.
4. 30 sec dip in buffered oxide etch (BOE) to remove surface oxides.
5. Rinse in DI for 30 sec.
6. 15-20 sec etch in H_2O_2 : Citric Acid : DI :: 1 : 11 : 44.
7. Rinse in DI for 30 sec.
8. 20 sec dip in NH_4OH : H_2O :: 1 : 30.
9. Blow dry with N_2.

G **Metallization**
Important Note: LOAD EVAPORATOR IMMEDIATELY AFTER SURFACE PREPARATION.

1. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/s.)
Ti	300	1-2
Pt	300	1-2
Au	3000	3-7

H **Liftoff**
Important Note: DO NOT LET ACE DRY ON WAFER

1. Immerse in a beaker of ACE sitting in a hot bath at 60° C.
2. Rinse in METH.
3. Rinse in running DI water.
4. Blow dry with N_2.

E.4 Mesa Isolation

Mask Layer: Mesa, Light Field

A **Solvent Cleaning**

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

C **Solvent Cleaning**

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

D **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful.

Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply AZ P4210 with syringe and filter to cover wafer.
4. Spin at 5.5 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

E **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 12 sec.
4. Use hard-contact (HP mode) and use O-ring.

F **Development**

1. Toluene soak: 4 min.
2. Mix fresh developer, AZ 400K : DI :: 1:4.
3. Develop for 90 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist is remaining, develop again in steps of 5 sec.

G **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

H **Hard Bake**

1. Hard bake in oven at 120° C for 30 min. in petri dish without cover.
2. This step hardens the resist and rounds off the edges of the photoresist.

I **Isolation Etch**

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix fresh etchant in a large beaker at least 15 min. before etching.
2. Etchant composition is citric acid : H_2O_2 : H_2O : H_3PO_4 :: 11 : 1 : 44 : 0.2.
3. Use magnetic stirrer bar at 300-400 rpm to agitate solution throughout this step.
4. Mix 132 ml of 1M of citric acid to 528 ml of water. Add 12 ml of fresh H_2O_2 using a small beaker and pippette. Add 2.4 ml of H_3PO_4 to the etchant.
5. Mix a dilute slution of NH_4OH : H_2O :: 1 : 10 in another beaker.
6. Dektak wafer, measure photoresist thickness.
7. Dip in dilute NH_4OH for 20 sec.
8. Rinse in DI for 3 min.
9. Etch in citric acid etchant solution for 2 min. Etch rate is $\approx$ 450$\mathring{A}$/min.
10. Rinse in running DI for 3 min.
11. Blow dry with N_2.
12. Use Dektak to determine etch depth and rate.
13. Continue etching till the semi-insulating InP layer is reached. This is observed by a color change of the wafer and the diasppearance of the MBE ring at the edges of the wafer.
14. Probe a few SRTDs and measure DC charactersitics to verify whether the isolation has been achieved between the active and passive mesas.
15. Overetching is almost always required to etch away the semiconductor beneath the airbridge submicron Schottky collector. The usual overetch time is $\approx$10-15 mins.
16. Repeat the etching and DC probing till the devices show isolation between active and passive mesas. Isolation etch is complete when the DC probing indicates that there is no current flow near about zero volt. At this point, the complete sweep of DC characteristics will show NDR region of the SRTDs.

17. SEM inspection to observe whether all the material has been etched between the active and passive mesas of all SRTDs across wafer.

J **Photoresist Stripping**
Important Note: DO NOT LET ACETONE DRY ON WAFER

1. Immerse wafer in a beaker of ACE with magnetic stirrer bar set at a high rpm.
2. Leave the wafer in ACE for at least 10 min.
3. Squirt rinse in METH followed by ISO.
4. Rinse in DI for 3 min.
5. Blow dry with N_2.
6. Examine under microscope. If any photoresit scum is visible go to the next step, other wise the isolation step is complete.
7. Immerse wafer in hot 1165 (photoresist stripper) at 100 ° C for 3-5 min.
8. Soak wafer in ISO for 5 min.
9. Rinse in DI for 3 min.
10. Blow dry with N_2.

E.5 Interconnect Metal

Mask Layer: Interconnect, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.

3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply OCG825 with syringe and filter to cover wafer.
4. Spin at 5 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.
6. Cool down after soft bake for 5 min.
7. Flood expose at 7.5 mW/cm^2 for 3 sec.
8. Toluene soak for 3 min.
9. Blow dry with N_2.
10. Apply OCG825 with syringe and filter to cover wafer.
11. Spin at 5 krpm for 30 sec.
12. Soft bake in oven at 90° C for 30 min. in petri dish without cover.
13. Cool down after soft bake for 5min.
14. Flood expose at 7.5 mW/cm^2 for 2 sec.
15. Toluene soak for 2 min.
16. Blow dry with N_2.
17. Apply AZ P4210 with syringe and filter to cover wafer.
18. Spin at 5.5 krpm for 30 sec.
19. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake, 10 min.
2. Edge bead removal necessary if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 12 sec.

4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Mix fresh developer, AZ 400K : DI :: 1:4.
2. Develop for 180 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.
6. Total photresist thickness is ≈ 4.0 μm.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Metal Evaporation**

1. Surface preparation by dipping in dilute NH_4OH:H_2O (1:10) for 20 sec.
2. Load the sample into E-beam evaporator immediately.
3. Place wafer in E-Beam mount.
4. Make sure the crystal monitor reads < 10; change if necessary.
5. Do not lower the boom.
6. Pump down to at least $7\times$ 10^{-7} Torr.
7. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.70
Au	15000	$\approx$ 20-25	1.55

G **Liftoff**
Important Note: DO NOT LET ACETONE DRY ON WAFER

1. Suspend wafer in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff

3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse in METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.
8. SEM inspection to verify whether the step coverage of metal over the mesa eges has been achieved.

E.6 Silicon Nitride

Mask Layer: Silicon Nitride, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.
2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Silicon Nitride Deposition**

1. Clean the PECVD chamber and deposit SiN on the chamber walls using the program 30CLNSIN.
2. Load the PECVD with a dummy GaAs wafer. Run the program SIN10 to deposit 1000 Å of SiN. The surface of the wafer should be roughly light blue in color.
3. Use ellipsometer to measure film thickness ($\approx$ 1000 Å) and index $\approx$ 2.0.
4. Repeat the deposition procedure on the real wafer if the desired thickness and refractive index are obtained on the dummy wafer.

C **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. HMDS vapors are very harmful and the HMDS bottle should always be covered. Never breathe if you put your head under the hood.

1. Cool down after PECVD deposition for 10 min.
2. Expose wafer to HMDS vapors for 10 min. by placing a big beaker over the wafer and the HMDS bottle.
3. Wafer on spinner chuck with vacuum. Blow with N_2.
4. Apply AZ P4210 with syringe and filter to cover wafer.
5. Spin at 6 krpm for 30 sec.
6. Soft Bake in oven at 90° C for 30 min. in petri dish without cover.

D **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 12 sec.
4. Use hard-contact (HP mode) and use O-ring.

E **Development**

1. AZ 400K : DI :: 1:4
2. Develop for 90 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.

5. If some photoresist remains develop again in steps of 5 sec.

F **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 25 sec.

G **Hard Bake**

1. Hard bake in oven at 120° C for 30 min. in petri dish without cover.
2. This step hardens the resist and rounds off the edges of the photoresist.

H **SiN Dry Etch**

1. Clean the RIE chamber by O_2 plasma etch at 25 sccm, 50 mTorr and 500 W RF power for 15 min. prior to etching.
2. Load a dummy wafer that has the same thickness of SiN as the real wafer.
3. Adjust the set points for the the flow of the gases as follows. SF_6 : Argon : O_2 : : 5 sccm : 10 sccm : 3 sccm. Adjust the pressure to 20 mTorr in the RIE chamber. Adjust the laser beam and detector set up to monitor the etch.
4. Switch on RF supply voltage in constant voltage mode and adjust voltage to 250 V. The corresponding RF power is $\approx$ 30 W.
5. Monitor the standing wave patterns till all the SiN has been etched. Total etch time is roughly 90 sec. Over etch by 15 sec and stop the etching process.
6. Evacuate the chamber of the gases and pump down for atleast 5 min. before opening the chamber.
7. Check visually whether all the SiN on the dummy wafer has been removed and whether the surface looks clean.
8. Repeat the etching process on real wafer with the laser monitoring the etch on another dummy wafer that has exactly the same thickness of the SiN.

I **Plasma Descum**

1. Plasma descum in CF_4 plasma at 300 mTorr/100 W for 5 sec.
2. Plasma descum in O_2 plasma at 300 mTorr/100 W for 20 sec.

J **Surface Clean**

1. Dip in $NH_4OH : H_2O_2$ (1 : 10) for 20 sec.
2. DI rinse for 3 min.
3. Blow dry with N_2.

K **Photoresist Stripping**
Important Note: DO NOT LET ACE DRY ON WAFER

1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes $\approx$ 2-5 min.).
2. Squirt ACE on wafer with squirt bottle.
3. Squirt rinse in METH followed by ISO.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. Examine under microscope to check whether all features have opened up and are clear of SiN.

E.7 Posts

Mask Layer: Posts, Dark Field

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. HOT TCA 5 min.

2. Cold ACE 5 min.
3. Hot ISO 5 min.
4. Running DI 3 min.
5. Blow dry with N_2.
6. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.
3. Apply SF11 with syringe and filter to cover wafer.
4. Spin at 4 krpm for 30 sec.
5. Bake on hot plate at 200° C for 5 min.
6. Cool down after hot plate bake for 5 min.
7. Wafer on spinner chuck with vacuum. Blow with N_2.
8. Apply SF11 with syringe and filter to cover wafer.
9. Spin at 4 krpm for 30 sec.
10. Bake on hot plate at 200° C for 5 min.
11. Cool down after hot plate bake for 5 min.
12. SF11 edge bead removal necessary at this point if the wafer is not a 2-inch wafer. After edge bead removal, dehydration bake in oven at 120° C for 30 min. in petri dish without cover.
13. Wafer on spinner chuck with vacuum. Blow with N_2.
14. Apply AZ P4210 with syringe and filter to cover wafer.
15. Spin at 5.5 krpm for 30 sec.
16. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary, if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 12 sec.

4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Mix fresh developer, AZ 400K : DI :: 1:4.
2. Develop for 90 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist is remaining, develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **DUV Exposure**

1. Deep UV flood expose at 10.0 mW/cm^2 for 300 sec with rotation.

G **Development**

1. Develop in SAL developer for 120 sec.
2. Rinse in running DI water for 3 min.
3. Blow dry with N_2.
4. Repeat DUV flood expose for 10 sec.
5. Develop in SAL developer for 30 sec.
6. Blow dry with N_2.
7. If SF11 is still remaining, repeat flood expose (10 sec) and SAL develop (30s) till all SF11 is removed in the posts.

H **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

I **AZ P4210 Photoresist Removal**
Important Note: DO NOT LET ACE DRY ON WAFER

1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes ≈ 1-2 min.).
2. Squirt ACE on wafer with squirt bottle.
3. Squirt rinse in METH followed by ISO.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. Examine under microscope to check whether posts are clear of photoresist.
7. Dehydration bake at 120° C, 30 min. in petri dish without cover.

J **Reflow of SF11**

1. Hot plate bake at 200° C for 10 min. to reflow SF11.
2. Cool down after hot plate bake, 10 min.
3. Examine under a microscope to verify whether the edges of the posts are rounded.

E.8 Airbridges

Mask Layer: Airbridge, Dark Field

A **Solvent Cleaning**
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Squirt with ACE, METH and ISO.
2. Running DI 3 min.
3. Blow dry with N_2.
4. Dehydration bake in oven at 120° C for 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration for 10 min.
2. Wafer on spinner chuck with vacuum. Blow with N_2.

3. Apply OCG825 with syringe and filter to cover wafer.
4. Spin at 5 krpm for 30 sec.
5. Soft bake in oven at 90° C for 30 min. in petri dish without cover.
6. Cool down after soft bake for 5min.
7. Flood expose at 7.5 mW/cm^2 for 3 sec.
8. Toluene soak for 3 min.
9. Blow dry with N_2.
10. Wafer on spinner chuck with vacuum. Blow with N_2.
11. Apply OCG825 with syringe and filter to cover wafer.
12. Spin at 5 krpm for 30 sec.
13. Soft bake in oven at 90° C for 30 min. in petri dish without cover.
14. Cool down after soft bake for 5min.
15. Flood expose at 7.5 mW/cm^2 for 3 sec.
16. Toluene soak for 3 min.
17. Blow dry with N_2. item Wafer on spinner chuck with vacuum. Blow with N_2.
18. Apply OCG825 with syringe and filter to cover wafer.
19. Spin at 5 krpm for 30 sec.
20. Soft bake in oven at 90° C for 30 min. in petri dish without cover.
21. Cool down after soft bake for 5min.
22. Flood expose at 7.5 mW/cm^2 for 2 sec.
23. Toluene soak for 2 min.
24. Blow dry with N_2. item Wafer on spinner chuck with vacuum. Blow with N_2.
25. Apply AZ P4210 with syringe and filter to cover wafer.
26. Spin at 5.5 krpm for 30 sec.
27. Soft bake in oven at 90° C for 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake for 10 min.
2. Edge bead removal necessary if the sample is not a 2-inch wafer.
3. Expose at 7.5 mW/cm^2 for 25 sec.
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Mix fresh developer, AZ 400K : DI :: 1:4.
2. Develop for 150 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.
6. Total photoresist thickness is ≈5.0 μm.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Metal Evaporation**

1. Surface preparation by dipping in dilute NH_4OH:H_2O (1:10) for 20 sec.
2. Load the sample into E-beam evaporator immediately.
3. Place wafer in E-Beam mount.
4. Make sure the crystal monitor reads < 10; change if necessary.
5. Lower the boom to get ≈3.0 times the evaporation rate.
6. Pump down to at least 7×10^{-7} Torr.
7. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	65	2-3	1.70
Pt	165	1-2	1.95
Au	10000	≈ 20-25	1.55

G **Liftoff**
Important Note: DO NOT LET ACETONE DRY ON WAFER

1. Suspend wafer in a beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.).
2. Squirt with ACE from a squirt bottle to help liftoff.

3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Squirt rinse in METH followed by ISO.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

H **SF11 Removal**

1. Suspend wafer in a beaker of hot 1165 at 100° C with magnetic stirrer bar at setting of 3-4 for 10 min.
2. Soak wafer in ISO for 5 min.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If SF11 is remaining beneath the airbridge metal, repeat steps 1 to 4 till all SF11 on the wafer is removed.

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