160 GHz Balanced Frequency Quadruplers Based on Quasi-Vertical Schottky Varactors Integrated on Micromachined Silicon

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***Abstract*—This work reports on an integrated frequency quadrupler operating at 160 GHz with maximum efficiency of 30% and corresponding output power of 70 mW. The quadrupler design includes two frequency doubler stages in cascade and is based on a balanced circuit architecture that addresses degradation issues often arising from impedance mismatches between multiplier stages. A unique quasi-vertical diode fabrication process consisting of transfer of GaAs epitaxy to a thin silicon support substrate is used to implement the quadrupler, resulting in an integrated drop-in chip module that incorporates 18 varactors, matching networks and beamleads for mounting. The chip is tailored to fit the multiplier waveguide housing, resulting in high reproducibility and consistency in manufacture and performance. Estimates of the varactor temperature for the multiplier were made using the diodes as integrated thermometers. These measurements estimate the operating temperature of the varactors in the quadrupler input stage to be 35 °C.**

***Index Terms*—Epitaxial transfer, frequency multiplier, Schottky diode, silicon integration, submillimeter-wave, varactor, waveguide.**

I. Introduction

FREQUENCY multipliers based on Schottky barrier diodes represent the most commonly-used solid-state device technology for generating power at frequencies ranging from 100 GHz to 1 THz. Over the years, these devices have remained critical to a variety of submillimeter-wave heterodyne-based instruments [1], including radiometers for space-borne applications, receivers for ground-based radio astronomy, and sources for vector network analyzer frequency extenders [2]. The design of varactor multipliers is a well-established topic and the fundamental issues have been understood since the work of Penfield and Rafuse [3]. From this foundation, a number of preferred multiplier circuit topologies have emerged—notably, the balanced doubler [4], [5] and tripler [6]–[9] configurations that employ anti-parallel or anti-series connected diodes. These circuit configurations have become commonplace due to their inherent isolation of even- and odd-order harmonics, eliminating the need for filters.

Generation of power at frequencies approaching 1 THz typically requires many stages of multiplication as the fundamental input signal is often in the microwave range where significant (watt-level) drive power is achievable. Direct multiplication to a high-order harmonic greater than the third is usually not considered practical as proper termination of all intermediate harmonics (idlers) is a complex (and sometimes intractable) design problem. Multipliers based on the heterostructure barrier varactor, a device that has the necessary intrinsic symmetry to generate only odd-order harmonics, is a notable exception and can be used to implement a direct quintupler by employing a single idler [10]. Nevertheless, submillimeter-wave multiplier sources typically consist of a chain of doublers and triplers, selected to yield the desired output frequency. Cascading multipliers is a pragmatic approach, with output powers of hundreds of milliwatts being obtained in the millimeter-wave band with this technique. Although the efficiencies for varactor doublers can be 50% or more [5], doublers and triplers are typically operated for maximum power output and are consequently less efficient [11]. The overall efficiency of a large multi-stage chain, as a result, is often on the order of a few percent or less [12]. Moreover, mismatches between adjacent multipliers in a cascade can readily disturb earlier multiplier stages by pulling them from their optimum operating point, further reducing efficiencies and output power. As a result, intermediate matching or isolation networks are frequently inserted between adjacent stages, contributing to loss and system complexity. In addition, the input stages of large multiplier chains must be capable of handling high power (several watts) to overcome the low efficiencies and produce usable output power, which is often significantly below 1 mW at frequencies above 1 THz.

This paper presents a frequency multiplier architecture that is intended to address a number of the issues noted above that are frequently encountered in cascaded multipliers. The circuit topology consists of a pair of balanced frequency doublers that are driven in phase quadrature using a hybrid coupler. This approach results, effectively, in a "unilateral" multiplier that presents a match to the input driving source, irrespective of the impedance of the doubler stages. The work presented

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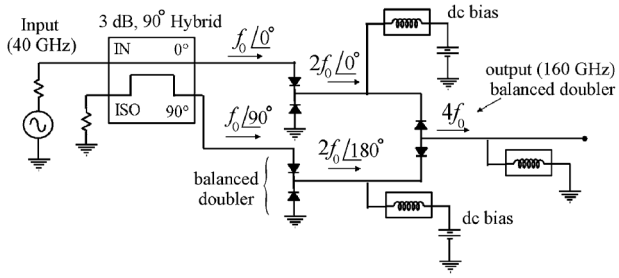

Fig. 1. Diagram of the quadrupler circuit architecture.

here applies this architecture to implement an integrated frequency quadrupler with output frequency of 160 GHz using quasi-vertical GaAs varactors fabricated on thin silicon support membranes.

II. Quadrupler Architecture and Design

Fig. 1 illustrates the basic architecture of the quadrupler circuit developed in this work. The input stage of the multiplier consists of a pair of balanced doublers that are driven through a quadrature hybrid, resulting in two outputs at twice the fundamental input frequency (f_0) and out-of-phase. This circuit topology is often employed for balanced amplifiers and phase-shifters, as any fundamental frequency power reflected from the inputs of the doublers (provided they are identical) is directed to the isolation port, which serves as power "dump." Consequently, the input source (which may be another multiplier stage in a cascade) is presented with a match over the bandwidth of the hybrid and is not subject to variations in loading and performance due to changes in the operating conditions of the balanced doublers that it drives. The intermediate outputs at $2f_0$ have the proper phasing to drive a second-stage balanced doubler that bridges the outputs of the two input-stage doublers, thus yielding a frequency quadrupler.

The use of a balanced circuit architecture to realize "unilateral" multipliers that are insensitive to the loading effects of the output stages appears to have been first proposed by Gewartowski in 1964 [13] who later applied this approach to realize a quadrupler with 2.5 W of output power at 6 GHz [14]. The quadrupler presented here makes use of the same basic approach, but differs from that of Gewartowski as it uses a second-stage balanced doubler to generate the fourth harmonic.

Design of the quadrupler circuit consists essentially of two steps—1) determining the proper embedding impedances to present to the varactors of the input balanced doubler driven at the fundamental input frequency of f_0 (40 GHz) and 2) similarly, determining the impedances to present to the diodes of the output doubler stage driven at a frequency of $2f_0$ (80 GHz). Fig. 2 illustrates the three networks comprising the design: 1) a stepped impedance input matching circuit implemented in (WR-22) waveguide; 2) an intermediate matching/filtering network designed to present the proper load impedance to the input doubler and source impedance to the output doubler at $2f_0$; and 3) a matching circuit that couples the output at $4f_0$ to a waveguide probe in the WR-5.1 band.

The input stage of the quadrupler consists of a pair of identical balanced frequency doublers, driven by the TE_{10} mode of

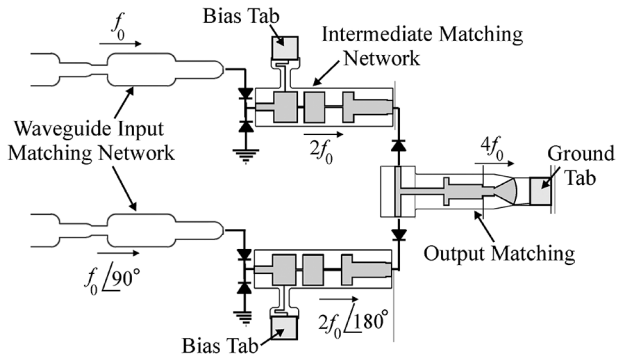

Fig. 2. Geometry of the quadrupler matching and filtering networks.

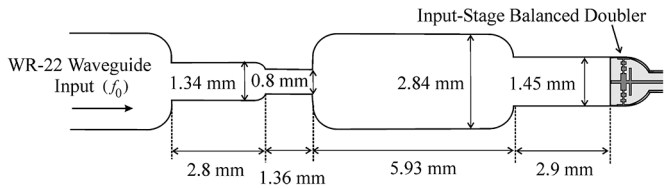

Fig. 3. Input waveguide network to first-stage frequency doubler.

an input WR-22 (33–50 GHz) waveguide. Design of the doubler is based on the method of Porterfield [5] where an array of anti-series oriented varactors extends across a reduced-height waveguide to suppress excitation of the undesired TM_{11} mode, which has a field distribution that can couple to the opposing currents generated by the diodes at the second harmonic. Fig. 3 shows the details of the waveguide stepped-impedance network and Fig. 4(a) is a rendering of the top-half of the geometrically symmetric input stage, detailing the transition from reduced-height waveguide to the diode array and suspended stripline output circuit. The input frequency and available power determine the varactor anode size, substrate doping, epilayer thickness, and number of diodes required for the doubler [5], as these parameters directly impact the diode series resistance, breakdown voltage, and onset of velocity saturation [15]. Based on the 350 mW WR-22 source readily available in our laboratory, the GaAs epitaxy was selected to have an epitaxial modulation (n) layer 200 nm thick with doping concentration of 2×10^{17} cm^{-3} and a 1 μm thick highly doped $(5 \times 10^{18}$ cm$^{-3})$ $n+$ buffer layer. With an anode diameter of 9.6 μm, these parameters are expected to yield diodes with zero-bias junction capacitance of 107 fF, reverse breakdown of approximately 9.5 V, and velocity saturation current of 460 mA [5], [15]. Current-voltage measurements of test diodes fabricated with the quadrupler circuit yielded a series resistance for these devices of 0.4 Ω.

As the design objective was to maximize quadrupler efficiency, a harmonic balance analysis using Agilent's *Advanced Design System (ADS)* was performed with the varactors described above to determine the optimum embedding impedances to present to the diodes in the input-stage doubler. These impedances were found to be $10 + j70$ (Ω) for the source impedance at 40 GHz and $20 + j35$ (Ω) for the output load at 80 GHz. The stepped-impedance waveguide transformer of Fig. 3 was designed to present this impedance to each diode of the six-element diode array at 40 GHz. Fig. 4(a) shows the

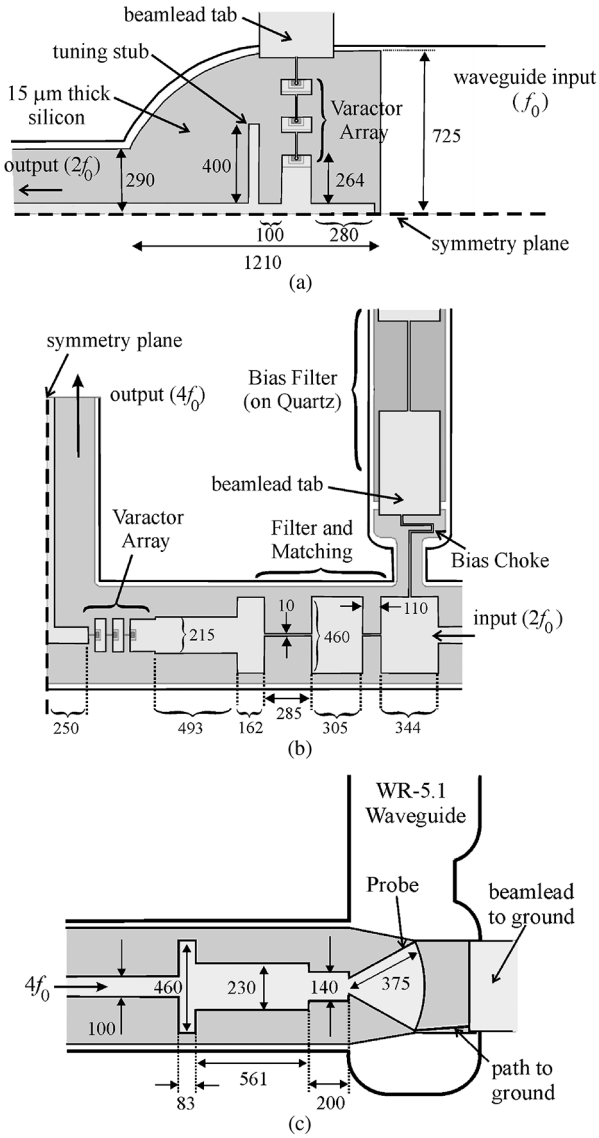

Fig. 4. Layout of the three primary sections of the quadrupler: (a) input doubler circuit; (b) output doubler circuit with intermediate matching stage; and (c) output matching circuit and transition to WR-5.1 waveguide. All dimensions noted have units of μm.

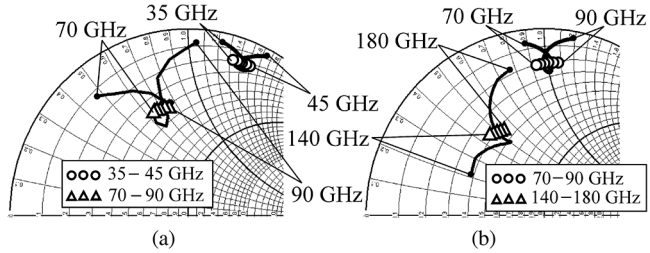

Fig. 5. Input and output impedance of: (a) input-stage doubler and (b) output-stage doubler. The symbols represent the optimum impedances found from harmonic balance and the solid lines the impedances presented by the matching networks of Fig. 4.

circuit features of the first-stage doubler geometry which transitions from reduced-height waveguide to suspended stripline. The symmetry plane is represented as an electric wall for the input fundamental signal, which is essentially unaffected by the stripline circuit to the left of the diode array as it lies along a perfectly-conducting boundary. The impedance presented to a diode by the circuit was determined using Ansoft's *High-Frequency Structure Simulator (HFSS)* to analyze the structure of Fig. 4(a).

For the output second harmonic, a magnetic wall boundary condition is imposed on the symmetry plane and the output circuit designed accordingly to present an impedance of $20 + j35\ (\Omega)$ to each diode in the array at 80 GHz. This matching circuit consists of a 74 Ω transmission line section and shunt stub of length 400 μm placed 100 μm from the diode array, as seen in Fig. 4(a). Fig. 5(a) shows the impedances presented to the diodes by the input and output stage circuits of Fig. 4(a), as well as the optimum impedances found from harmonic balance.

The geometry of the intermediate section of the multiplier, extending from the output of the first-stage doubler to the input of the second-stage doubler, is shown in Fig. 4(b). This section includes a lowpass filter for the 80 GHz output of the first-stage doubler followed by a stepped-impedance transformer that presents $10 + j50\ (\Omega)$ to the diodes at the input of the second-stage doubler. Because the outputs of the two first-stage doublers are out-of-phase, the symmetry plane of Fig. 4(b) is an electric boundary for the input at 80 GHz. This virtual electric boundary extends along the quadrupler output circuit, effectively removing its influence on the input signal at $2f_0$ (80 GHz).

As with the input doubler stage, optimum impedances for the diodes of the output doubler stage ($10 + j50\ (\Omega)$ at 80 GHz and $20 + j25\ (\Omega)$ at 160 GHz) are found using harmonic balance analysis. The varactor diodes for the output stage make use of the same epitaxy as the input doubler, but the anode diameter is scaled to 8 μm to provide a zero-bias junction capacitance of 75 fF. Fig. 5(b) shows the impedances presented to a diode in the second-stage doubler found from harmonic balance and *HFSS* simulations of the structure in Fig. 4(b).

The final step of the quadrupler design consists of transforming the output impedance of the second-stage doubler to the TE_{10} mode impedance of the output waveguide, thus maximizing power coupled to the output WR-5.1 waveguide at 160 GHz. The output matching network (Fig. 4(c)) consists of a simple shunt stub and stepped-impedance stripline section that transforms the waveguide probe impedance to $20 + j25\ (\Omega)$ for the diodes of the doubler array. A thin line (of width 6 μm) connecting the edge of the waveguide probe to the beamlead tab provides ground for the diodes of the second-stage doubler

Final design and optimization of the quadrupler is accomplished with a modular approach where the circuit is partitioned into its primary sections, as described above, and each analyzed using *HFSS*. Scattering parameters obtained for the matching networks from *HFSS* are imported into *ADS* to perform harmonic balance analysis and determine the resulting multiplier performance. This process is iterated, adjusting the geometry of the circuit each time, to bring the impedances presented to the varactors close to their optimum values.

Fig. 6 shows the final geometry of the quadrupler chip resulting from this design process. The chip is a single drop-in unit, approximately 7.5 mm in length, made of 15 μm thick high-resistivity ($>10\ \mathrm{k}\Omega \cdot \mathrm{cm}$) silicon that incorporates three

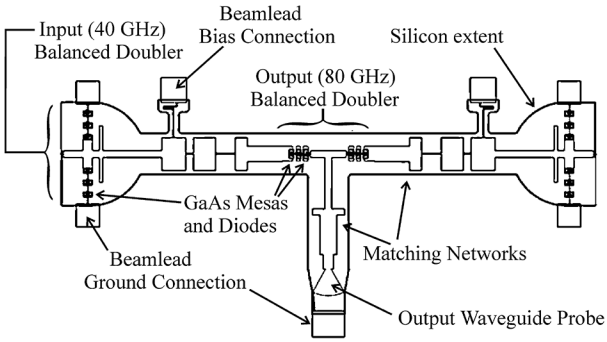

Fig. 6. Layout of the full integrated quadrupler chip. The overall length of the chip is ∼7.5 mm.

sets of balanced doublers (totaling 18 varactor diodes) with associated matching networks, and includes gold beamlead tabs extending from the chip perimeter to accommodate alignment, mounting and bias connections.

III. Fabrication and Assembly

Fabrication of the multiplier chip shown in Fig. 6 is based on a quasi-vertical diode process developed at the University of Virginia (Charlottesville, VA, USA) and described in [16], [17]. A key step of the process is transfer of the GaAs epitaxy to a silicon-on-insulator (SOI) substrate that serves as the final carrier chip for the diodes and their associated circuitry. After initial formation of the device ohmic contacts, the diode epitaxy is bonded, ohmic contact-side-down, to the SOI substrate. Following this step, most of the GaAs is etched from the wafer, leaving only mesas for fabrication of the diodes. The remaining features of the diodes and multiplier circuits (anode, contact finger and cathode metallization) are fabricated using standard lithographic, metal deposition, and etching processes as described in [17]. Fig. 7(a) is a scanning electron micrograph (SEM) showing the geometry of one of the quasi-vertical diode arrays of the quadrupler circuit. A view of an integrated multiplier circuit before the final etch that separates individual chips is seen in Fig. 7(b).

Following the diode processing steps, the wafer is bonded topside-down to a temporary carrier wafer, revealing the backside silicon handle of the SOI. This "handle" silicon is removed through reactive ion etching to the buried oxide layer, which acts as an etch stop. Buffered hydrofluoric (HF) acid is used to etch the oxide, leaving the multiplier circuits on a thin (15 μm), high-resistivity silicon membrane bonded to the carrier. A backside reactive-ion "extents" etch is used to separate the multiplier chips and define their geometry. The final step in the process is removal of the temporary carrier wafer, releasing the individual chips. Fig. 8 shows a portion of a completed multiplier chip, including the input-stage doubler diode array, integrated beamlead tabs, and the 15 μm silicon membrane.

The housing for the quadrupler circuit is fabricated as an E-plane split-block assembly from gold-plated aluminum using standard milling methods. As shown in Fig. 9, the housing includes a WR-22 3-dB stepped branchline coupler [18] to provide in-phase and quadrature inputs to the quadrupler chip, WR-22 and WR-5.1 waveguide sections, and channels to

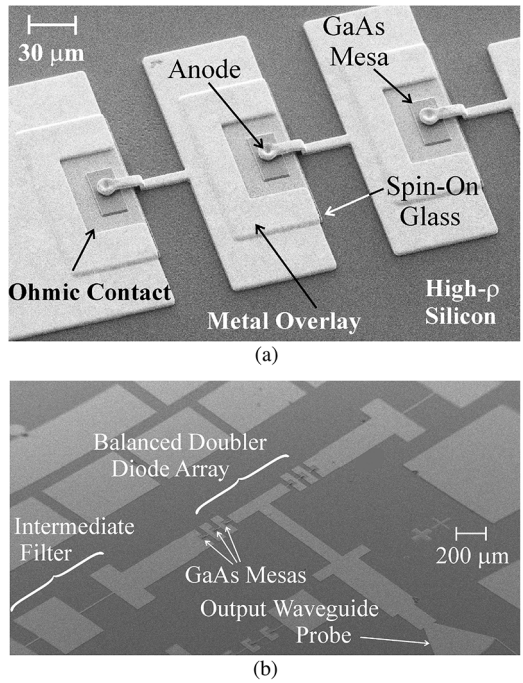

Fig. 7. (a) Scanning electron micrograph of quasi-vertical diodes comprising the output doubler array. The ohmic contact lies directly below the anode and GaAs mesa and is bonded to a high-resistivity silicon substrate. (b) Image of the completed quadrupler circuits prior to the backside extents etch and chip separation. The image shows the region near the output-stage doubler.

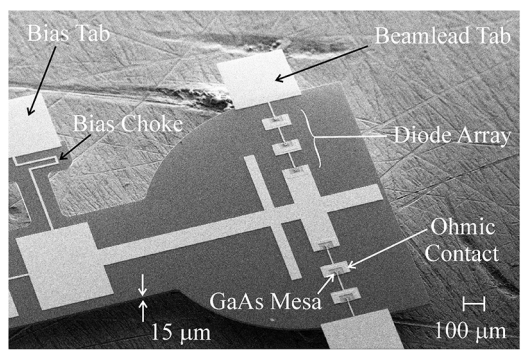

Fig. 8. SEM of the input doubler diode array and beamlead portion of the chip.

accommodate quartz-supported filters for bias connections. External bias is supplied to the chip through low-profile GPPO connectors. The WR-22 input and isolation ports of the multiplier are designed to mate with standard UG-383 flanged waveguide and the output (WR-5.1) is a UG-387 interface.

Fig. 10 shows a photograph of the quadrupler chip mounted to the housing. Beamlead tabs protruding from the chip at the two input-stage doublers and WR-5.1 output probe provide grounding and support for the circuit as it is clamped in the split-block seam of the housing during assembly. Two additional beamleads protrude from hairpin bias chokes and are bonded to quartz-supported filters to provide dc bias to the diode arrays.

IV. RF Measurements

Characterization of the quadrupler is done using the experimental setup shown in Fig. 11. The input signal is supplied by

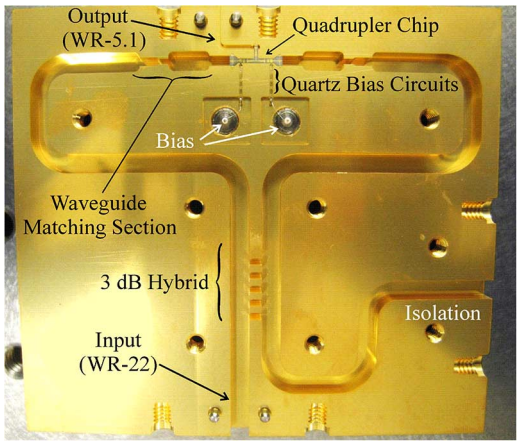

Fig. 9. Photograph of the quadrupler housing assembly showing the mounted chip and waveguide design features.

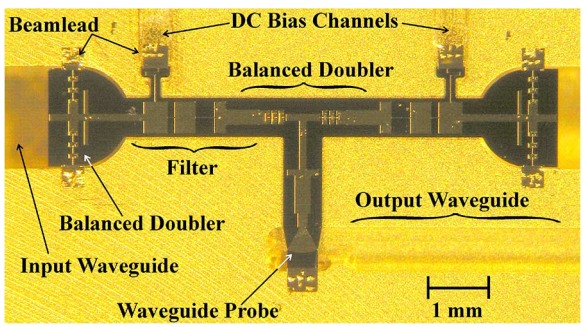

Fig. 10. Image of the quadrupler chip mounted to the waveguide housing.

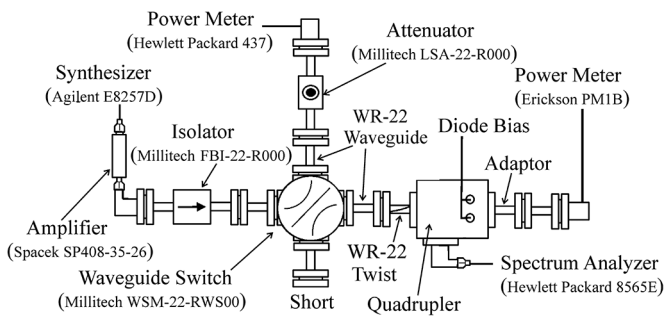

Fig. 11. Diagram of the quadrupler measurement setup.

an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain, 36 to 43 GHz bandwidth and output power of 26 dBm at the 1 dB compression point. A WR-22 waveguide switch is used to monitor the available power as well as direct the input signal to the multiplier block. An Erickson PM1B power meter is used to measure the multiplier output power in the WR-5.1 band and a spectrum analyzer placed at the quadrupler isolation port monitors power scattered from the input-stage doublers, permitting the return loss of these doublers to be measured during operation. Measurement of the quadrupler was done at the University of Virginia and repeated at Virginia Diodes, Inc., Charlottesville, VA, USA, to ensure consistent results were obtained.

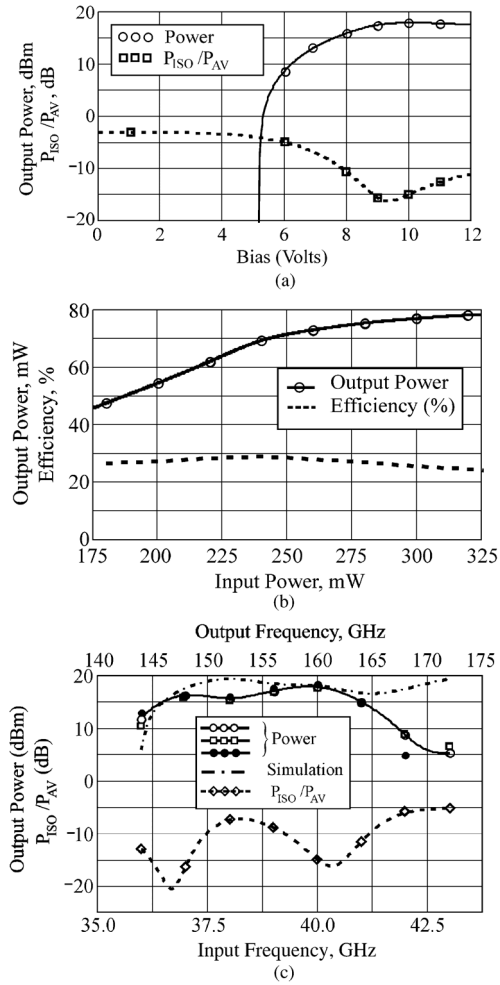

Fig. 12. (a) Output power and power at the isolation port of the quadrupler, normalized to input available power, at 160 GHz as a function of bias. (b) Quadrupler output power and efficiency, at a bias of 10 V and output frequency of 160 GHz, as a function of input power. (c) Output power and isolation port power (normalized to available input power) of the quadrupler versus frequency. The three sets of power data correspond to different quadrupler chips. The predicted performance from harmonic balance is shown as the dot-dash line.

Fig. 12(a) shows the measured output power of the quadrupler at 160 GHz as the (reverse) bias voltage to the diodes is varied. With 220 mW of available power at the input, a peak output power of 62 mW is obtained at a bias of 10 V. It should be noted that the orientation of the diodes requires application of a voltage with positive polarity through the DC bias channels to place the varactors in reverse bias. Fig. 12(a) also shows the power measured at the isolation port, normalized to the available power at the input port, as bias is varied. Within the operating band of the quadrature hybrid, this measurement represents power reflected from the two input doubler stages and provides a measure of their return loss. Below a bias voltage of 6 V, no output power was measured.

The quadrupler output power at 160 GHz and bias of 10 V as a function of input power is shown in Fig. 12(b). Over the 175–325 mW range of input power applied, the quadrupler efficiency remained approximately 25% or better, with a maximum efficiency near 30% at an input power of 240 mW. At an applied

input power of 325 mW, an output of 79 mW was obtained at 160 GHz.

Fig. 12(c) shows the multiplier output power and the power at the isolation port (normalized to available input power) over the 144–172 GHz output frequency range, corresponding to the 36–43 GHz bandwidth of the input amplifier. These measurements were performed with 220 mW of input power and a voltage bias of 10 V. The 3 dB output bandwidth of the quadupler is approximately 20 GHz, or 13%. The three sets of power data presented in Fig. 12(c) correspond to separate assemblies of the quadrupler, each using different chips, illustrating a high degree of repeatability and consistency in performance resulting from the integrated architecture of the multiplier. Results from simulation of the quadrupler circuit based on the *HFSS* and harmonic balance analysis used in the design are shown for comparison.

V. Thermal Characterization

As the input stage of a frequency multiplier chain is usually driven at the highest power levels (ranging from hundreds of milliwatts to several watts), thermal management and power handling often are important design considerations. Carrier velocity saturation will degrade a multiplier's performance at high applied voltages [15] and elevated temperatures contribute additional loss. Excessive heating is a significant issue for GaAs devices operating at submillimeter wavelengths as this material is generally a poor thermal conductor and is often thinned to only a few microns to mitigate excitation of substrate modes [19]. Consequently, researchers have directed significant effort towards improving the thermal grounding of these circuits, including bonding the GaAs-supported multipliers to highly thermal conductive substrates, such as diamond, to more efficiently remove heat [20].

To assess heating of the integrated quadrupler presented in this work, a single prototype input-stage doubler circuit was fabricated using the same diode design and process as described in Section III. This approach was chosen as the input doubler is subjected to the highest power levels in the quadrupler design and use of a single doubler stage (shown in Fig. 13) simplifies measurement and characterization. The doubler circuit incorporates the same input matching as the quadrupler design with its output coupled to a WR-12 waveguide. Because the quasi-vertical diode design utilized in the multiplier is bonded to silicon (which has thermal conductivity nearly a factor of three higher than GaAs) and the ohmic metal lies approximately 1 μm directly below the anode and GaAs epitaxy, the doubler is expected to perform favorably compared to GaAs membrane diodes with respect to heating.

The RF performance of the doubler is summarized in Fig. 14. Measurement of the doubler used the same basic experimental setup as shown in Fig. 11, with an additional directional coupler placed at the input to monitor reflection from the circuit. A peak doubler efficiency of 60% was achieved at 80 GHz for an input available power of 100 mW and bias of 10 V. The 3 dB bandwidth of the doubler [Fig. 14(b)] is approximately 18% and a maximum output power of 113 mW was achieved at 80 GHz with at input of 380 mW (the upper power limit of the Spacek amplifier). Above 400 mW of applied input power, the voltage

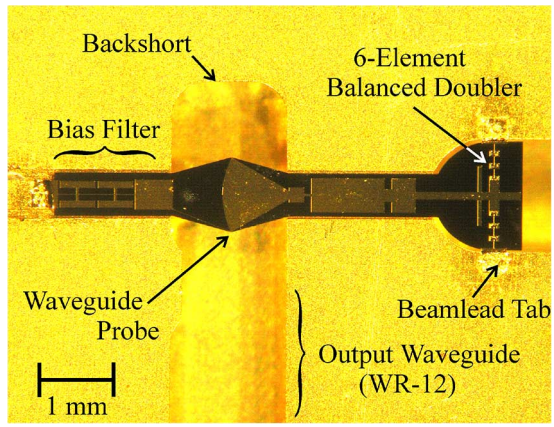

Fig. 13. Image of frequency doubler integrated on 15 μm silicon for thermal characterization.

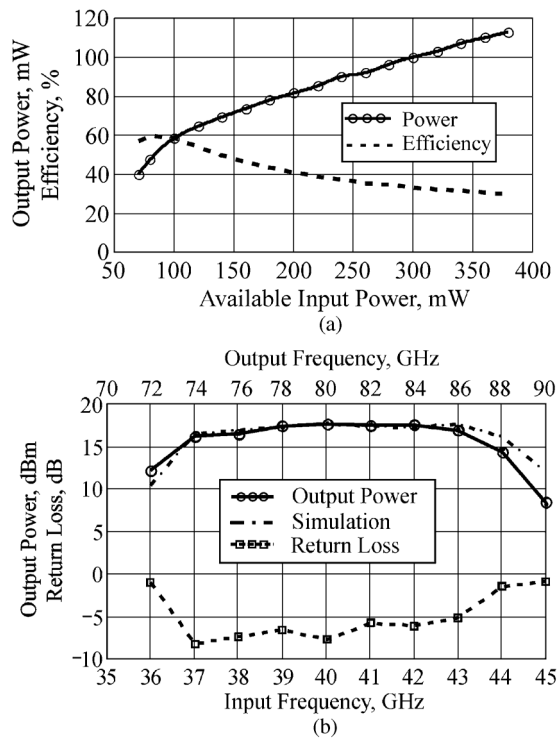

Fig. 14. (a) Output power and efficiency of the input-stage doubler at input frequency of 40 GHz and bias of 10 V as a function of available input power. (b) Output Power and return loss of the doubler as a function of frequency. The simulated output power from harmonic balance analysis is shown as the dot-dash line.

swing across the diodes is predicted, from harmonic balance analysis, to exceed the 9.5 V breakdown voltage of the individual diodes.

To estimate the operating temperature of the varactors comprising the doubler, the current-voltage characteristic of the diodes was used as an *in situ* thermometer. Initially, a set of dc current–voltage measurements of the six-element diode array were taken at temperatures ranging from 25 °C to 90 °C. These measurements were done with the doubler chip placed on a temperature-controllable hot plate, after the diodes were allowed to reach thermal equilibrium. Data taken from these measurements served as a calibration to permit the temperature

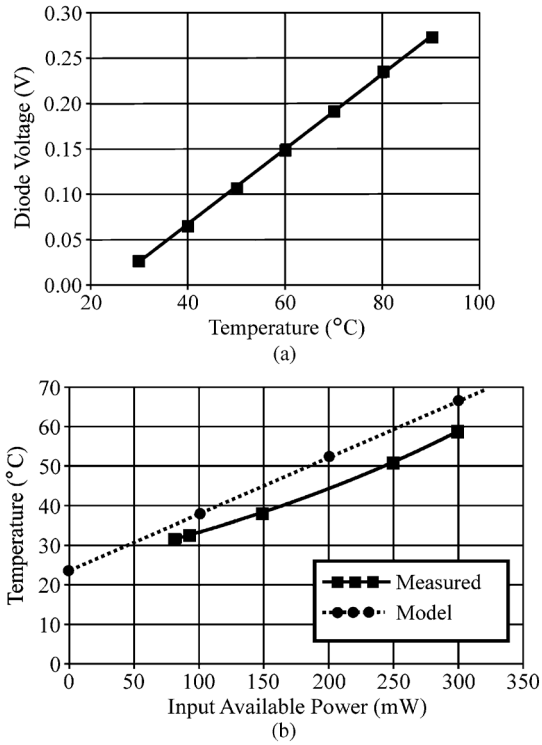

Fig. 15. (a) Measured change in the diode array voltage at a 100 μA bias as a function of temperature (slope of 4.1 mV/deg). (b) Estimated anode temperature of the integrated doubler as a function of input power. The modeled response shows the results from *SolidWorks* simulations.

of the diodes to be estimated when subjected to RF power. Fig. 15(a) shows the change in voltage drop across the diodes found from this measurement, at a fixed current bias of 100 μA and as a function of applied temperature.

The estimated temperature of the diodes in the doubler circuit as a function of available input power at 40 GHz is provided in Fig. 15(b). For this measurement, which was performed at Virginia Diodes, Inc. using a customized experimental setup based on the technique documented in [21], the doubler is pumped with the input RF signal at a fixed power for several seconds. Afterwards, the input power source is removed, a current bias of 100 μA immediately applied, and the diode voltage sampled and monitored over a time interval of 50 ms. Using the measured voltages, extrapolating, and applying the calibration data of Fig. 15(a) allows the temperature of the varactors to be estimated. Although this method cannot give temperature estimates for the individual diodes in the array, it does provide a measure of the approximate temperature rise of the devices when subjected to high input power levels. When driven at 100 mW for peak efficiency, the temperature of the varactors is estimated from these measurements to be 35 °C.

To assess the reasonableness of the temperature estimations described above, thermal analysis of the doubler structure was performed with Dassault Systémes' *SolidWorks* simulator. For this analysis, each of the six anodes is assumed to dissipate an equal amount of power and the doubler is assumed to have efficiency of 50%. Thus, for 100 mW of incident power, each anode is modelled as dissipating 8 mW. The thermal conductivities of the materials comprising the doubler in the *SolidWorks* analysis were 56 W/m-K for the 1 μm thick GaAs, 150 W/m-K for the 15 μm thick silicon membrane, and 0.6 W/m-K for the 500 nm thick spin-on glass used to bond the GaAs epitaxy to silicon (based on manufacturer's data). With the waveguide block acting as a heat sink at 23 °C, simulation gives an anode temperature of 38 °C, in respectable agreement with the temperature estimated from measurement. Fig. 15(b) compares the results of the *SolidWorks* simulation with measurement and suggest that the experimental approach likely underestimates the operating temperature of the varactors by a few degrees. It should be added that the peak efficiency of the integrated multiplier presented in this work (60%) is relatively high, a factor of approximately 2.5 times larger than the multipliers presented in [19], and this high efficiency clearly impacts heat dissipation and temperature rise in the devices. The maximum input drive level tested for the circuit was 300 mW, which yielded an estimated diode temperature near 60 °C.

VI. Summary

The multiplier described in this work, to the authors' knowledge, is the first integrated quadrupler demonstrated above 100 GHz. The balanced circuit architecture of the quadrupler addresses a number of challenges inherent in multiplier design, namely degradation in performance due to mismatch between adjacent stages in a chain and improved power-handling. Several quadrupler chips were measured, giving consistent results and illustrating the high degree of reproducibility achievable using a fully integrated design. The quadrupler yielded a peak efficiency at 160 GHz of 29% with output power of 70 mW.

A unique quasi-vertical GaAs diode was developed and employed to realize the quadrupler. Among the primary features of these devices are their vertical geometry with ohmic contact that underlies the GaAs epitaxy and anode. This structure brings the anode into close proximity with the ohmic metal and can be tailored to minimize the device series resistance and improve heat-sinking. Moreover, the diode epitaxy is transferred to high-resistivity silicon that is subsequently micromachined to form a thin (15 μm) fully integrated drop-in module with beamleads for electrical connection, alignment, and mounting.

Estimates of the anode temperature for the input-stage doubler of the quadrupler were made using the varactors as integrated thermometers. These measurements suggest the operating temperature of the input stage of the multiplier, when operating at peak efficiency, to be 35 °C.

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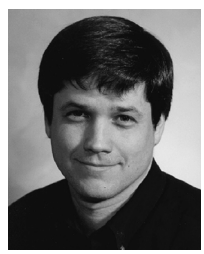

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