A 206 ~ 220 GHz CMOS VCO Using Body-Bias Technique for Frequency Tuning

Po-Han Chiang [2], Jen-Hao Cheng [1], Yi-Ching Wu [1], Chau-Ching Chiong [2], Wen-De Liu [3], Guo-Wei Huang [3], Tian-Wei Huang [1], Huei Wang [1]

[1] Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 10617, Taiwan
[2] Institute of Astronomy and Astrophysics, Academia Sinica, Taipei, 10617, Taiwan
[3] National Nano Device Laboratories, Hsinchu, 30078, Taiwan

Abstract — A 206 ~ 220 GHz varactor-free voltage-controlled oscillator (VCO) is proposed to improve the output power and tuning range. The topology of the VCO is push-push cross-coupled pair. By using body-bias technique, the parasitic capacitor of the cross-coupled pair can be adjusted, and the varactors in the conventional VCO design can be removed. The proposed VCO was designed and implemented in TSMC 65-nm CMOS technology with a chip size of 0.25 x 0.25 mm^2. The tuning range is 6.6% (from 206.2 to 220 GHz). The measured phase noise is -66 dBc/Hz at 1 MHz offset frequency. The output power is 1.3 dBm at 216 GHz with 54-mW dc power consumption and its maximum dc-to-RF efficiency is 2.1%. To the best of our knowledge, this varactor-free VCO achieves the highest dc-to-RF efficiency among published CMOS VCOs around 200 GHz.

Index Terms —Voltage-controlled oscillator (VCO), body-bias, CMOS, dc-to-RF efficiency.

I. Introduction

With the quick development of millimeter wave (MMW) applications such as high data rate communication, medical imaging, and spectroscopy [1], [2], the frequency sources are become important at sub terahertz. Using CMOS process has the advantage for high-level integration with baseband circuits, but the challenges of the VCOs in CMOS are the low breakdown voltage, high substrate loss, and lower unit current gain frequency (f_T).

In the past decade, many VCOs above 200 GHz using CMOS process were published [3]–[7]. However, most tuning methods of the VCOs are varactor-based. Because the quality factor of varactors decreases rapidly with frequency [5], these VCOs suffered from relatively low output power level and narrowed tuning range. At such high frequency (i.e. frequency > 200 GHz), it is difficult to realize a amplifier. Therefore, a high output power and wide tuning range signal source is necessary. A couple of varactor-free oscillators have been reported recently [5]–[7], but they still have some drawbacks such as high dc power consumption and low dc-to-RF efficiency.

The technique of the adaptive body bias is widely used in many circuits [8]–[11]. It has been proposed to reduce the impact of the die-to-die threshold voltage (V_{th}) variations [8]. Also, the forward-body-bias (FBB) is used to reduce V_{th} and enhance the f_T [9]–[10]. Furthermore, reversed-body-bias (RBB) technique is also used to improve the power handling for the switches [11].

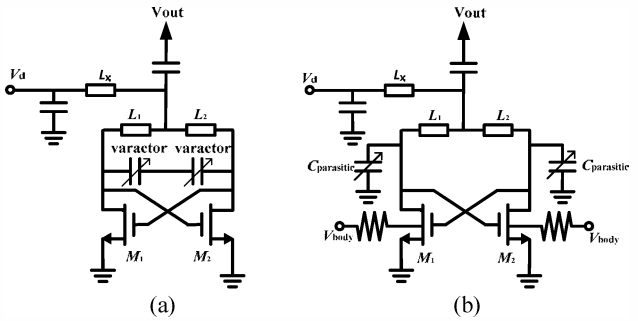


Fig. 1. Schematic of the (a) conventional push-push VCO and (b) the proposed varactor-free push-push VCO.

In this paper, the body-bias technique is utilized to design a wide tuning-range G-band VCO. Unlike traditional varactor-tuning mechanism shown in Fig. 1(a), body bias technique is used to control the parasitic capacitors of the cross-coupled pair to adjust tuning range. Without the capacitance of the varactors, the larger device size is utilized to provide higher output power. At 1.2-V supply voltage, the tuning range of the proposed VCO is 6.6%. The maximum output power is 1.3 dBm and the correspondent dc power consumption is 54 mW. Compared with CMOS VCOs around 200 GHz, this work demonstrates the highest dc-to-RF efficiency of 2.1%.

II. Circuit Design

The circuit schematic of the proposed varactor-free VCO is shown in the Fig. 1(b). The M_1 and M_2 form the cross-coupled pair. Without the varactors, large size of the transistors (M_1-M_2) are chosen to provide sufficient negative resistance and produce higher output power. It can also increase the slope of the tuning curve due to larger parasitic capacitance. However, large transistor size leads to higher dc power consumption. Therefore, there is a design trade-off between output power and dc power consumption. The optimized size of M_1 and M_2 are chosen as 33.6 μm.

Since the VCO is designed to operate at high frequency, the inductors L_1 and L_2 are implemented by microstrip lines. The line length is 14 μm and the width is 5 μm. The inductance of L_1 and L_2 are both 11.6 pH. The inductors L_1 – L_2 and parasitic

978-1-4799-8275-2/15/$31.00 ©2015 IEEE

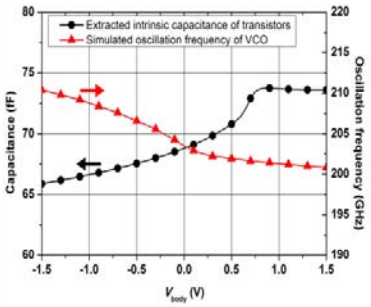


Fig. 2. Simulated parasitic capacitance and oscillation frequency versus body-bias voltage (V_{body}).

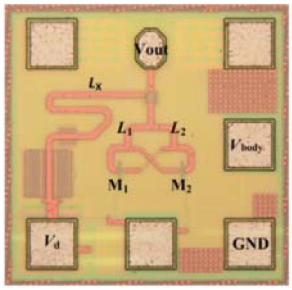


Fig. 3. Chip micrograph of the proposed VCO.

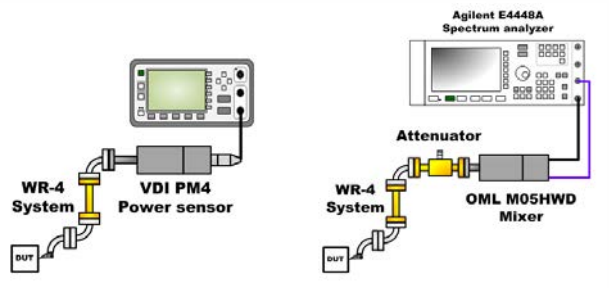
capacitors of the cross-coupled pair (M_1–M_2) serve as the bandpass filter to pass through the fundamental oscillation frequency.

As shown in Fig. 1(a), conventional VCO commonly uses varactor to control the tuning range. However, the quality factor of varactor decreases rapidly with increasing frequency that leads to the narrow tuning range. The fundamental oscillation frequency of the VCO can be expressed as [12]

$$\omega_{\text{osc}} = \frac{1}{\sqrt{LC_{\text{par}}}}, \quad C_{\text{par}} = C_{\text{gs}} + C_{\text{db}} + 4C_{\text{gd}} \qquad (1)$$

where C_{gs} is the gate-to-source capacitance , C_{db} is the drain-to-body capacitance, C_{gd} is the gate-to-drain capacitance and C_{par} is total parasitic capacitance. These intrinsic capacitances of the transistors can be extracted by calculating the Y-parameters [13]. Fig. 2 shows the simulated capacitance of C_{par} and the frequency tuning curve under different body-bias conditions (from -1.5 V to 1.5 V).

It is observed that C_{par} varies with body-bias voltage (V_{body}). C_{par} decreases from 74 to 68 fF while the V_{body} increases from -1.5 V to 1.5 V. As C_{par} changes, the oscillation frequency changes as well. The simulated tuning range is about 5.4% (from 199 GHz to 210 GHz). By adopting this property, the body-bias technique can replace the function of the varactor. Moreover, the output power can be preserved without output buffer amplifier due to the absence of the varactor. As show in Fig. 1, the 1.2-V supply voltage is fed through the quarter-wavelength transmission line L_X at 200 GHz. In addition to serving as dc feed, L_X exhibits a high impedance to ensure the second-harmonic signal flow to the output. The V_{body} is connected to the body of M_1 and M_2 through 2-KΩ resistors to adjust the output frequency.



(a) (b)

Fig. 4. Measurement setups for (a) output power measurement and (b) frequency measurement.

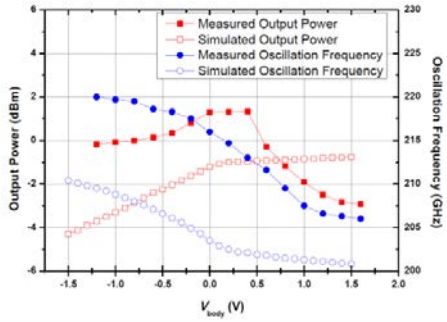


Fig. 5. Measured dc-to-RF efficiency versus V_{body}.

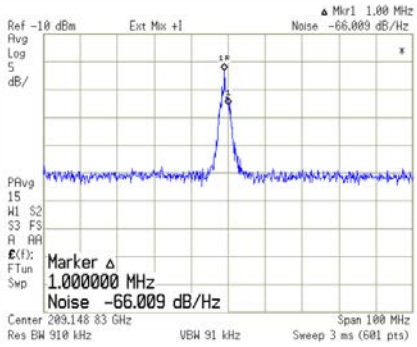


Fig. 6. Measured phase noise at 209 GHz (-66 dBc/Hz at 1 MHz offset frequency.

III. Experimental Results

The VCO was designed and fabricated in a 65-nm CMOS technology with 3.4-μm ultra-thick metal (UTM). The chip photo is shown in Fig. 3, and the chip size is 0.25 × 0.25 mm^2. The measurement setups for output power and frequency are illustrated in Fig. 4(a) and Fig. 4(b) respectively. Theses setups contain a WR−4 waveguide, an Agilent E4448A spectrum analyzer, an OML M05HWD mixer, an attenuator and a power sensor. The losses due to the cables, adaptors and probes have been carefully calibrated. Operating at 1.2-V supply voltage, the dynamic dc current is from 39 mA to 71 mA. Fig. 5 shows the measured tuning characteristics and output power versus V_{body}. The tuning range of the proposed VCO is about 6.6% (from 206.2 GHz to 220 GHz). The measured output power is larger than −4 dBm among the tuning range and the maximum output power is 1.3 dBm with 45-mA dc current. The frequency discrepancy is caused by the

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED CMOS VCOS ABOVE G-BAND.

Ref.	Tech. (CMOS)	Design feature	Freq. (GHz)	Output Power (dBm)	Tuning Range (%)	Phase Noise (dBc/Hz)	DC Power (mW)	Max. dc-to-RF efficiency (%)	Chip size (mm^2)	FOM (dB)
[3]	130-nm	push-push cross-coupled	192	-20	0.68	-100 @10 MHz	16.5	0.06	0.176	-173
[4]	90-nm	colpitts	196	-19	2.3	NA	29	0.04	0.189	N/A
[5]	65-nm	multi-core oscillators	290 320	-1.2 -3.3	4.5 2.6	-78 @1 MHz -77 @1 MHz	325 339	0.23 0.14	0.36	-162.1 -161.8
[6]	65-nm	multi-core oscillators	260	0.5	9.5	-78 @1 MHz	800	0.14	2.25	-157
[7]	65-nm	multi-core oscillators	256	4.1	4.3	-94 @1 MHz	227	1.14	0.4355	-178
This Work	**65-nm**	**push-push cross-coupled**	**220**	**-1.6**	**6.6**	**-66.3 @1 MHz -81 @10 MHz**	**43.2**	**2.1**	**0.0625**	**-154**

$$\mathrm{FOM} = L(\Delta\omega) - 20\cdot\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\cdot\log\left(\frac{P_{dc}(\mathrm{mW})}{1mW}\right) \quad [4]$$

inaccurate device model at such high operating frequency. The maximum dc-to-RF efficiency is 2.1%. The measured phase noise at 209 GHz is −66 dBc/Hz at 1 MHz offset frequency, as shown in Fig. 6. The figure of merit (FOM) [4] of the proposed VCO is −154 dB. Table I summaries the performances of previously reported CMOS VCOs around 200 GHz, and this work achieves 6.6% tuning range and the highest dc-to-RF efficiency.

IV. CONCLUSION

The proposed varactor-free G-band VCO has been designed and fabricated in a 65-nm CMOS technology. By using body bias technique, the parasitic capacitance of the cross-coupled pair varies with the body-bias voltage. This VCO achieves a 6.6% tuning range (from 206.2 to 220 GHz) and 1.3-dBm output power at 1.2-V supply voltage, while the dc power consumption is from 46.8 mW to 85.2 mW. The maximum dc-to-RF efficiency is 2.1% at 216 GHz. The proposed VCO achieves a wide tuning range and the highest dc-to-RF efficiency among recently published CMOS VCOs around 200 GHz.

V. ACKNOWLEDGEMENT

This work is supported in part by the Ministry of Science and Technology, Taiwan under Contract NSC 101-2219-E-002-007, Contract NSC 102-2918-I-002-002, Contract NSC 102-2219-E-002-005 and NTU Research Excellence Project no. NTU-ERP-104R8908. The chip fabrication is supported by TSMC University Shuttle Program.

REFERENCES

[1] P. H. Siegel, "Terahertz technology in biology and medicine," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 10, pp. 2438–2447, Oct. 2004.

[2] R. Han, Y. Zhang, Y. Kim, D. Kim, H. Shichijo, E. Ahshari, and K. K. O, "280 GHz and 860 GHz image sensors using schottky-barrier diodes in 0.13μm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp. 254–256, Feb. 2012.

[3] C. Cao and K. K. O, "192 GHz push-push VCO in 0.13μm CMOS," *Electron. Lett.*, vol. 42, pp. 208–210, Feb. 2006.

[4] H.-Y. Chang, H. Wang, "A 98/196 GHz low phase noise voltage controlled oscillator with a mode selector using a 90 nm CMOS process," *IEEE Microw. and Wireless Compon. Lett.*, vol. 19, no. 3, pp. 170–172, Mar. 2009.

[5] Y. Tousi, O. Momeni, and E. Afshari, "A novel CMOS high-power terahertz VCO based on coupled oscillators: Theory and implementation," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012.

[6] R. Han, E. Afshari, "A 260GHz broadband source with 1.1 mW continuous-wave radiated power and EIRP of 15.7dBm in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 138–139, Feb. 2013.

[7] M. Adnan, E. Afshari, "A 247-to-263.5 GHz VCO with 2.6 mW peak output power and 1.14% dc-to-RF efficiency in 65nm bulk CMOS," *ISSCC Dig. Tech. Papers*, pp. 262–263, Feb. 2014.

[8] S. Narendra, D. Antoniadis, and V. De, "Impact of using adaptive body bias to compensate die-to-die Vt variation on within-die Vt variation," in *Low Power Electronics and Design Symp.*, pp. 229–232, Jun. 1999.

[9] C.-P. Chang, J.-H. Chen, Y.-H. Wang, "A fully integrated 5 GHz low-voltage LNA using forward body bias technology." *IEEE Microw. and Wireless Compon. Lett.*, vol. 19, no. 3, pp. 176–178, Mar. 2009.

[10] D. Wu, R. Huang, W. Wong, Y. Wang, "A 0.4-V low noise amplifier using forward body bias technology for 5 GHz application." *IEEE Microw. and Wireless Compon. Lett.*, vol. 17, no. 7, pp. 543–545, Jul. 2007.

[11] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 31–39, Jan. 2006.

[12] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGRAW-Hill.

[13] G. Dambrine, et al., "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 36, pp. 1151–1159, Jul. 1988.