Design and Analysis of 239 GHz CMOS Push-Push Transformer-Based VCO With High Efficiency and Wide Tuning Range

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***Abstract*—A push-push transformer-based voltage-controlled oscillator (VCO) is proposed and analyzed to achieve high efficiency and a wide tuning range at sub-terahertz (THz) frequencies. Analyses show that the coupling factor of the transformer to obtain high output power ($\mathrm{P_{OUT}}$) has to be carefully chosen by consideration of gate-to-drain voltage gain as well as matching impedances seen from the drain and to the gate of a VCO transistor at the 2nd harmonic frequency ($2f_o$). Analysis also shows that the transformer-based resonator allows a wide tuning range. In addition, it has been shown that the introduction of a parallel inductor to a varactor leads to high $\mathrm{P_{OUT}}$ and low phase noise. The proposed 239 GHz VCO with a 65 nm CMOS process demonstrates the high efficiency of 1.45%, the $\mathrm{P_{OUT}}$ of -4.8 dBm, and the wide tuning range of 12.5% with a supply voltage of 1.2 V.**

***Index Terms*—High efficiency, J-band, millimeter wave, push-push oscillator, terahertz, transformer, voltage-controlled oscillator (VCO), wide tuning range.**

I. Introduction

SINCE THZ signals can pass through nonmetallic materials and allow high resolution-imaging due to their small wave-lengths, many THz image systems for enclosed objects have been researched [1]. In addition, THz communication systems for high data rates have been also actively developed to utilize wide bandwidths [2]. They can be also used to identify substances by finding unique features in their absorption spectra [3]. Thus, THz signals are expected to open various new applications, including applications in bio and medical areas [4].

To implement such systems, THz signal sources are necessary. The sources have been made optically [5] or electrically. Recently, CMOS signal sources have been able to produce high-frequency signals up to 1 THz using harmonic signals [6], as CMOS technology has been scaled down. Because CMOS technology has the advantage of integration with other functions, it could be beneficial in realizing small and integrated systems. However, it still has challenges to achieve high $\mathrm{P_{OUT}}$, high DC-to-RF efficiency, and a wide frequency tuning range. This is because the supply voltage also must be reduced as it is scaled down. Also, the transconductance ($\mathrm{g_m}$) of a transistor is quite small at high frequencies close to $f_{\max}$. Moreover, the low Q factor of a varactor limits the tuning range and degrades the $\mathrm{P_{OUT}}$.

Several VCO design methods have been introduced to have high frequencies. In particular, push-push structures, which can produce 2nd harmonic signals by using two fundamental anti-phased signals in an oscillator [7] have been widely used. Because the $\mathrm{g_m}$ of a transistor and the Q factor of a varactor at the fundamental frequency are higher than those at high frequencies, better performance can be expected. To obtain a higher $\mathrm{P_{OUT}}$, one can combine powers from a number of coupled oscillators in a chip [8], [9] or combine the powers from antennas after radiation [10], [11]. The respective oscillator in the coupled oscillators should have high efficiency.

Some previous works have designed high-$\mathrm{P_{OUT}}$ oscillators with high efficiency by optimizing the gate-to-drain voltage gain of a transistor. By using an n-stage ring oscillator, the phase of a gain stage is adjusted to the optimum value [10], [12]. In other previous works, the optimum phase has been obtained by the insertion of a transmission line between gate and drain [9], [11], [13]. The 2nd harmonic signal loss due to the low impedance of a gate of a VCO transistor has been considered as well [8], [9], [11].

The low Q factor of a varactor in a VCO degrades the $\mathrm{P_{OUT}}$ because of the small voltage swing. To overcome this problem, variable phase delays between adjacent stages have been introduced to achieve a wide tuning range while obtaining high power [8], [9], [13]. However, this approach also has a limitation because the Q factor of the respective coupled oscillator should be low to allow a wide tuning range, which leads to small $\mathrm{P_{OUT}}$ [8]. The distribution of negative gm cells in a $\Lambda/2$ standing wave oscillator also has been introduced to enable a wide tuning range [24], but high 2nd harmonic power cannot be generated because the voltage swings across the distributed gm cells are small. Previous works [14], [15] has shown that a Colpitts VCO without a varactor has high efficiency, in which the frequency tuning is obtained by gate bias control.

In this paper, a 239 GHz push-push transformer-based VCO is proposed, which allows high efficiency and a wide tuning range at the same time. By using the transformer-based VCO

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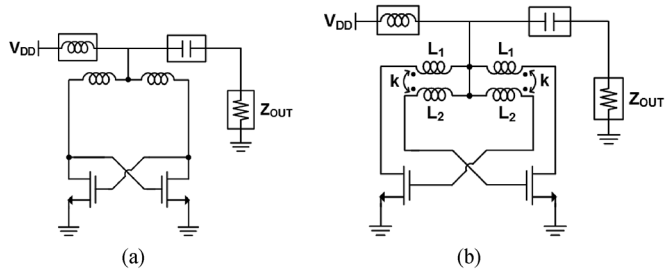


Fig. 1. Schematic of (a) a conventional push-push cross coupled oscillator for comparison and (b) the proposed push-push transformer-based oscillator.

structure, the gate-to-drain voltage gain becomes close to the optimum value, and the load impedance at $2f_o$ is matched with the conjugate of the drain impedance, which are necessary conditions to have high P_{OUT}. These are dependent on the coupling factor of the transformer. This will be explained in Section II. The transformer-based structure also provides a wide tuning range, which will be discussed in Section III. Finally, in Section IV, it will also be shown that the P_{OUT} can be enhanced by the introduction of a parallel inductor to the VCO varactor. The supply voltage used in all analyses was 1 V. As a result, the proposed VCO achieved the high P_{OUT} and efficiency of -4.8 dBm and 1.47% at a supply voltage of 1.2 V, respectively. The tuning range is 12.5%, which is the highest among the state-of-art VCOs over 200 GHz.

II. Determination of Coupling Factor for High P_{OUT}

Fig. 1(a) shows a conventional push-push direct cross coupled oscillator (DXCO) and Fig. 1(b) presents the proposed push-push transformer-based oscillator for high P_{OUT}. Transformer-based oscillators without a harmonic output signal have been already introduced in previous works [6]–[8]. This configuration shows an advantage of low phase noise due to the enhanced Q factor of the resonator by a factor of $1 + k$, where k is the coupling factor of the transformer. The higher voltage swing, caused by the high Q factor of the resonator, leads to increased harmonic power. Thus, according to previous works, as the coupling factor approaches 1, better performance in terms of the fundamental output power and the phase noise are expected.

However, as the oscillation frequency goes up, the best performance is obtained at a coupling factor less than 1. Fig. 2(b) shows the equivalent circuit of the transformer-based oscillator using the T-equivalent model of a transformer shown in Fig. 2(a). At the optimum value of the coupling factor, the phase (Φ) of the gate-to-drain voltage gain of the VCO transistor has to be the optimum value, which maximizes the generated power of the transistor at the fundamental frequency (f_o). This leads to high voltage swing and the resultant high 2nd harmonic output power.

The 2nd harmonic P_{OUT} is also affected by impedance matching conditions at $2f_o$. First, the load impedance (Z_L) which is closer to the conjugate of the drain impedance (Z_D) has the transistor produce the higher 2nd harmonic power. Second, the large magnitude of the transformed gate impedance (Z_T) can reduce the gate leakage. The Z_L and Z_T values as well as the gate swing voltage are strongly dependent on the coupling factor. We analyze these mechanisms in section A and B. Eventually, the optimum coupling factor and output impedance (Z_{OUT}) for high P_{OUT} are found by load pull simulation at $2f_o$, which will be discussed in section C.

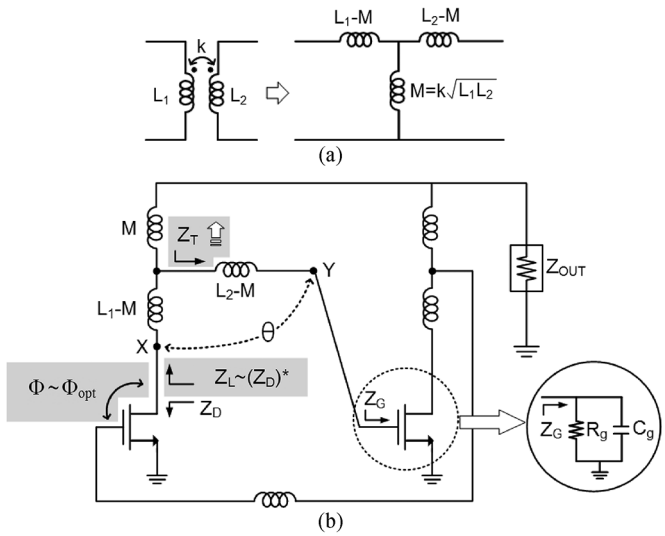


Fig. 2. (a) T-equivalent model of a transformer and (b) equivalent circuit of the transformer-based oscillator.

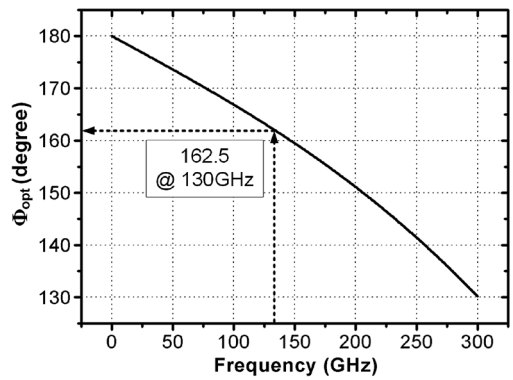


Fig. 3. Simulated optimum phase of gate-to-drain voltage gain of a NMOS transistor with the size of 18 μm/60 nm(= W/L).

A. Optimum Phase and Amplitude of Gate-to-Drain Voltage Gain for High Voltage Swing

Previous works derived the optimum phase and the amplitude of the gate-to-drain voltage gain of a VCO transistor. To maximize the generated power of the transistor, the optimum phase should be [12]

$$\Phi_{\rm opt} = \angle - (y_{21} + y_{12}^*), \tag{1}$$

where y_{21} and y_{12} are the y-parameters of the transistor. Previously, [11] also verified that if the following conditions are satisfied, the amplitude should be 1:

$$\begin{aligned} 2g_{11} &< |y_{12} + y_{21}^*|, \\ 2g_{22} &< |y_{12} + y_{21}^*| \end{aligned} \tag{2}$$

where g_{ij} denotes the real parts of $y_{ij}(i, j = 1, 2)$.

Using the extracted y-parameters of a transistor $(W/L = 3 \times 6\ \mu m/60\ nm)$, the optimum phase of the voltage gain is plotted in Fig. 3. This shows that the optimum phase is 162.5 degree at 130 GHz.

In this work, the phase difference (Φ) between drain and gate is tailored by the coupling factor of the transformer. Because the total phase change in an oscillation loop must be 360 degrees, the phase change (θ) caused by the transformer reduces the phase difference between gate and drain, or $\Phi = 180^\circ - \theta$.

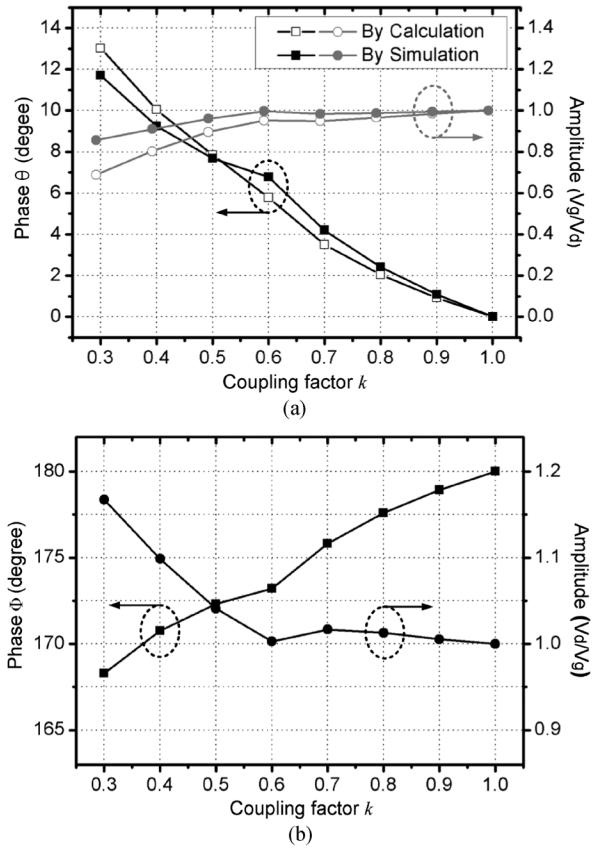


Fig. 4. (a) Calculated and simulated phase (θ) and amplitude changes caused by transformer. (b) Simulated phase (Φ) and amplitude of the voltage gain.

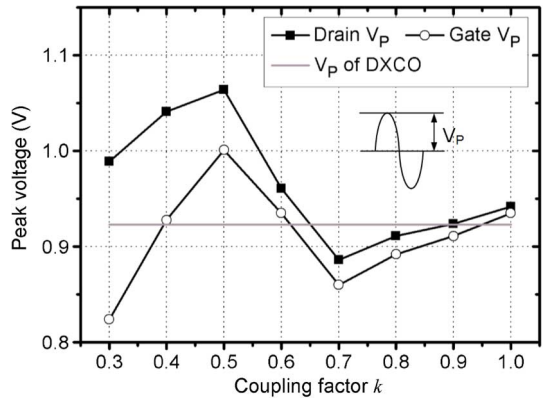


Fig. 5. Simulated peak voltage of gate and drain for fundamental frequency.

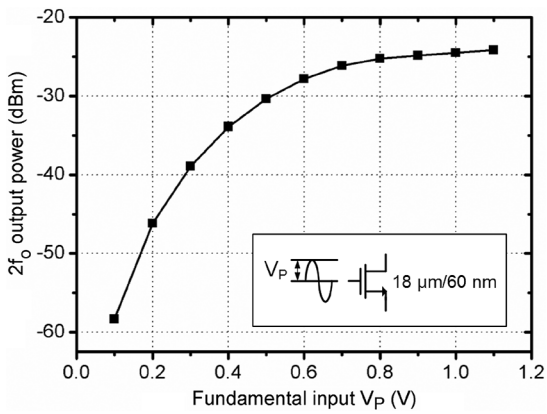


Fig. 6. Simulated 2nd harmonic (260 GHz) power with 50 Ω load with respect to fundamental (130 GHz) input peak voltage.

To find θ, we calculated the transfer function of $\mathrm{V_Y/V_X}$ in Fig. 2(b):

$$\frac{V_Y}{V_X} = -\frac{kR_g}{\omega^2 L \cdot (1-k^2) \cdot C_g R_g - R_g - j\omega L \cdot (1-k^2)}, \tag{3}$$

where $\mathrm{R_g}$ and $\mathrm{C_g}$ are the gate resistance and gate capacitance, respectively. Here, $\mathrm{L_1 = L_2 = L}$ is assumed, and the loss of the inductor is ignored for simple analysis. The phase and amplitude changes caused by the transformer are given as

$$\angle\left(\frac{V_Y}{V_X}\right) = \theta = \arctan\left(\frac{\omega L(1-k^2)}{R_g\left(\omega^2 L C_g (1-k^2) - 1\right)}\right), \tag{4}$$

$$\left|\frac{V_Y}{V_X}\right| = \frac{kR_g}{\sqrt{\left\{\omega^2 L \cdot (1-k^2) \cdot C_g R_g - R_g\right\}^2 + \left\{\omega L \cdot (1-k^2)\right\}^2}}, \tag{5}$$

The phase change θ increases with the decrease in the coupling factor k, because it is mainly influenced by the inductance L and the coupling factor k of the numerator of (4). In reality, the phase change is further increased due to the increase of the inductance $(\mathrm{L_{1,2}})$ to maintain the oscillating frequency. We calculated the phase and amplitude changes and plotted them with the simulated results of the oscillator in Fig. 4(a). In the calculation, $\mathrm{C_g}$ included the Miller effects of the drain-gate capacitance as well as the gate-source capacitance. The calculated results agree very well with the simulated results.

Based on the above results, the phase and amplitude of the transistor voltage gain were obtained and presented in Fig. 4(b). Note that the phase change approaches the optimum value at the smaller coupling factor k, but the amplitude moves away from the optimum value of 1. When the coupling factor k is under 0.5, the amplitude change rapidly increases. Therefore, the optimum coupling factor k for high voltage swing is determined by considering this trade-off. Fig. 5 shows the simulated gate and drain peak voltages. To find the peak voltages, a harmonic balance simulation was carried out, and the peak voltages were obtained at the fundamental frequency (f_o). The Q factors of the inductors were set as 30, which is a realistic value. The peak voltages are highest at the coupling factor k of 0.5, where the amplitude change begins to increase with the decreases in the coupling factor k. In the range of $k > 0.7$, the enhancement of the resonator Q-factor [16] is observed, so the drain peak voltage increases again. The maximum gate peak voltage is higher than that of a conventional push-push DXCO by 0.08 V as seen in Fig. 1(a).

Fig. 6 plots the relation of the 2nd harmonic power with a 50 Ω load to the input gate peak voltage. It shows that a large gate voltage swing is necessary to have a high 2nd harmonic output power. However, when the gate peak voltage is higher than 0.8 V, the 2nd harmonic output power is slightly changed by the increase of the voltage swing. Nevertheless, there is a significant difference in the final $\mathrm{P_{OUT}}$. This is due to the matching condition at $2f_o$.

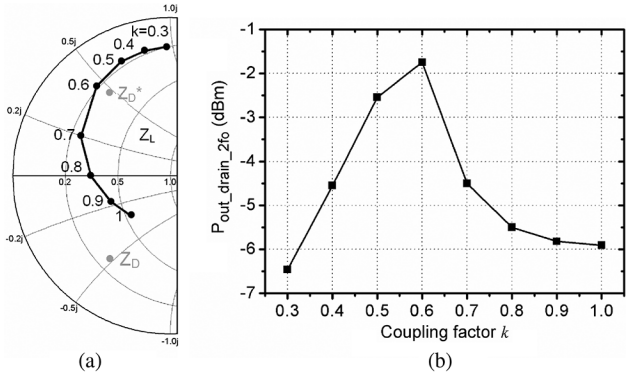


Fig. 7. (a) Drain impedance $\mathrm{Z_D}$ and load impedance $\mathrm{Z_L}$ at 260 GHz and (b) simulated 2nd harmonic power at the drain of the transistor in the oscillator.

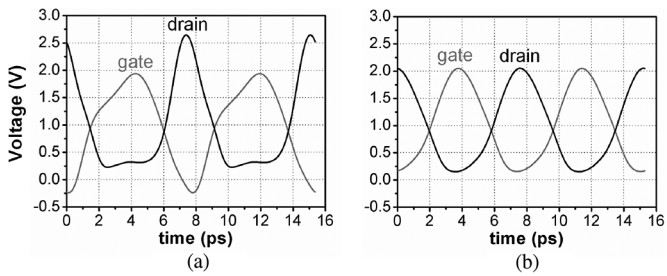


Fig. 8. Voltage waveform of drain and gate at (a) $\mathrm{k} = 0.5$ and (b) $\mathrm{k} = 1$.

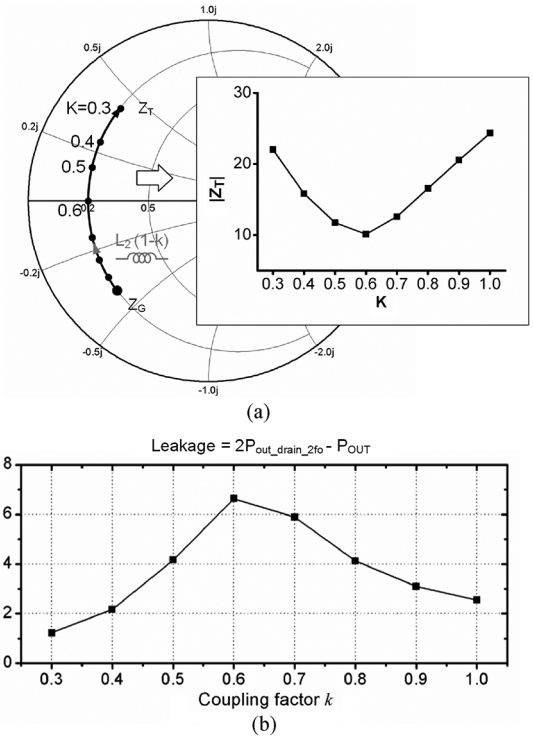


Fig. 9. (a) Gate impedance $\mathrm{Z_G}$ and its transformed impedance $\mathrm{Z_T}$ by inductance of $\mathrm{L_2 - M}$ at 260 GHz and (b) simulated 2nd harmonic leakage power.

B. Effects of Impedance Matching on P_{OUT} *at* $2f_\mathrm{o}$

Conjugate Matching at Drain (Z_L)*:* The maximum 2nd harmonic power can be generated by the transistor when the load impedance is conjugate-matched to the drain at $2f_\mathrm{o}$. Fig. 7(a) presents the drain impedance $(\mathrm{Z_D})$ and the load impedance $(\mathrm{Z_L})$ in Fig. 2(b). In the simulation to find the optimum $\mathrm{Z_L}$, the $\mathrm{Z_{OUT}}$ was set to be the optimum value $(\mathrm{Z_{OPT}})$ to obtain maximum $\mathrm{P_{OUT}}$. When the coupling factor k is 1, the $\mathrm{Z_L}$ is capacitive because the overall capacitive impedance of the gate appears. As the coupling factor increases, the $\mathrm{Z_L}$ becomes inductive. Then, the load impedance is very close to the conjugate of the $\mathrm{Z_D}$ at the coupling factor k of 0.6. The simulated 2nd harmonic power at the drain, presented in Fig. 7(b), also shows that the largest power is generated at the coupling factor k of 0.6. This implies that the drain matching condition at $2f_\mathrm{o}$ has a greater effect on the generation of the 2nd harmonic power than the amplitude of the gate voltage swing when the gate peak voltage is higher than 0.8 V.

Increase in the generated 2nd harmonic power can be also found in the voltage waveforms. Fig. 8 shows the simulated voltage waveforms of drain and gate at the coupling factor k of 0.5 and 1. When the coupling factor k is 0.5, the peak drain voltage of the fundamental component is about 0.1 V higher than when the coupling factor k is 1, as shown in Fig. 5. However, this figure shows that the real drain voltage swing at the coupling factor k of 0.5 is much larger than that at the coupling factor k of 1 because of the higher 2nd harmonic power.

Magnitude of Gate Impedance (Z_T)*:* A previous work [11] showed that a high impedance looking into the gate gives a high $\mathrm{P_{OUT}}$ by blocking the 2nd harmonic signal leakage to the gate. Unfortunately, the transformer-based oscillator has large 2nd harmonic leakage to the gate due to its low impedance at high frequencies. We plotted $\mathrm{Z_T}$ and $|\mathrm{Z_T}|$ in Fig. 9(a). When the coupling factor k is 1, the $\mathrm{Z_T}$ is equal to the $\mathrm{Z_G}$. As the coupling factor k increases, $|\mathrm{Z_T}|$ decreases until the coupling factor k of 0.6. It increases again with a larger coupling factor. Because the smaller $|\mathrm{Z_T}|$ increases the leakage power, the simulated leakage power is inversely related to the $|\mathrm{Z_T}|$, as shown in Fig. 9(b). The leakage power is obtained by subtracting the $\mathrm{P_{OUT}}$ from the generated power shown in Fig. 7(b). The $\mathrm{P_{OUT}}$ is the simulated power at the push-push output, which will be discussed more in next section. This shows that the oscillator has the highest leakage power at the coupling factor k of 0.6 as expected.

This analysis gives a design insight into how to achieve high $\mathrm{P_{OUT}}$. When the coupling factor k is less than 0.6, the large inductor $\mathrm{L_2}$ leads to large $|\mathrm{Z_T}|$ and low leakage power. Thus, high $\mathrm{P_{OUT}}$ can be obtained at the push-push output. This mechanism is also used to explain $\mathrm{P_{OUT}}$ enhancement after the introduction of a parallel inductor to the VCO varactor.

C. Output Matching at $2f_\mathrm{o}$

Because the above factors have different tendencies to maximize the 2nd harmonic output power with respect to the coupling factor k, the optimum coupling factor k was eventually found through the load pull simulation, which revealed the maximum power and efficiency as well as the $\mathrm{Z_{OPT}}$ [17]. Fig. 10 shows the 2nd harmonic load-pull simulation results obtained when the coupling factors were 0.3, 0.5, 0.7, and 0.9. The $\mathrm{Z_{OPT}}$s with respect to coupling factor k vary slightly, but they give much higher output power and efficiency in comparison with the output impedance of 50 Ω. In the case of $\mathrm{k} = 0.5$, the maximum power and efficiency were -3.73 dBm and 1.95%, respectively. The output power was 2.5 dB higher than that of the oscillator

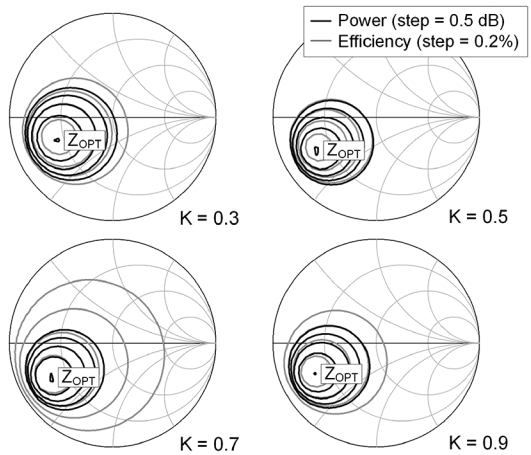


Fig. 10. 2nd harmonic load-pull simulation results at k = 0.3, 0.5, 0.7, and 0.9.

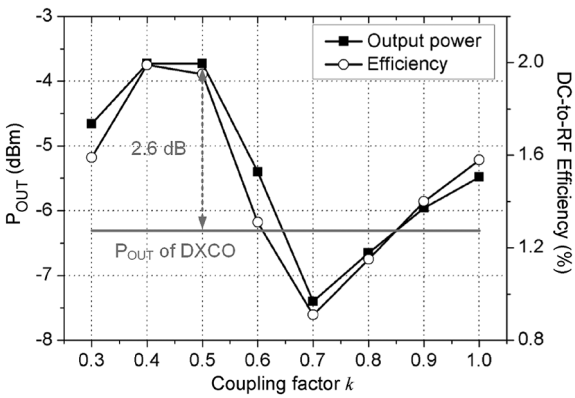


Fig. 11. Maximum push-push P_{OUT} and DC-to-RF efficiency.

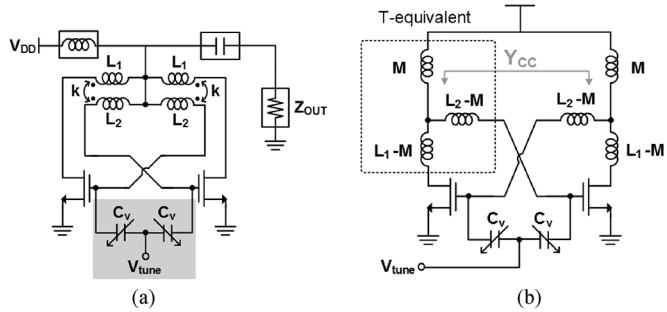


Fig. 12. (a) Schematic of the transformer-based VCO with varactor and (b) its equivalent circuit.

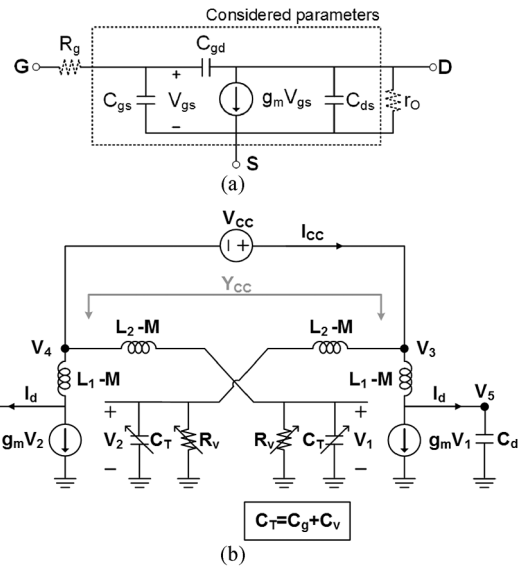


Fig. 13. (a) Simplified model of the transistor and (b) cross coupled part of the transformer-based VCO for admittance calculation.

with the output impedance of 50 Ω. The efficiency also became 1% higher than that of the oscillator with a 50 Ω load.

We also carried out a load-pull simulation with respect to every coupling factor k and obtained the maximum power and efficiency for every coupling factor k. The results are presented in Fig. 11. This graph shows that the maximum P_{OUT} is obtained at the coupling factors of 0.4 and 0.5, in which the DC-to-RF efficiency also has the highest value. In comparison to the conventional push-push DXCO, the P_{OUT} and DC-to-RF efficiency of the proposed oscillator are 2.6 dB and 0.72% higher, respectively.

In summary, coupling factor k was used to satisfy the optimum signal conditions and the conjugate match condition at $2f_o$. It was also used to increase Z_T so that there will be less 2nd harmonic leakage. At the same time, Z_{OUT} was optimized by 2nd harmonic load-pull simulation to allow high P_{OUT}.

III. Transformer-Based VCO for Wide Tuning Range

The transformer-based VCO including varactors at the gates is presented in Fig. 12(a). The transformer-based structure gives a wide tuning range because the capacitance control range in the resonator becomes larger than that of the varactor itself. To verify this, we analyzed its equivalent circuit [18] presented in Fig. 12(b). We calculated the admittance (Y_{CC}) of the cross coupled part. The simplified transistor model was used for this analysis as shown in Fig. 13(a). We ignored the resistive parameters of R_g and r_o for simplicity. Including the model, the cross coupled part is presented for the admittance calculation in Fig. 13(b).

From Fig. 13(b),

$$Y_{CC}(s) = -\frac{1}{2} \cdot \frac{g_m - (sC_T + 1/R_v) - \alpha}{1 + (sC_T + 1/R_v) \cdot s(L_2 - M)}, \quad (6)$$

where $\alpha = sC_d/(1+s^2C_dL_1(1-k))\{1+(sC_T+1/R_v)\cdot s(L_2-M) + s(L_1-M)g_m\}$.

The total capacitor (C_T) comprises the gate capacitor (C_g) and the varactor (C_v). Here, C_d and R_v denote the drain capacitance and the parallel resistor of the varactor, respectively.

From equation (6), see equations at bottom of next page. If $\omega(L_2 - M) \ll R_v$, then

$$Re\{Y_{CC}\} \approx -\frac{g_m/\{1-\omega^2C_d(L_1-M)\}}{2\{1-\omega^2C_T(L_2-M)\}} + \frac{1/R_v}{2\{1-\omega^2C_T(L_2-M)\}^2}, \quad (9)$$

$$\mathrm{Im}\{Y_{CC}\} \approx \frac{\omega C_T}{2\{1-\omega^2C_T(L_2-M)\}} + \frac{\omega C_d}{2\{1-\omega^2C_d(L_1-M)\}^2}. \quad (10)$$

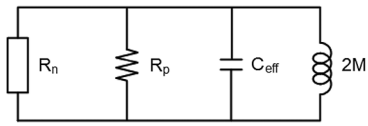


Fig. 14. Simplified equivalent circuit of the transformer-based VCO.

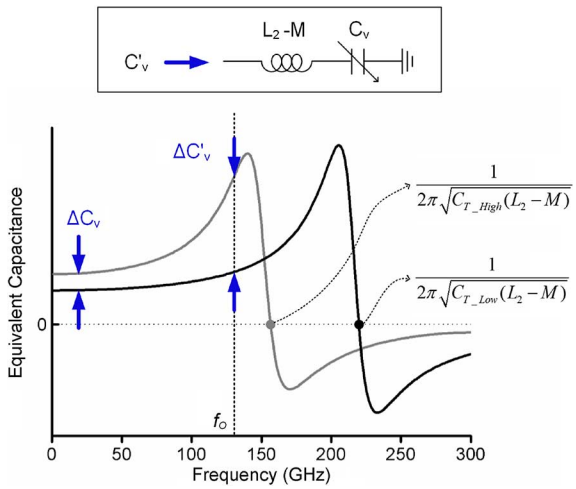


Fig. 15. Capacitance variation of varactor with series inductor.

From (7) and (8), we obtained the equivalent negative resistance ($\mathrm{R_n}$), positive resistance ($\mathrm{R_p}$), and effective capacitance (C_{eff}) shown in Fig. 14:

$$R_n = -\frac{2\left\{1-\omega^2 C_T(L_2-M)\right\}\left\{1-\omega^2 C_d(L_1-M)\right\}}{g_m}, \tag{11}$$

$$R_p = 2R_v\left\{1-\omega^2 C_T(L_2-M)\right\}^2, \tag{12}$$

$$C_{eff} = \frac{C_T}{2\left\{1-\omega^2 C_T(L_2-M)\right\}} + \frac{C_d}{2\left\{1-\omega^2 C_d(L_1-M)\right\}^2}. \tag{13}$$

In (13), the $\mathrm{C_T}$ and the $\mathrm{C_d}$ of the effective capacitances C_{eff} are increased by the factors of $\{1-\omega^2\mathrm{C_T}\cdot(\mathrm{L_2}-\mathrm{M})\}$ and $\{1-\omega^2\mathrm{C_T}\cdot(\mathrm{L_2}-\mathrm{M})\}^2$, respectively. At the same time, the amount of the capacitance change is also increased due to its denominator of $\{1-\omega^2\mathrm{C_T}\cdot(\mathrm{L_2}-\mathrm{M})\}$. When $\mathrm{C_T}$ is increase, the denominator decreases. This enhances the variation of the total capacitance. Fig. 15 depicts this mechanism. By inserting series inductor $(\mathrm{L_2}-\mathrm{M})$ with the varactor, the capacitance drastically increases as the frequency goes up. By decreasing the coupling factor k (or increasing inductance), the series resonance frequency approaches the oscillating frequency. The amount of effective capacitance change ($\Delta\mathrm{C_v'}$) becomes much larger than that of the varactor. This results in the wide tuning range of the VCO.

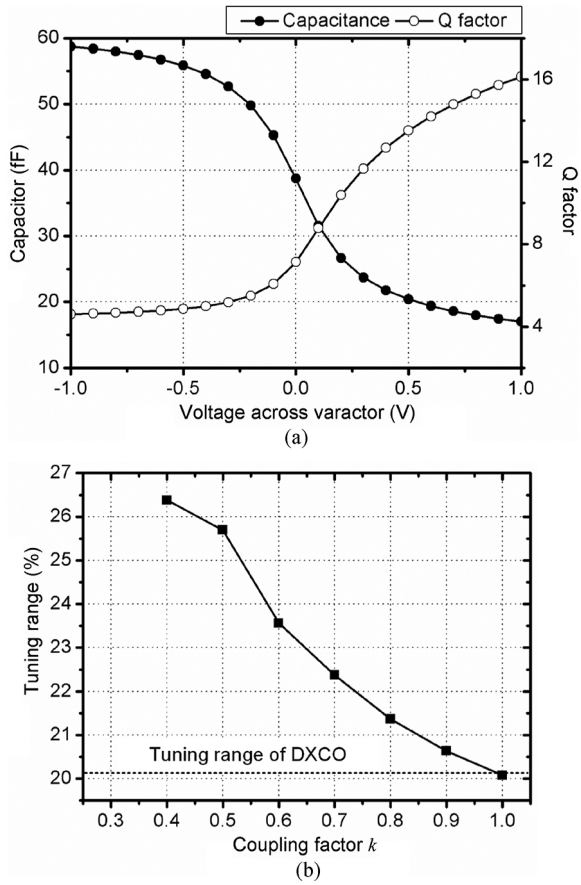


Fig. 16. (a) Characteristic of the varactor at 130 GHz and (b) the simulated tuning range.

The used varactor characteristic is presented in Fig. 16(a), and Fig. 16(b) shows the tuning range of the VCO according to the coupling factor k. It shows that the tuning range increases with a smaller coupling factor k. When the coupling factor k is 0.4, the tuning range is 6.1% higher than that of the conventional DXCO.

IV. $\mathrm{P_{OUT}}$ Enhancement Using Parallel Inductor

Even if start-up conditions are satisfied when equivalent transconductance $\mathrm{G}_m(=-1/\mathrm{R_n})$ is greater than $1/\mathrm{R_p}$, the

$$Re\{Y_{CC}\} = \frac{1/R_v - gm\left\{1-\omega^2 C_T(L_2-M)\right\}/\left\{1-\omega^2 C_d(L_1-M)\right\}}{2\left\{1-\omega^2 C_T(L_2-M)\right\}^2 + 2\left\{\omega(L_2-M)/R_v\right\}^2}, \tag{7}$$

$$\mathrm{Im}\{Y_{CC}\} = \frac{\omega C_T\left\{1-\omega^2 C_T(L_2-M)\right\} + \omega(L_2-M)(g_m/Rv-1)}{2\left\{1-\omega^2 C_T(L_2-M)\right\}^2 + 2\left\{\omega(L_2-M)/R_v\right\}^2} + \frac{\omega C_d\left[\left\{1-\omega^2 C_T(L_2-M)\right\}^2 + \omega^2(L_2-M)\{(L_2-M)/R_v^2 + (L_1-M)g_m/R_v\right]}{\left\{1-\omega^2 C_d(L_1-M)\right\}\left[2\left\{1-\omega^2 C_T(L_2-M)\right\}^2 + 2\left\{\omega(L_2-M)/R_v\right\}^2\right]}. \tag{8}$$

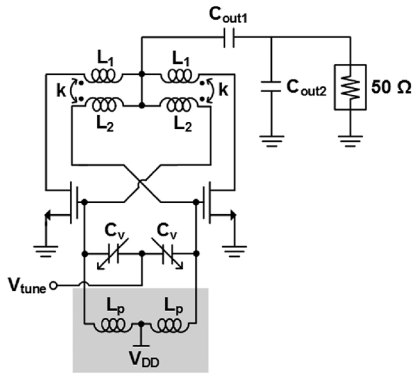


Fig. 17. Transformer-based VCO including a parallel inductor ($\mathrm{L_P}$) to the varactor.

$\mathrm{G_m}$ value should be much larger than $1/\mathrm{R_p}$ ($\mathrm{G_m} \gg 1/\mathrm{R_p}$) for large voltage swing [25]. Therefore, the magnitude of $\mathrm{G_mR_p}$ is an indicator of voltage amplitude.

From (11) and (12),

$$G_m R_p = \frac{g_m R_v \left\{1 - \omega^2 C_T (L_2 - M)\right\}}{1 - \omega^2 C_d (L_1 - M)}. \tag{14}$$

This shows that $\mathrm{G_mR_p}$ decreases with the increase in the $\mathrm{C_v}$ as well as the decrease in the $\mathrm{R_v}$, which vary in relation to applied bias cross the varactor. Hence, the $\mathrm{P_{OUT}}$ is decreased further than when only the $\mathrm{R_v}$ is considered. In addition, it becomes worse with a small coupling factor k. To alleviate the degradation, an inductor of $\mathrm{L_P}$ parallel to the varactor is introduced as shown in Fig. 17.

The parallel inductor effectively enhances $\mathrm{G_mR_p}$. Including the parallel inductor, the elements of the equivalent circuit are given as shown in the equations at the bottom of the page. Then,

$$G'_m R'_p = \frac{g_m R_v \left\{1 + (1/L_P - \omega^2 C_T) \cdot (L_2 - M)\right\}}{1 - \omega^2 C_d (L_1 - M)}. \tag{18}$$

Here, $\mathrm{R'_n}$, $\mathrm{R'_p}$, $\mathrm{C'_{eff}}$, and $\mathrm{G'_m}$ are equivalent negative resistance, positive resistance, effective capacitance, and equivalent transconductance with the consideration of $\mathrm{L_p}$. Equation (18) shows that a smaller $\mathrm{L_P}$ reduces the degradation of $\mathrm{G'_mR'_p}$ due to the increase in $\mathrm{C_T}$. In this way, the improved $\mathrm{G'_mR'_p}$ leads to high voltage swing, low phase noise, and resultant high $\mathrm{P_{OUT}}$.

However, a smaller $\mathrm{L_P}$ also results in a smaller gate voltage swing due to its low impedance. To identify the optimum $\mathrm{L_P}$, we simulated VCO performance in regards to voltage swing amplitude, phase noise, $\mathrm{P_{OUT}}$, and tuning range with respect to the $\mathrm{L_P}$, as shown in Fig. 18. When the $\mathrm{L_P}$ decreases, the transformer inductors ($\mathrm{L_{1,2}}$) should be adjusted so that the oscillation frequency remains at 130 GHz. In the simulation, the Q factors

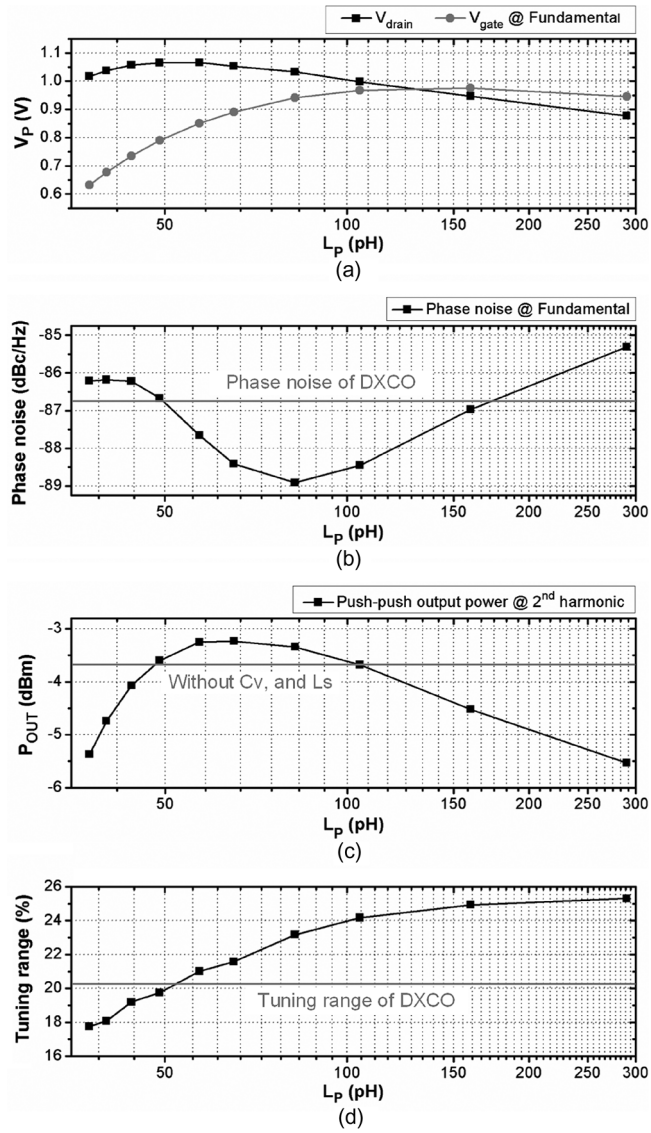


Fig. 18. (a) Peak voltage at drain and gate, (b) phase noise at fundamental frequency, (c) push-push output power, and (d) tuning range. (a), (b), and (c) are obtained at minimum capacitance of varactor.

of all inductors are also set to be 30, and the coupling factor is fixed as 0.5.

Fig. 18(a) shows that the drain voltage swing increases by the introduction of the $\mathrm{L_P}$. As previously mentioned, too small $\mathrm{L_P}$ reduces the voltage swing because of low impedance at the gate. The phase noise is also improved, and its minimum value is -88.9 dBc/Hz at a 1 MHz offset in the $\mathrm{L_P}$ of 82 pH as shown

$$R'_n = -\frac{2\left\{1 + (1/L_P - \omega^2 C_T) \cdot (L_2 - M)\right\}\left\{1 - \omega^2 C_d (L_1 - M)\right\}}{g_m}, \tag{15}$$

$$R'_p = 2R_v \left\{1 + (1/L_P - \omega^2 C_T) \cdot (L_2 - M)\right\}^2, \tag{16}$$

$$C'_{eff} = \frac{C_T}{2\left\{1 + (1/L_P - \omega^2 C_T) \cdot (L_2 - M)\right\}} + \frac{C_d}{2\left\{1 - \omega^2 C_d (L_1 - M)\right\}^2}. \tag{17}$$

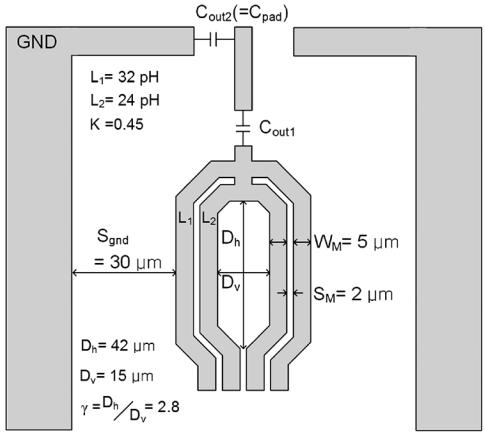


Fig. 19. Layout and dimension of the transformer-based resonator.

in Fig. 18(b). It is 2 dB lower than that of the conventional DXCO. Fig. 18(c) shows that P_{OUT} is enhanced by the introduction of the L_P. The small L_P allows the large L_2, so that the P_{OUT} increases due to the higher magnitude of the impedance seen at the gate, $|Z_T|$. Note that the maximum P_{OUT} does not decrease, even when large varactors are used for a wide tuning range. Fig. 18(d) shows that the tuning range is slightly reduced by the introduction of the L_P because the change of the effective capacitance in (17) decreases. However, the tuning range is still larger than that of the conventional DXCO in the enhanced output power region with L_P.

The L_P also provides another advantage of eliminating the choke inductor. This makes the push-push output matching network very simple, and additional area for a choke inductor is not necessary.

V. Design of Transformer-Based Resonator

We have analyzed the P_{OUT} and the tuning range of the transformer-based VCO with respect to the coupling factor of the transformer in the previous sections. As a result, the coupling factor should be between 0.4 and 0.5 for high P_{OUT} and a wide tuning range. In addition, the inductance of L_2 should be large enough at the 2nd harmonic frequency to reduce the leakage of the 2nd harmonic power caused by the gate. The final schematic of the proposed VCO is presented in Fig. 17.

In reality, the inductances of L_1, L_2 and L_P were reduced to keep the operating frequency the same because parasitic capacitances were introduced by metal lines for power combining and cross coupled interconnection. Therefore, the inductances of L_1, L_2 and L_P are 32 pH, 24 pH, and 41.5 pH, respectively. The layout and dimensions of the final design are presented in Fig. 19. The coupling factor k is simulated to be 0.45, which is achieved by a 2 μm space between L_1 and L_2. In this design, the ratio (γ) between the inner diameters in the horizontal direction (D_h) and the vertical direction (D_v) is 2.8. When γ is close to 1, the Q factor of the inductor is the highest. However, a higher γ has the advantage of higher P_{OUT} because the common-mode inductance of L_2 becomes the larger at the 2nd harmonic frequency.

The optimum output impedance was identified by the load-pull simulation including electromagnetic (EM) simulation of the circuit. As shown in Fig. 19, the matching network was constructed by a series capacitor (C_{out1}) and shunt capacitor (C_{out2}), which are introduced by a probing pad.

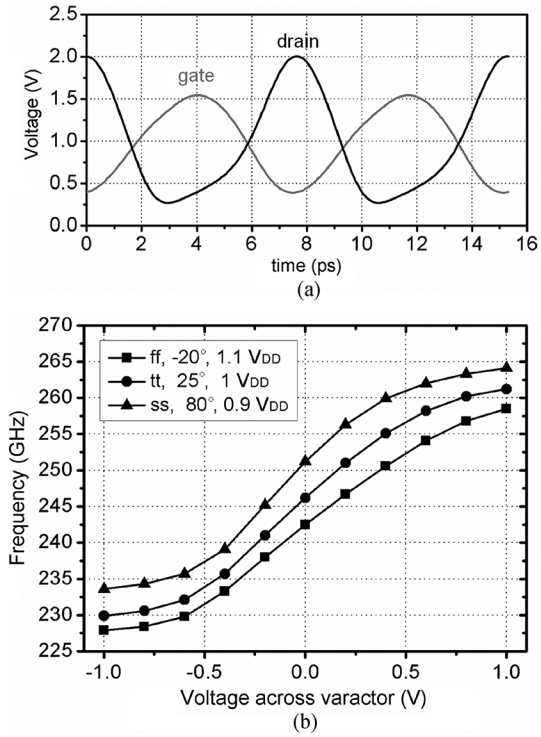


Fig. 20. (a) Simulated waveform of drain and gate for final version of VCO and (b) simulated frequency tuning curve for PVT variations.

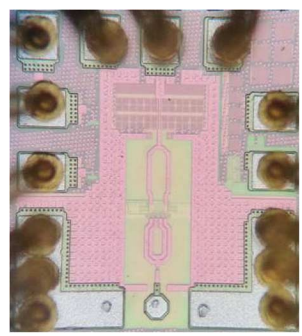


Fig. 21. Chip photograph (400 μm × 450 μm).

Fig. 20(a) shows the waveforms of drain and gate for the final version of the VCO, and which amplitude satisfies the reliability of the transistor. We also simulated and plotted the frequency tuning over process, temperature, and supply (PVT) variations, as shown in Fig. 20(b). The maximum deviation of frequency was about 9.6 GHz for a given control voltage. The maximum P_{OUT} was also varied from -10.5 dBm to -1.6 dBm (typically -5 dBm) over the PVT variations.

VI. Implementation and Measurement Results

The chip was fabricated using a TSMC 65 nm CMOS process. A photograph of the chip is presented in Fig. 21; it measured 400 μm × 450 μm including pads. It was mounted on an FR4-PCB board for measurement, and all biases were applied through bonding wires. For spectrum and phase noise measurement, the set-up was configured as shown in Fig. 22. A WR3.4 SHM 2nd sub-harmonic mixer of VDI mixed the output signal with 115 GHz signal from a frequency multiplier of Quinstar. Then, the output signal is converted down to the 10 GHz frequency range. By sweeping the frequency of the

TABLE I
COMPARISON WITH STATE-OF-THE-ART VCOS OVER 200 GHZ

	Frequency (GHz)	TR (%)	P_{OUT} (dBm)	Efficiency (%)	P_{dc} (mW)	Phase noise (dBc/Hz)	technology
This	239	12.5[1)]	-4.8	1.47	18.5	-98.43 to -110.9 @ 10MHz offset	65nm CMOS
[14]	221	10.8[2)]	-6.2	0.28	86.4	-90.5 @ 1MHz offset	90nm CMOS
[19]	240	5.6	-7	1.53	13	-93 @10MHz offset	32nm CMOS
[9]	256	4.3 (6.5) [2)]	4.1	1.14	227	-94 @1MHz offset	65nm CMOS
[11]	260	1.4 (9.5)[3)]	0.5[4)]	0.14[5)]	800	-78.3 @1MHz offset	65nm CMOS
[10]	288	1.4[2)]	-1.5	0.3	275	-87 @10MHz offset	65nm CMOS
[15]	293	5.74	-2.74[4)]	2.76[5)]	19.2	-93 @10MHz offset	65nm CMOS
[20]	543	4.04	-31	0.005	16.8	NA	40nm CMOS
[21]	290	8	-14	0.04	105.6	-80.28 @1MHz offset	90nm SiGe BiCMOS
[22]	232	11.7	-3.6	0.81	54	-98 @10MHz offset	120nm SiGe HBT
[23]	255	5.7	2.9	2.29	85	-87.8 @10MHz offset	250nm InP HBT

1) Including only frequency tuning by varactors.
2) Including frequency tuning by change of supply voltage.
3) Pulse modulation.
4) Radiated power.

1) Including only frequency tuning by varactors.
2) Including frequency tuning by change of supply voltage.
3) Pulse modulation.
4) P_{OUT} calculated from their radiation efficiencies.

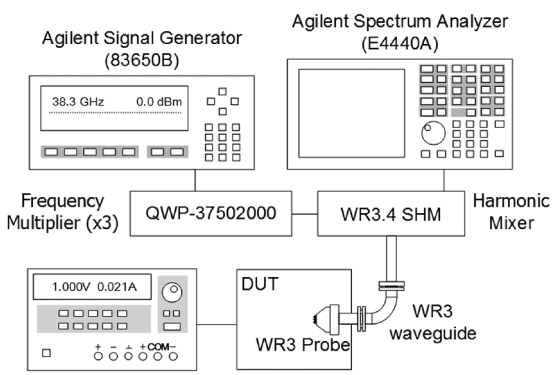


Fig. 22. Measurement setup for spectrum and phase noise.

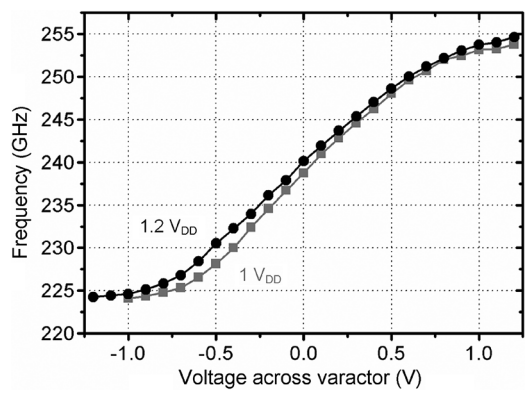


Fig. 23. Measured tuning range of VCO.

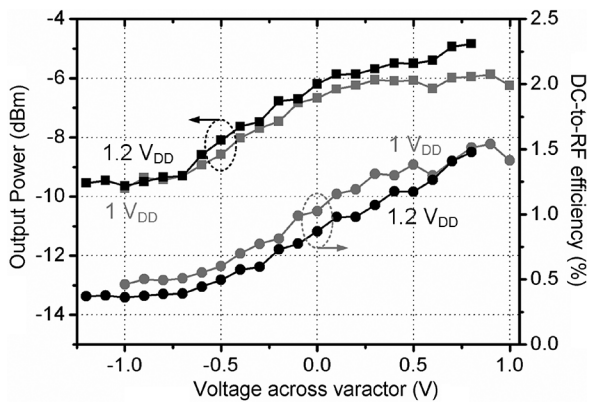


Fig. 24. Measured P_{OUT} and DC-to-RF efficiency of VCO.

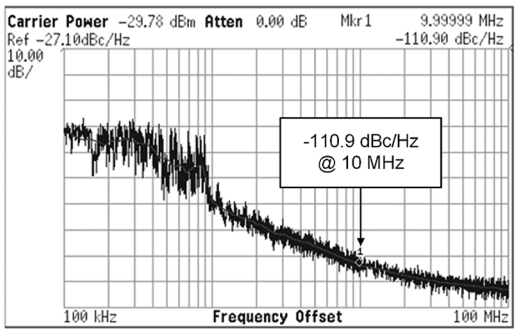
signal generator, we measured the whole frequency range using E4440A, of which the frequency range was DC to 26.5 GHz. To measure the P_{OUT}, we used a PM4 power meter of VDI. A WR3 probe of GGB, two 90° bent waveguides (EB3R-90) of CMI and a taper waveguide (WR-3.4 to WR-10) of VDI were used. Their losses were about 3 dB, 2 dB and 0.38 dB, respectively.

From the spectrum measurement, we plotted the frequency of the output signal with respect to the applied varactor voltage in Fig. 23. It changed from 224 GHz to 254 GHz (12.5%). The P_{OUT} and DC-to-RF efficiency are presented in Fig. 24. The supply voltage was 1.2 V, and its current varied from 18.5 mA to 25 mA according to the applied varactor voltage. The maximum P_{OUT} was -4.8 dBm, and the minimum P_{OUT} was -9.5 dBm. The DC-to-RF efficiency varied from 0.37% to 1.47%. It still showed higher efficiency than the conventional cross coupled oscillators. Fig. 25 shows the measured phase noise. At the frequencies of 224 GHz and 254 GHz, the phase noise values were -110 dBc/Hz and -98.43 dBc/Hz at the 10 MHz offset, respectively.

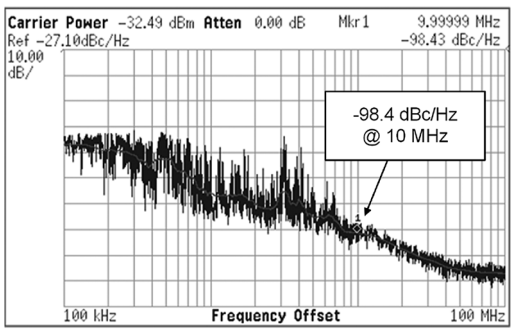
Table I compares this work to the previous works which have the state-of-art performance of tuning range and DC-to-RF efficiency over the frequency of 200 GHz. This work demonstrates a wide tuning range and high efficiency at the same time, and the tuning range is the highest among VCOs over 200 GHz.

VII. CONCLUSION

A 239 GHz transformer-based VCO with a wide tuning range and high efficiency was presented. The optimum coupling factor



(a)



(b)

Fig. 25. Measured phase noise at (a) 224 GHz and (b) 254 GHz.

of the transformer to obtain high P_{OUT} was determined to satisfy following conditions: 1) the phase and the amplitude of the gate-to-drain voltage gain of a VCO transistor are close to their optima at f_o, 2) the transformer load impedance is matched to the conjugate of the drain impedance at $2f_o$, and 3) the 2nd harmonic leakage to the gate is minimized. The coupling factor range of 0.4 to 0.5 was simply found to be the optimum by load-pull simulations with respect to the coupling factors. A wide tuning range is also accomplished by using the transformer-based VCO. The P_{OUT} reduction due to the low Q varactor is overcome by the introduction of an inductor that is parallel to it, which enhances the equivalent $G_m \cdot R_p$. This also leads to increased P_{OUT} and low phase noise at the small expense of tuning range.

As a result, the proposed VCO achieved the wide tuning range of 12.5% and the high efficiency of 1.47%. This tuning range is the highest among the state-of-art VCOs over 200 GHz.

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