64 to 86 GHz VCO Utilizing Push-Push Frequency Doubling in a 80 GHz f_T SiGe HBT Technology

Gang Liu, A. Çağrı Ulusoy, Andreas Trasser and Hermann Schumacher

gang.liu@uni-ulm.de
Institute of Electron Devices and Circuits, Ulm University
Albert-Einstein-Allee 45, 89081 Ulm Germany

***Abstract*— In this paper, the authors present a VCO/doubler IC with an output frequency near the maximum frequency of oscillation of the technology used. The IC operates from 64 GHz to 86 GHz with a maximum output power of -3.4 dBm at 79 GHz. It is designed using an 0.8 μm SiGe HBT technology with f_T/f_{max} of 80/90 GHz. The high frequency of operation is achieved by push-push frequency doubling. -4.5 dBm output at 87.1 GHz was reached by increasing the supply voltage. To the authors' knowledge, a frequency generation IC operating so close to f_{max} with comparably wide tuning range and high output power has not yet been reported.**

***Index Terms*— VCO, Push-Push, Frequency Doubler.**

I. Introduction

Emerging millimeter-wave applications, such as 60 GHz high-speed data transmission, 79 GHz automotive radar, 94 GHz imaging sensor etc., are putting increasing demands on the output frequency of solid-state oscillators. However, the maximum output frequency, in fundamental mode, achievable with a certain technology is limited by its maximum frequency of oscillation f_{max}. Oscillation beyond half of f_{max} is generally difficult to obtain. To further extend the oscillator output frequency, push-push oscillators are commonly used. Oscillators that produce signals above f_{max} have been reported [1] [2], but with quite low output power. Output power can be improved through a tuning network at the output, which also limits the tuning range as a drawback [3]. This work shows that high oscillation frequency (near f_{max}), high output power and wide tuning range can be achieved by combining a fundamental VCO with a highly efficient push-push frequency doubler.

The presented VCO was designed for the 60 GHz down-conversion stage of a consumer-oriented multi-GBit/s short-range data link. The output power generated by the VCO is adequate to drive a 60 GHz mixer designed using the same technology. It successfully demonstrates that a 60 GHz frequency down-conversion stage is feasible using this low-cost technology, despite the relatively low f_T and f_{max}.

II. Technology Overview

The technology used for this work is a commercially available, low cost, 0.8 μm SiGe HBT process from Telefunken Semiconductors GmbH & Co. KG, Germany. It offers two types of NPN transistors. A selectively implanted collector (SIC) improves the f_T from 50 GHz (for the non-SIC npn transistor) to 80 GHz, with a lower collector-emitter breakdown voltage (BV_{CEO}) of 2.4V (4.3V for the non-SIC npn transistor). PN, Zener and varactor diodes are available and four types of resistors, as well as MIM and Nitride (optional) capacitors are provided. The process features a three-layer metal system, with a top thick metal of 2.55 μm thickness. Two types of substrates are available (20 Ωcm and 1000 Ωcm). The low resistivity 20 Ωcm substrate was used in this design.

III. Circuit Description

To achieve high oscillation frequency and output power, a combination of a fundamental VCO and a push-push frequency doubler was chosen. Compared with push-push oscillators, where the output is usually taken from the common node of the oscillator circuit itself, high output power is easier to achieve. The fundamental VCO was designed to have wide tuning range and high fundamental power. The push-push doubler was then optimized for maximum output power at the doubled frequency.

A. Fundamental VCO

The fundamental VCO is the improved version of the one reported in [5], by the same authors. Fig. 1 shows the schematic. It is fully differential, with two differential output branches. One was connected to the frequency doubler and the other one is intended to drive a frequency divider, which can be used in a phase locked loop. The VCO has a negative resistance topology. The varactor diodes (C_{VAR}) connected to the emitter of T_1 generate a negative real part of the impedance looking into the bases of T_1 and T_2. The base inductors (L_B) complete the resonance and determine the oscillation frequency. To isolate the VCO core from the load, a common-base stage (T_3 and T_4) was used as output buffer. Output matching was done through L_{C1} and L_{C2} to increase the output

power. All inductors and matching networks were realized as Thin-Film Microstrip Lines (TFMLs). Several varactor diodes were connected in parallel to increase their Q-factor. Biasing was done by using resistive voltage dividers and current sources. The fundamental VCO generates around 7 dBm output power with more than 10 GHz tuning range.

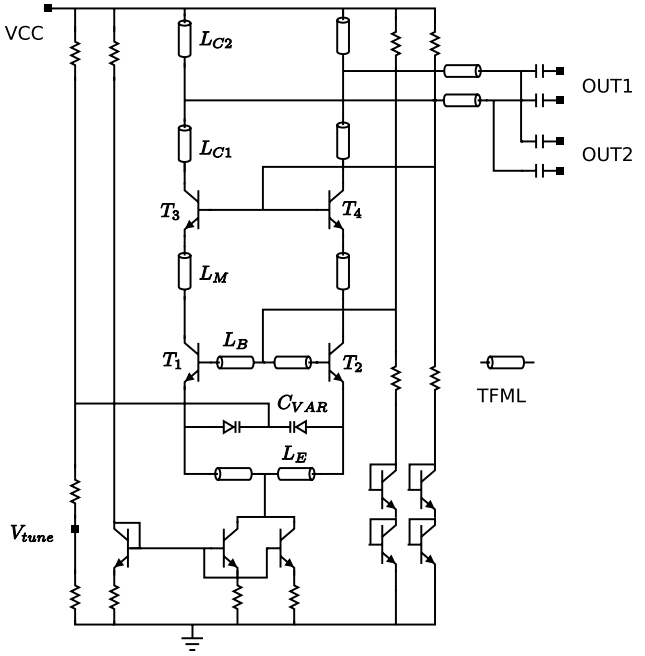

Fig. 1. Schematic of the fundamental VCO.

B. Push-Push Frequency Doubler

To double the fundamental frequency, a simple push-push frequency doubler was used. Fig. 2 shows the schematic of the frequency doubler. It consists mainly of a transistor pair. Biasing was done through a current mirror and a resistive voltage divider. The input signal is fed into the bases of the transistor pair while the output is taken from the emitter node. L_e is a stacked inductor which utilizes the available three metal layers and has an inductance of around 1 nH at 24 GHz. Measured S-parameters of the inductor were used in the design for simulation.

When the input signal is large enough, the transistor pair operates similar to a full-wave rectifier. The current that flows through the load will repeat every half of the period of the input signal, which generates then a large signal at twice the fundamental frequency at the emitter node. When the input signal is 180 degrees out of phase, the fundamental frequency components add destructively and cancel at the emitter node. If the input is not exactly 180 degrees out of phase, a leakage of the fundamental frequency at the output will appear.

At very low input power level, the conversion gain of the frequency doubler increases as the input power increases.

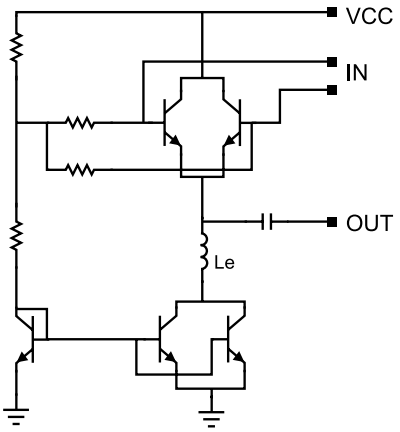

Fig. 2. Schematic of the push-push frequency doubler.

The maximum conversion gain of -4.5 dB is reached with a 30 GHz input signal of 3 dBm. The conversion gain starts to drop slowly when the input power is further increased. Due to the high supply voltage (4V), the saturated output power of the frequency doubler at 60 GHz is around 5 dBm with a 15 dBm input power level. However, in this work, the maximum power that can be delivered to the frequency doubler is around 7 dBm, generated by the fundamental VCO, with one output left open. With the input power fixed, the conversion gain drops slowly as the input frequency increases. Fig. 3 shows the simulated output power when the input frequency is swept from 1 GHz to 45 GHz, with an input power level of 7 dBm. It can be seen that the frequency doubler has a very wide operational bandwidth. The output power only drops by around 7 dB for output frequencies from 30 GHz to 90 GHz.

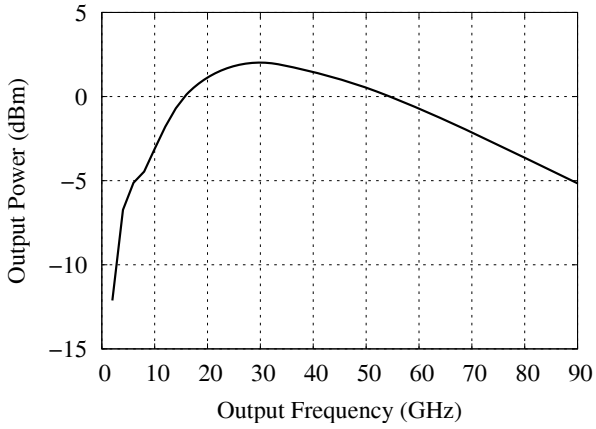

Fig. 3. Simulated output power at different output frequency with 7 dBm input power.

C. Final VCO

The final design combines the fundamental VCO and the frequency doubler on one chip, while both subcircuits were also realized separately for testing purposes. One output of the fundamental VCO was connected to the input of the frequency doubler while the other output was reserved for output at the fundamental frequency. Fig. 4 shows the micrograph of the fabricated chip. The TFMLs were folded and the circuit is still quite compact, with a size of only 1130 $\times$ 670 μm^2 including the pads.

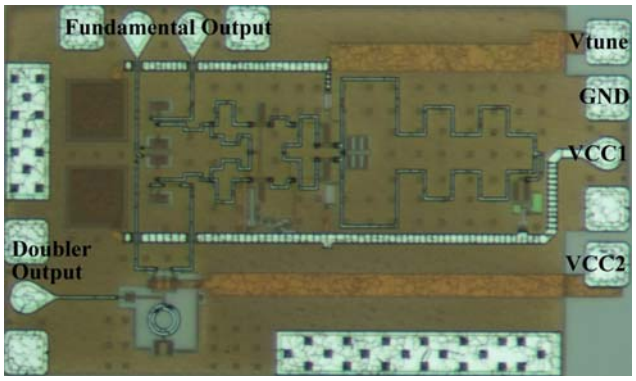

Fig. 4. Micrograph of the final VCO. The chip size 1130 $\times$ 670 μm^2 including pads.

IV. Measurement Results

The VCO was characterized on wafer. A PGPGP (power-ground-power-ground-power) DC wedge was used to supply the DC voltages. The output was connected through a 110 GHz GSG probe, a 1 mm cable and a coaxial to waveguide adapter to an Agilent V-band mixer (Agilent 11970V), which is used to extend the frequency range of the spectrum analyzer (Agilent 8565E). The V-band mixer is specified only for frequencies from 50 to 75 GHz. Frequencies above 75 GHz were measured using the same setup, with an estimated conversion loss of the mixer. To test the highest output power at the frequency-doubled output, the fundamental output was first left open in order to deliver the maximum input power to the frequency doubler. Fig. 5 shows the measured output power and frequency.

The frequency is continuously tunable from 64 GHz to 86 GHz. A maximum output power of -3.4 dBm was measured at 79 GHz. At lower frequencies, the output power decreases because of a decrease in the fundamental oscillator output power for low V_{tune}. The output power drops slightly faster than the simulation at higher frequencies. The reason for this needs to be further investigated. It should be noted that the measurement setup has an error margin of $\pm$ 1 dB, considering the estimated conversion loss of the V-band mixer above 75 GHz and the losses of the probe, coaxial to waveguide adapter and cable.

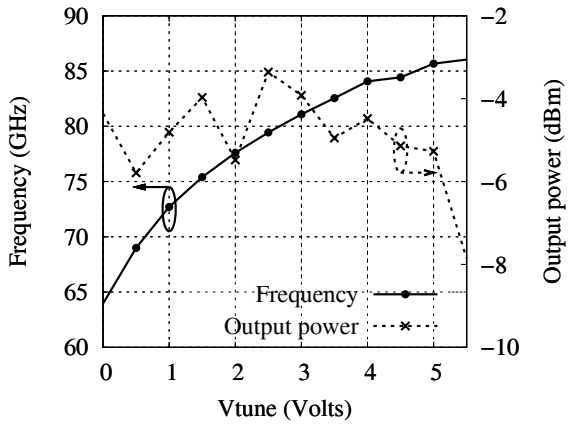

Fig. 5. Measured output power and frequency of the final VCO, with the second fundamental output left open.

It is difficult to measure the phase noise accurately by on wafer measurements, since the spectrum is influenced by low-frequency noise coupled into the DC supply connected to the tuning pad. The phase noise of the VCO without tuning voltage was measured at 81.5 GHz carrier frequency to be -83 dBc/Hz at 1 MHz offset.

By increasing the supply voltage of the fundamental VCO to 6.5V, the circuit can produce -4.5 dBm output power at 87.1 GHz. Fig. 6 shows the measured output spectrum at 87.1 GHz. 4 dB should be added for the loss of probe, adapter and cable.

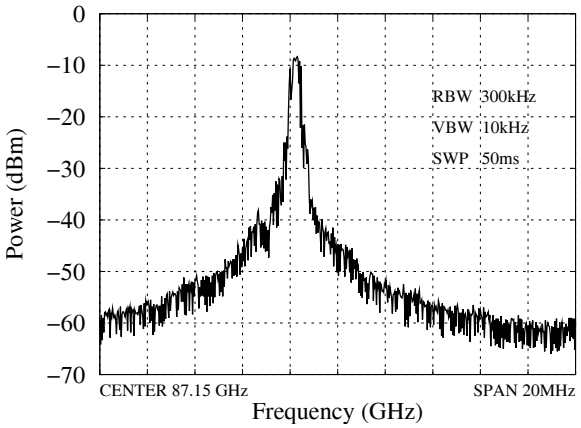

Fig. 6. Measured spectrum of the VCO at 87.1 GHz.

In a second step, the fundamental output was connected through a 40 GHz GSSG probe to another spectrum analyzer, so both the fundamental and the doubled frequency can be monitored. Since the fundamental output is differential, the other output was terminated with a 50Ω load. Fig. 7 shows the measurement results.

It can be seen that the fundamental output delivers a power of around 4 dBm above 40 GHz. At lower

frequencies, the power decreases slowly because the output matching deteriorates as the frequency decreases. Loading of the fundamental output also decreases the input power delivered to the frequency doubler, which then results in a drop of the output power at the doubler output. The power level of the fundamental output is quite sufficient to drive a divide by 32 frequency divider and an external phase locked loop can be built to stabilize the frequency.

The fundamental VCO consumes 45 mA at a 5.5 V supply while the doubler consumes 17 mA at 4 V. The voltage supply of the fundamental VCO can be redesigned for 4V supply with similar current consumption and output power.

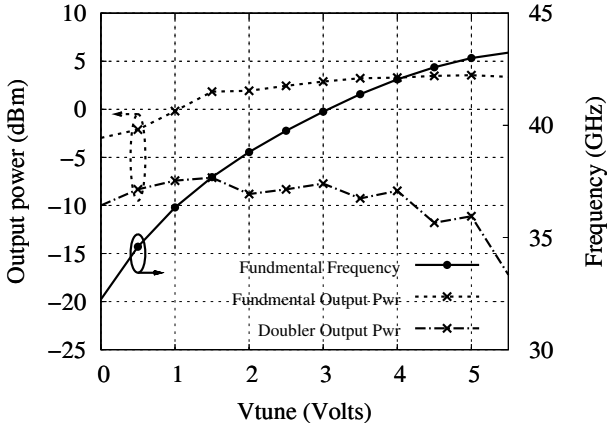

Fig. 7. Measured output power of the fundamental and double-frequency output.

As described in Section III-B, a common-mode component of the input signals will result in an incomplete suppression of the fundamental component at the output. Since the fundamental VCO has two differential outputs, asymmetries, like intersecting lines, are unavoidable, which then cause a phase deviation at the fundamental output. When the fundamental output of the VCO was left open, a -7 dBm leakage of the fundamental frequencies at the output was measured. Compared with the input power (around 7 dBm), the suppression of the fundamental frequency by the frequency doubler is around 14 dB. Because the fundamental frequency is quite well separated from the output frequency, it can be easily filtered out by using external filters.

V. Conclusion

A fully integrated frequency generation IC consisting of a fundamental voltage controlled oscillator and a frequency doubler was designed and characterized. The circuit achieves a wide tuning range of more than 22 GHz, centered at 75 GHz with relatively high output power, sufficient to drive an active mixer. It reaches a highest oscillation frequency of 87.1 GHz with -4.5 dBm output power, although the circuit is designed using a 0.8 μm SiGe HBT technology with f_T and f_{max} of only 80 and 90 GHz, respectively. A phase noise of -83 dBc/Hz was measured at 1 MHz offset (tuning voltage left open). A simultaneous differential output at the fundamental frequency is also provided for phase locked loop purpose. Together with an existing Gilbert cell mixer in the same technology, the use of this low-cost technology for 60 GHz down-converters can thus be successfully demonstrated.

Acknowledgment

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