Low Noise Amplification at 0.67 THz Using 30 nm InP HEMTs

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***Abstract*—In this letter, low noise amplification at 0.67 THz is demonstrated for the first time. A packaged InP High Electron Mobility Transistor (HEMT) amplifier is reported to achieve a noise figure of 13 dB with an associated gain greater than 7 dB at 670 GHz using a high f_{MAX} InP HEMT transistors in a 5 stage coplanar waveguide integrated circuit. A 10-stage version is also reported to reach a peak gain of 30 dB. These results indicate that InP HEMT integrated circuits can be useful at frequencies approaching a terahertz.**

***Index Terms*—Coplanar waveguide (CPW), high electron mobility transistor (HEMT), low noise amplifier (LNA), millimeter-wave (MM-Wave), monolithic microwave integrated circuit (MMIC), sub-millimeter wave.**

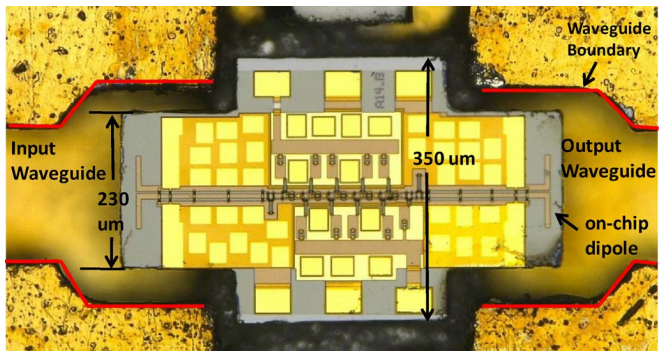

Fig. 1. Microphotograph of 670 GHz LNA in split block housing.

I. Introduction

In the last few years, the development of Terahertz f_{MAX} transistor technologies [1] has pushed operating frequencies of amplifiers well into the sub-millimeter wave range. The first demonstrations of sub-millimeter amplification were undertaken at the 340 GHz atmospheric window using InP HEMT [2] and MHEMT [3] technologies. Amplification has now been demonstrated above 500 GHz with a cascode amplifier reported in [4], which reached a packaged gain of 10 dB at 550 GHz. In this letter, the operating range is pushed to 670 GHz. We report a packaged low noise amplifier (LNA) with peak gain of 8 dB and noise figure (NF) 13 dB (5500 K) for a 5 stage amplifier, and a second 10-stage amplifier with a peak measured gain of 30 dB. Note that GaAs double side band (DSB) Schottky mixers have recently been reported at 520–590 GHz demonstrated a 3000–4000 K noise temperature [5] at room temperature. In a Single Side Band (SSB) application, the reported InP LNA would therefore provide competitive performance to a GaAs Schottky receiver at this frequency range.

A microphotograph of the five stage amplifier in split-block waveguide housing is shown in Fig. 1 with the signal electromagnetically coupled from the waveguide to the amplifier die, thus avoiding RF wirebonds. The basic concept

is described in [6], but modifications have been made to the structure to accommodate the wider electrical length necessary to accommodate dc biasing circuitry bonded at the top and bottom of the circuit. In particular, sections of InP substrate have been removed at the corners of the substrate to prevent overmoding in the waveguide cavity containing the on-chip dipole used to couple the signal to the integrated circuit.

II. THz InP HEMT Technology

Critical for realizing amplifiers at the target design frequency of 0.67 THz is a transistor with sufficiently high gain at the design frequency. To achieve the target operating frequency, we use an InP HEMT epitaxial profile with a composite InGaAs/InAs channel and a 30 nm Electron Beam Lithography (EBL) gate process. The device is then passivated with SiN. This process has produced InP HEMTs with greater than 2300 mS/mm transconductance, maximum channel current above 900 mA/mm, MAG/MSG values as high as 14.5 dB at 110 GHz and f_{MAX} of 1.2 THz and $f_T > 0.6$ THz. The MMIC process [1] employs two metal interconnection layers with a second layer airbridge, precision thin film resistors and MIM capacitors. The 3 in InP wafers are thinned to 25 micron thickness and grounding slot vias are reactive ion etched with a plated Ti/Au back metal.

III. Five Stage Packaged LNA

A variety of challenges exist with designing amplifiers at frequencies described in this letter. In addition to the requirement for an extremely high f_{MAX} transistor, the short wavelength and high conductor losses at these frequencies give the requirement that dimensions must be both physically and electrically compact. This requires scaled photolithographic processes, which must be well controlled to allow predicable and repeatable circuit features (trace and airbridge geometries and substrate etch features). Due to the extremely small feature size of these chips,

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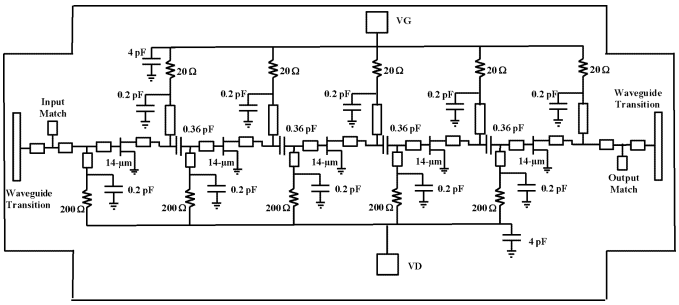

Fig. 2. Schematic of five-stage LNA. Rectangles indicate CPW transmission lines used for matching.

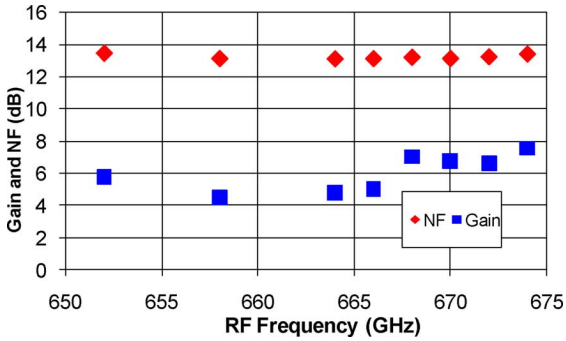

Fig. 3. Measured NF and gain for packaged amplifier.

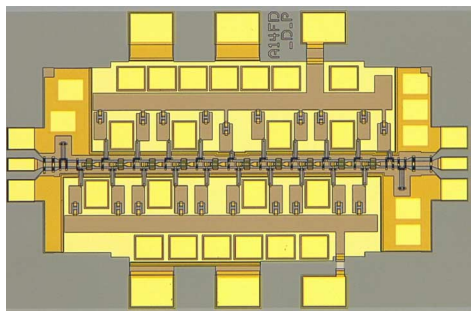

Fig. 4. Microphotograph of 10-Stage 670 GHz LNA.

we have begun to refer to them as "TMICs," or Terahertz Monolithic Integrated Circuits. A second challenge is in the area of transistor modeling, where it is necessary to extract model parameters at relatively low frequencies (< 110 GHz) and then extrapolate performance upwards in frequency to predict circuit response. In general, our design approach has been to scale all possible dimensions with wavelength. This has allowed many of the same design techniques and coplanar waveguide models to be used in the designs. However, significant attention is placed on tolerance and yield implications of aggressive scaling.

Referring to the microphotograph shown in Fig. 1, the TMIC occupies a total die area of $655 \times 375\ \mu\mathrm{m}^2$. The real estate occupied by the top and bottom dc biasing pads and required standoffs is a total of 140 μm of the total 375 μm chip height. This is necessary to accommodate 0.7 mil bondwires at the dc pads. The basic transition has been described in [6]. Note that the corners of the chip are etched to make the regions containing the electromagnetic transitions narrow enough to cut off higher order modes. A wall of vias is used at the input and output of the electromagnetic transition to prevent energy from coupling to the InP substrate.

The amplifier portion of the TMIC is implemented in grounded coplanar waveguide. Referring to the microphotograph in Fig. 1 and the schematic shown in Fig. 2, shunt open-circuited stubs are used for input and output matching. Due to the small capacitance and inductance of the frequency scaled 14 μm transistors, both the input and output load match are relatively well behaved at 670 GHz and lie close to the 50 ohm admittance circle and only a simple shunt connected CPW transmission line necessary for an optimal gain math. Most series CPW transmission lines are less than 5 μm long, and no shunt transmission line is longer than 20 μm long. In Fig. 1, the LNA is centered in the chip. This adds a loss of approximately 0.7 dB due to the coplanar waveguide, which will degrade the NF. We have adjusted this in a later chip revision and expect improved performance in the future when measurements are performed. A 0.2 pF bypass capacitor is used, followed by resistors at the gate and drain.

NF of the packaged amplifier has measured at NASA's Jet Propulsion Laboratory using a down-converting mixer and a horn antenna with absorbing material as load and liquid nitrogen for hot and cold measurements using the Y-factor method. The results are shown in Fig. 3. A minimum NF of 13 dB is obtained with an associated gain of 7–8 dB. The gain measured in this method is comparable to that obtained in S-Parameter measurements. Note that a significant amount of loss is incurred from the package at this frequency, with a total of ~ 4 dB loss estimated from measuring the package with coplanar waveguide through lines and then subtracting the coplanar waveguide losses. This gives a chip gain of 11-12 dB, which is 2.2–2.4 dB/stage of realized transistor gain.

IV. Ten Stage LNA

The results in the prior section were based on an initial design iteration at 670 GHz. The results indicated that the high WR1.5 waveguide loss and on-chip CPW losses means that high TMIC gain is essential for setting the module NF, and that all CPW excess transmission line lengths must be minimized. The second iteration TMIC shown in Fig. 4 is the result of these observations. The number of gain stages has been increased to ten, which both eliminates the input and output coplanar waveguide losses as well as doubling the total number of gain stages. The design process is similar; with the exception that a transistor model based on 30 nm InP HEMT measurements was used for improved accuracy. Based on the initial packaged module results and simulation, $\sim$ 30 dB gain was expected on-chip at 670 GHz. Referring to Fig. 4 it is clear that all excess CPW transmission line length at the input and output have been eliminated. The chip size itself is unchanged and is fixed to accommodate the module blocks shown in Fig. 1.

One important aspect should be noted for the TMIC shown in the microphotograph. Ground-signal-ground pads are at the input and output instead of the integrated dipole transition. This allows on-wafer probing at the WR1.5 waveguide band for the first time when used with WR1.5 waveguide probes developed

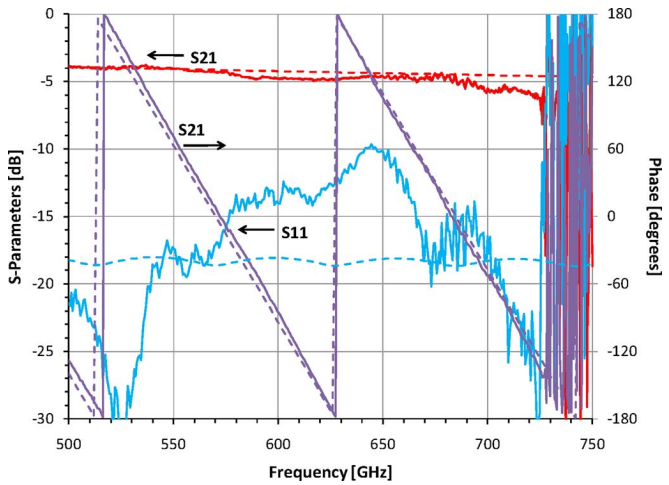

Fig. 5. Measured (solid) and simulated (dash) response of 1000 μm CPW line measured with on-wafer TRL calibration.

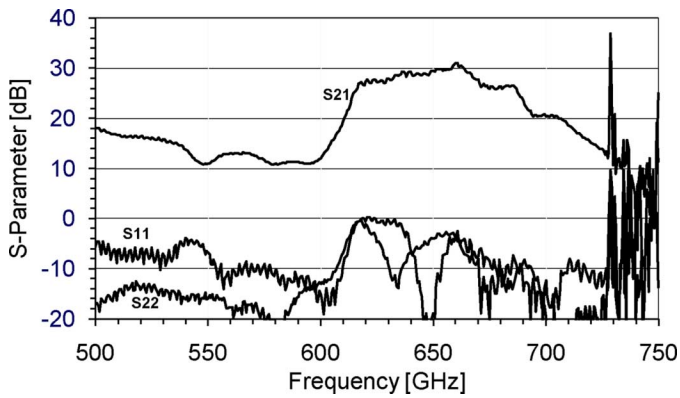

Fig. 6. Measured on-wafer S-Parameters of 10-stage LNA.

by the University of Virginia. These probes cover the entire WR1.5 waveguide band with an insertion loss of 7-8 dB for each probe at the center of the band. These probes are a scaled prototype of the probes presented in [7].

Full 2-Port S-Parameter measurements have been obtained on the packaged amplifier. This was done using a set of WR1.5 frequency extension modules developed by Virginia Diodes, Inc. The frequency extension modules were calibrated using an on-wafer TRL calibration for accurate probetip response. To demonstrate the usefulness of this technique, the measured response of a 1000 μm long CPW through line is shown after calibration in Fig. 5 as a calibration verification. The measured insertion loss of the probe is predicted within 1–2 dB to a frequency of approximately 700 GHz. Additionally, the phase response of the line also agrees well with measurement. At this time, no systematic accuracy measurements have been performed, but agreement is generally good and shows that on-wafer measurement techniques can be applied at frequencies approaching one terahertz. Note that the dynamic range of the test set falls off above 725 GHz, which results in the jagged response shown in the range above 725 GHz.

The measured S-Parameter data for the ten stage LNA is shown in Fig. 6. Peak gain of 30 dB is obtained at $\sim$ 660 GHz, which represents a realized amplifier gain of 3 dB/stage. The higher realized gain compared to the five stage amplifier is attributed to both improved transistor matching, and elimination of the CPW feedlines at the input and output which are visible in Fig. 1. Each of these improvements should lower the amplifier NF.

V. Conclusion

In this letter, a five-stage amplifier module and an iterated 10-stage design operating at 0.67 THz have been presented. The module demonstrates 7–8 dB packaged gain at 670 GHz and 13 dB NF. An iterated 10-stage shows 30 dB peak gain of 30 dB at 660 GHz measured on wafer, for a realized gain per stage of 3 dB. We project the high-gain design should show improved NF when packaged and fully characterized.

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