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SiGe HBT Technology Based on a 0.13-μm Process Featuring an f_{MAX} of 325 GHz

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ABSTRACT A self-aligned SiGe HBT technology achieving a cutoff frequency (f_T) of 253 GHz was developed using a selective SiGe epitaxial growth process. Germanium concentration in an i-SiGe layer just under a p^+ intrinsic base region was raised to 27.4% to improve f_T, and boron concentration in the intrinsic base region reached 2.4×10^{20} cm^{-3} as a deposition to maintain a breakdown voltage of 1.5 V. A 0.13-μm SiGe BiCMOS technology geometrically advanced from an earlier 0.18-μm version shrinks the emitter width from 0.2 to 0.12 μm to reduce collector-base capacitance and base resistance. It achieves a maximum oscillation frequency (f_{MAX}) of 325 GHz. This technology can be applied to optical and mm wave communication systems.

INDEX TERMS Bipolar junction transistors, SiGe HBT, SiGe selective epitaxial growth, LP-CVD, self-aligned structure.

I. INTRODUCTION

The device performance of Si-based bipolar transistors has been improved by the application of technologies such as double-polysilicon self-aligned structures and precious shallow diffusion layer formation techniques. The self-aligned structure is advantageous because it can determine the distance between different diffusion areas of transistors without the influence of lithography alignment, thus reducing both parasitic resistance and parasitic capacitance [1]–[5]. By applying an *in-situ* phosphorus doped poly-Si deposition technique to emitter electrodes, narrow and precious intrinsic base could be formed under the condition of small thermal budget for forming emitter layers in a Si substrate. Si-based bipolar transistors achieved a cutoff frequency (f_T) of over 40 GHz in the 1990s by applying a combination of low-energy accelerated BF_2 implantation and rapid thermal annealing (RTA) [4], and the introduction of a rapid vapor phase doping (RVD) process finally enabled an f_T of 100 GHz in a Si-based bipolar transistor [6], [7]. A selectively implanted pedestal collector (SIC) region just under the intrinsic base region has been proposed to improve the f_T by suppressing the increase of collector-base capacitance (C_{CB}) [5].

SiGe heterojunction bipolar transistor (HBT) technology, which emerged in the 2000s, has been extensively applied to high-speed communication systems. The original concept of HBT was conceived at an early stage of the development of bipolar junction transistors [8], [9], and SiGe HBT technologies have been rapidly developed to the production level by using ultra high vacuum-chemical vapor deposition (UHV-CVD) or low pressure-CVD (LP-CVD). The f_T performance of various devices has steadily increased from 100 GHz to 410 GHz [10]–[24]. These high speed HBTs have been applied to optical and mm wave communication systems.

Several techniques have been proposed to achieve optimal device performance. For example, a graded germanium profile has been used to produce accelerated electrical force driving minority carriers [10], and introducing a carbon doping technique into an intrinsic base region can suppress boron diffusion during emitter formation to maintain a shallow intrinsic base region [11], [12]. There are two approaches to forming a SiGe intrinsic base region [13]: blanket epitaxial growth over the entire area of a wafer and selective epitaxial growth (SEG) on only the Si and poly-Si layers. The SEG

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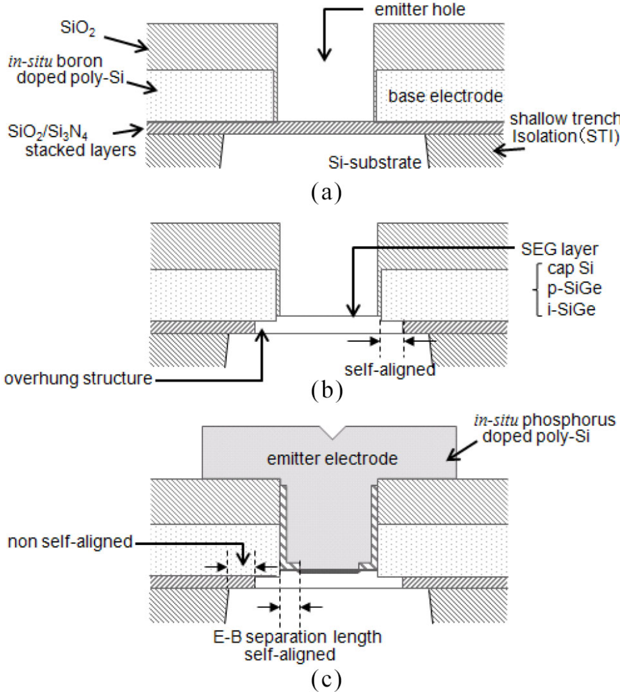


FIGURE 1. Process flow for making SiGe base region and emitter-base separation wall as self-aligned structure. (a) Emitter hole formation. (b) Selective SiGe epitaxial growth. (c) Emitter poly-Si formation.

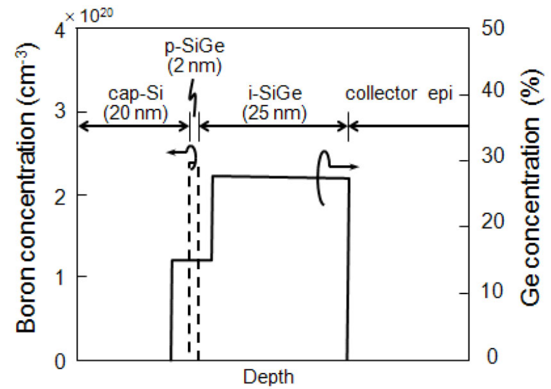


FIGURE 2. Schematics of boron and germanium profile in as-grown SiGe layer.

TABLE 1. Pattern dependency for p-SiGe epitaxial growth

Measurement pattern (epi growth area/wafer ratio)	Growth rate [nm/min]	Boron concentration [cm^{-3}]	Ge content [%]
Patterned wafer 400 µm × 400 µm (0.1 %)	7.4	9.7×10^{20}	10.3
Patterned wafer 400 µm × 400 µm	7.2	–	10.1
20 mm × 20 mm (1.3 %)	3.6	6.6×10^{19}	7.7
Bare Si wafer (100 %)	3.5	4.3×10^{19}	8.2

* 660 ºC, pressure=5 Torr,
SiH_2Cl_2=100 ml/min, HCl=0 ml/min, B_2H_6=10 ml/min, GeH_4=6.3 ml/min

approach has the advantage of enabling production of an almost perfect self-aligned structure without applying any complex additional processes [14]–[18]. When the blanket epitaxial growth is used for an intrinsic base region, selective boron- doped poly-Si growth has been applied to form a raised extension base layer which enables formation of a self-aligned structure [19]–[22].

The improved lithography technologies of the 0.13-μm node can improve the SiGe HBT performance by reducing parasitic regions, and common techniques such as shallow trench isolation and salicide formation, when applied to conventional CMOS process technologies, have reduced the parasitic resistance and capacitance of bipolar transistors [23], [24].

This paper focuses on how to improve the f_T and maximum oscillation frequency (f_{MAX}) of a self-aligned SiGe HBT using the SEG approach for forming an intrinsic base region. Section II details the selective SiGe epitaxial growth technology that is applied in Hitachi's SiGe HBT. The results showed germanium concentration affects the f_T and transistor yield. Section III describes the 0.13-μm technology and structure inventions used to reduce parasitic parameters and achieve an f_T of 253 GHz and an f_{MAX} of 325 GHz. We conclude the paper with a brief summary.

II. SELECTIVE SIGE EPI TECHNOLOGY

Hitachi's SiGe HBTs have been fabricated on a 200-mm Si(100) wafer. The first part of the HBT formation consists in the construction of a collector region with n^+ buried layer (NBL) implantation, 0.15-μm-thick non-doped Si epitaxial growth, shallow trench isolation and n^+ collector plug. The process to form a base region using a selective SiGe epitaxial growth technique is shown in Fig. 1. Stacked layers consisting of SiO_2/*in-situ* boron-doped poly-Si/Si_3N_4/SiO_2 layers are deposited. After the formation of an emitter hole by dry etching the stacked layers (Fig. 1(a)), a poly-Si overhung structure inside the emitter hole is formed by wet-etching the stacked SiO_2/Si_3N_4 layers and the SiGe layer is selectively grown on a clean Si substrate in the exposed emitter hole using a single-wafer LP-CVD system of Applied Materials Centura® Epi (Fig. 1(b)). HCl etching gas and 20 l/min H_2 blow are used to avoid the memory effect, which is residual boron contamination in the chamber. The SEG layer consists of three regions: an intrinsic SiGe (i-SiGe) layer grown with SiH_2Cl_2 and GeH_4 as source gases, a boron-doped SiGe (p-SiGe) layer grown by adding B_2H_6 as dopant gas, and a cap intrinsic silicon (cap Si) layer. The 2-nm-thick

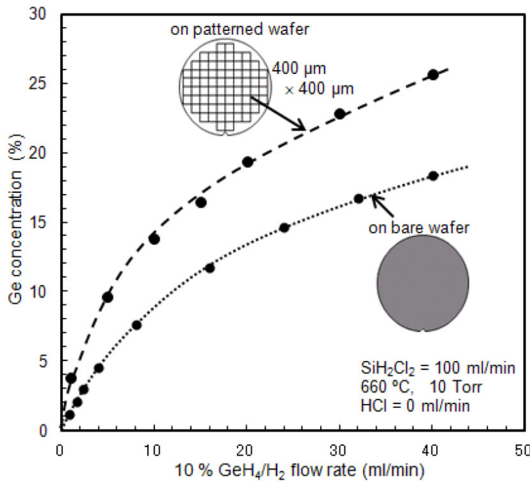


FIGURE 3. Germanium concentration dependency for GeH_4 flow rate.

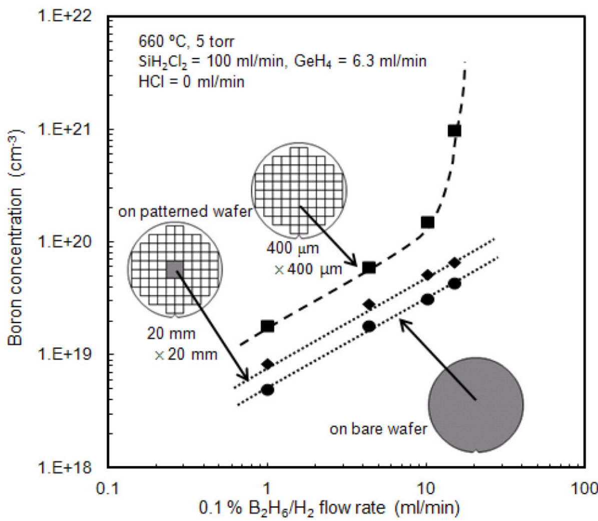


FIGURE 4. Boron concentration dependency for B_2H_6 flow rate.

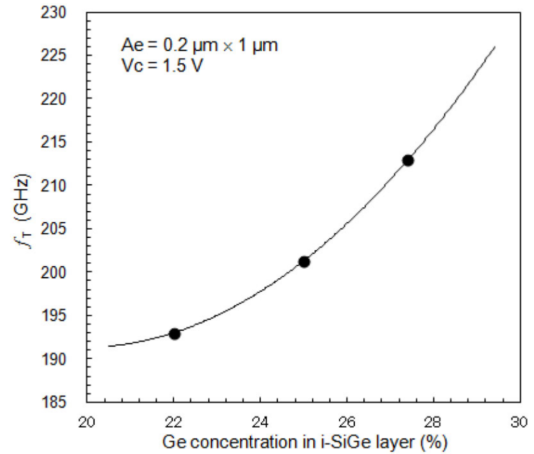


FIGURE 5. Cutoff frequency with various germanium concentrations of i-SiGe layers. The thickness of the i-SiGe layers is 18 nm. Other conditions of the SEG layers and SIC implantations are the same. Emitter area size (Ae) is 0.2 × 1 μm.

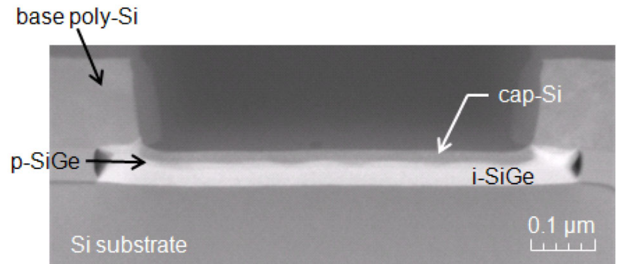


FIGURE 6. Cross sectional TEM of SiGe epitaxial growth layer with 22% Ge content. The thickness of the i-SiGe layer is 26 nm. HCl gas flow is 10 ml/min. Process pressure to form i-SiGe layer is 3 Torr.

p-SiGe layer includes 2.4×10^{20} cm^{-3} boron concentration and 0.1–0.2 % carbon imposed by 1 % CH_3SiH_3/H_2 of 5–10 ml/min gas flow. The SiGe layers and the Si layer are grown at 660–670 °C and at 740 °C, respectively. It has previously been reported that bandgap grading produced by a graded germanium profile in the base region induces drift electric field, which aids minority carrier transport through the base region, so we chose a step-shape germanium profile (Fig. 2) [14]. This germanium profile, which increases from 10-15 % in the p-SiGe layer of the intrinsic base region to 22-30 % in the i-SiGe layer, is formed to generate a drift electric field resulting in higher frequency operation as well as the graded germanium profile. A step-shape germanium profile is easy to monitor at the production phase. The SIC region was formed by two phosphorus implantation steps: after the emitter hole opening (Fig. 1(a)) and after the selective SiGe epitaxial growth (Fig. 1(b)). Phosphorus ions of 3×10^{13} cm^{-2} were implanted through the stacked SiO_2/Si_3N_4 layers with an acceleration energy of 200 keV for the first SIC implantation step, and those of 1×10^{13} cm^{-2} were implanted with that of 60 keV for the second SIC implantation step.

An emitter-base separation wall is fabricated as the self-aligned structure, and an emitter electrode using an *in-situ* phosphorus-doped poly-Si layer is formed (Fig. 1(c)). Final high temperature spike annealing at 1000 °C is used to activate and diffuse impurities from the *in-situ* phosphorus-doped poly-Si into the cap Si layer to form the HBT's emitter regions. Phosphorus concentration in the emitter poly-Si layer was 4.5×10^{20} cm^{-3}. Cobalt silicidation is then simultaneously performed on the MOSFETs, HBTs, and contact areas of the poly-Si resistors.

In this work, the Si/SiGe layer thickness is evaluated through cross sectional SEM/TEM and spectroscopic ellipsometry (NanoSpec® 9300, Nanometrics Inc.). Carbon concentration is measured by secondary ion mass spectrometry (SIMS). Germanium concentration is evaluated by SIMS and by spectroscopic ellipsometry, and the boron concentration is directly measured by SIMS and indirectly by measuring the sheet resistance, which is evaluated using a four-probe van der Pauw pattern. The size of the emitter hole on a 0.2 μm × 1 μm emitter is 0.35 μm × 1.35 μm.

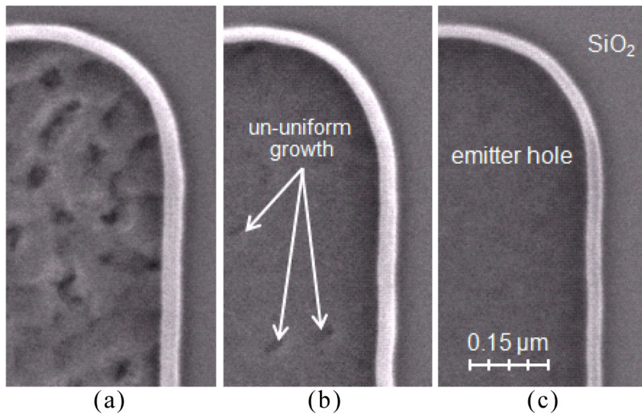


FIGURE 7. Plane-view SEM inside emitter hole after SiGe epitaxial growth. The average thickness and Ge concentration of the i-SiGe layer are 30 nm and 23%, respectively. HCl flow rate is (a) 20 ml/min, (b) 10 ml/min, and (c) 0 ml/min.

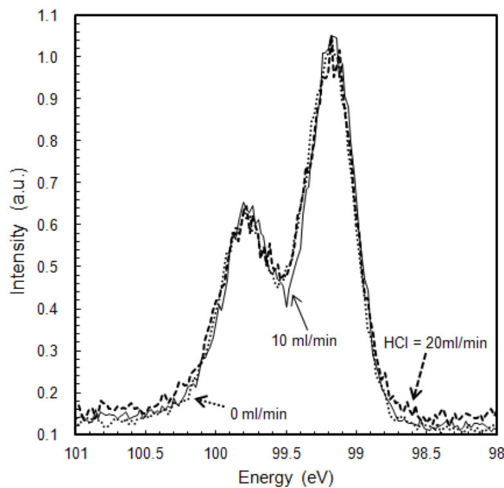


FIGURE 8. Si–Si bonding strength measured by x-ray photoelectron spectroscopy (XPS). Measurement area size is 400 × 400 μm.

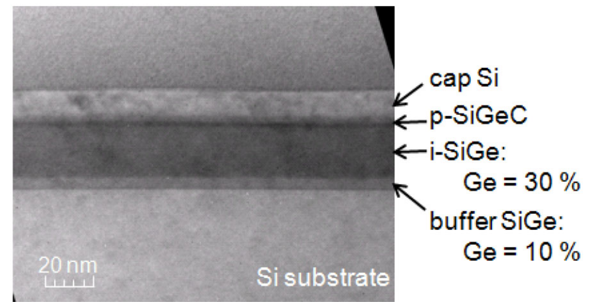


FIGURE 9. Cross sectional TEM of the intrinsic base region of a SiGe HBT with 30% Ge in the i-SiGe layer adding a i-SiGe buffer layer of 10% Ge content. HCl etching gas was not used to form this sample.

This is too small to be evaluated by SIMS or spectroscopic ellipsometry, so a 400-μm square open area in a test element group (TEG) chip is used to evaluate the SiGe layers. The ratio of the exposed emitter hole area on the wafer is less than 0.1 %.

Table 1 shows the evaluation results of the growth rate and impurity concentration of the p-SiGe layers formed under the SEG condition without HCl. The flow rates of SiH_2Cl_2, B_2H_6, and GeH_4 were 100 ml/min, 10 ml/min, and 6.3 ml/min, respectively. Pressure was 5 Torr and process temperature was 660 °C. Pattern dependency was observed within the same processing period, and the growth rate on the bare Si wafer without any oxide layer was half that on the 400-μm square open area. Boron and germanium concentrations on the bare Si wafer were also half that on the 400-μm square open area. A comparison on the same wafer showed that a chip-size open Si area (20 mm × 20 mm) had almost the same growth rate as that on the bare Si wafer and did not affect the growth rate and germanium concentration on the device area. Figs. 3 and 4 show the germanium concentration dependency for the GeH_4 flow rate and the boron concentration dependency for the B_2H_6 flow rate. Both results had the same tendency shown in Table 1, and the 400-μm square open area on the patterned wafer always had higher germanium and boron concentrations. The GeH_4 and B_2H_6 flow rates were lower than the SiH_2Cl_2 flow rate, and the mean free paths of the boron and germanium atoms were two to three digits shorter than the distance in the chip-size open area. Supply limited reaction for boron and germanium doping can happen while Si atoms are maintaining the surface reaction control, which lowers the boron and germanium concentrations in the chip size open area. On the other hand, germanium and boron atoms can reach inside the 400-μm square open area from the outside area covered by oxide. Lower impurity concentration in the chip size open area induced the lower growth rate, as shown in Table 1.

When the B_2H_6 flow rate increased beyond 10 ml/min, boron concentration in the 400-μm square open area rapidly increased. A previous paper reported that a too high B_2H_6 flow rate over 30 ml/min induces roughening of the growth surface [25]. Chip size open areas were used to evaluate the boron concentration of the SiGe layer in that study [25], in which unexpectedly high boron concentration was induced and lattice mismatch due to too much boron resulted in the deterioration of the epitaxial layers. It was demonstrated in the present work that a 1×10^{21} cm^{-3} boron concentration in a device size Si area can be realized without any deterioration of the SEG layers.

When we used the process pressure of 5–10 Torr, no size dependency of the growth rate and impurity profiles from area sizes of 0.35 μm × 1.35 μm to 400 μm × 400 μm was observed in the cross sectional TEM and sheet resistance measurements. Germanium concentration on a small Si area (20 μm × 20 μm) measured by a micro auger probe showed no obvious difference beyond measurement error width. The SiGe growth rate was almost completely constant among emitters with different hole sizes, and no local loading effect at different hole sizes smaller than a 400-μm square area was observed.

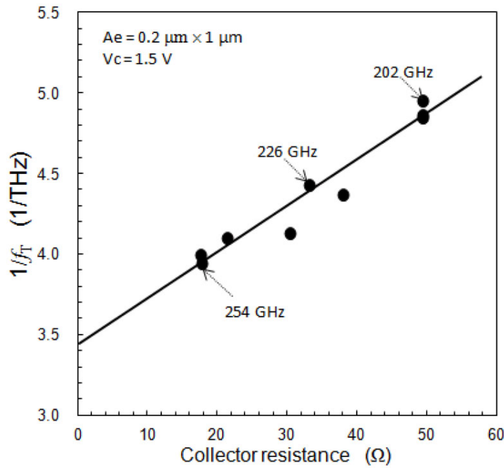


FIGURE 10. Relation between cutoff frequency and collector resistance on the same chip.

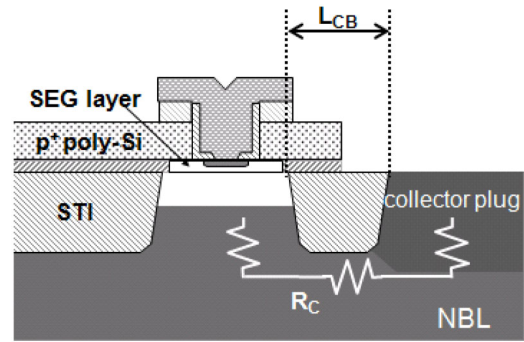


FIGURE 11. Schematic cross section of the SiGe HBT.

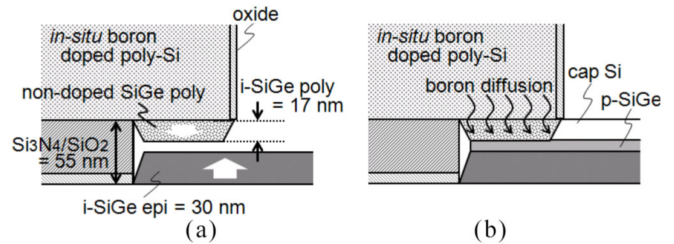


FIGURE 12. Schematic flow of selective SiGe epitaxial growth in a cavity (a) after growth of the i-SiGe layer and (b) after completion of the SEG processing step.

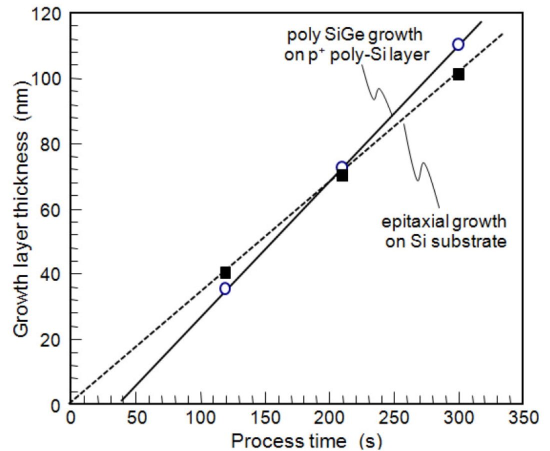


FIGURE 13. Comparison of SiGe-epitaxial growth rate on Si substrate and SiGe-poly growth rate on p^{+} poly-SiGe layer.

Fig. 5 shows the f_T measurement results with various germanium concentrations of the i-SiGe layer. Other fabrication conditions of the cap Si and p-SiGe layers were the same. Results showed that, with the SiGe HBT, the higher germanium concentration improved the f_T from 192 GHz to 213 GHz, and the same 1.5 V breakdown voltage between emitter and collector (BVceo) was maintained. When the germanium concentration in the p-SiGe layer was increased from 10 % to 15 %, the BV_{CEO} was reduced by 0.2 V. The germanium concentration in the p-SiGe layer directly affected the built-in potential between the emitter and the base, but the germanium concentration in the i-SiGe layer did not suppress the barrier potential. Even the step-shape germanium profile could produce a strong drift electric field and improve the f_T just as well as the graded germanium profile. However, heavy germanium concentration on the Si substrate was limited due to strain generated by the 4 % lattice mismatch between Ge and Si [27]–[29]. Layer-by-layer hetero epitaxial growth on a Si substrate initially occurred, but increasing the SiGe layer thickness increased the deformation energy inside the SiGe epitaxial layer due to a misfit between Ge and Si, and island-like (3-D) growth started reducing the deformation energy, as shown in the cross sectional TEM in Fig. 6.

HCl gas flow induced the deterioration of the SiGe epitaxial growth layer, as shown in Fig. 7. This phenomenon did not change among the various hole sizes from 0.35 μm × 1.35 μm to 400 μm × 400 μm. The 10 ml/min HCl gas flow deteriorated the SiGe surface even under the condition of 23 % germanium concentration. No poly-Si like structure or misfit dislocation was observed from the plane and cross sectional TEM (Fig. 6) in the deteriorated i-SiGe layer, which means that no strong stress beyond the critical condition was induced during SiGe epitaxial growth. The Si-Si bonding strengths were measured at different HCl gas flow rates (Fig. 8), with the results indicating that the SEG layer with the deteriorated surface (Fig. 7(a) and (b)) had the same intensity of Si-Si bonding as that with the smooth surface (Fig. 7(c)). Chlorine atoms were not detected from the SiGe growth layer by SIMS, which means that such atoms did not directly induce lattice mismatch by getting into the SiGe layer. The 20-ml/min HCl gas flow rate did not deteriorate the SiGe growth layer at 15.9 % germanium concentration, meaning that the combination of chlorine and germanium atoms was what deteriorated the SiGe surface.

Adding a 5-nm-thick i-SiGe layer containing 10% Ge under a highly germanium contained i-SiGe layer resulted in an i-SiGe layer with a smooth surface, as shown in Fig. 9.

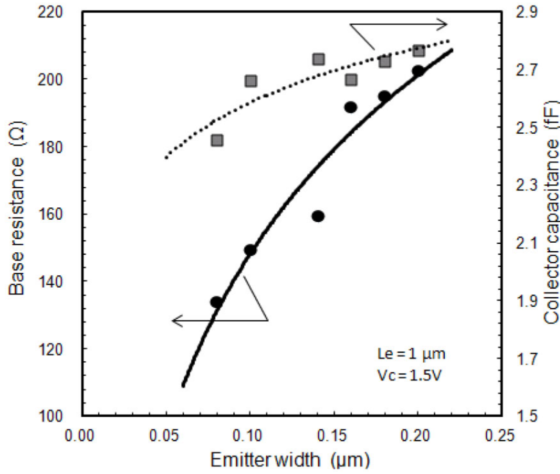


FIGURE 14. Emitter width dependency of parasitic parameters of the SiGe HBT. f_T= 227 GHz. Emitter length is 1.0 μm.

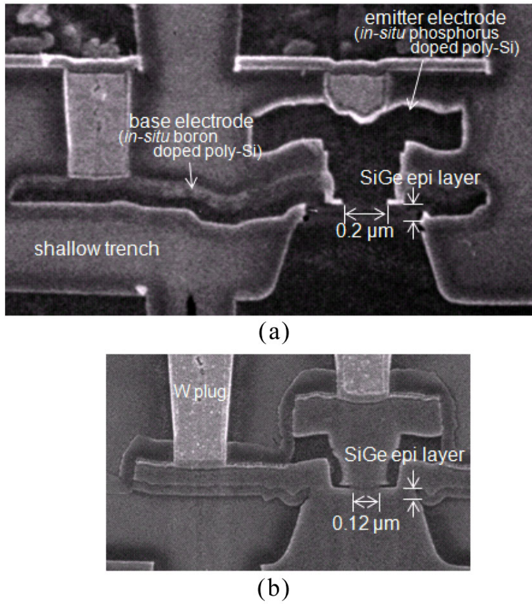
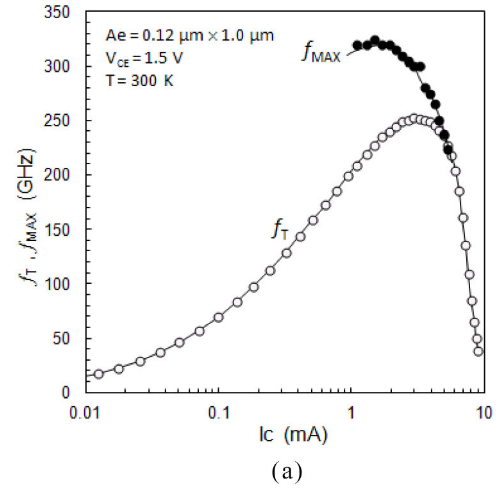


FIGURE 15. SEM cross sections of (a) a 0.18-μm based SiGe HBT and (b) a 0.13-μm based SiGe HBT.

The additional 10% germanium layer functioned as a buffer layer and eased the strained force in the highly germanium contained layer. Germanium concentration of 30% in the 20-nm-thick i-SiGe layer could be formed without any deterioration, indicating that strain due to lattice mismatch induced the surface deterioration of the i-SiGe layers. The island-like growth can be linked to the strain release action from the Si-Ge mismatch [27], and chlorine or HCl desorption from the growing surface limited the SiGe epitaxial growth rate at the low temperature of 660°C [25] in the case of the HCl addition. This indicates that chlorine atoms played some part in the roughening of the highly germanium contained growth layer on the Si surface, but we could not clarify if the addition of the HCl link increased the strain in the i-SiGe layer.



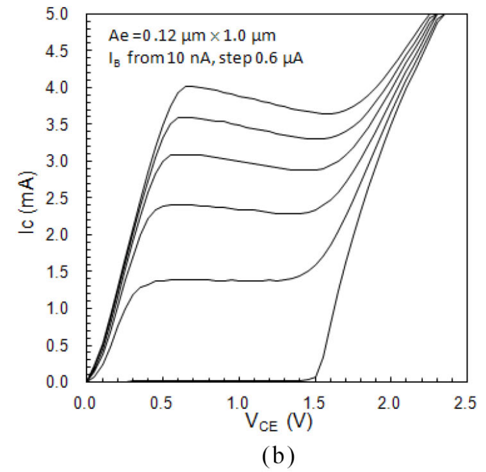


FIGURE 16. Measurement result of (a) f_T/f_{MAX}-collector current curve and (b) common-emitter output characteristics of the SiGe HBT.

A single device on the on-wafer two-port test element was measured for the RF evaluation. We used an HP8510C vector network analyzer up to 40 GHz, and the measurement system was calibrated by using the impedance standard substrate (ISS) of Cascade Microtech. The parameters of f_{MAX} and f_T were extracted from the Mason's power gain and the current gain (h_{21}) near 20 GHz with −20 dB/decade roll-off [19], [20].

III. REDUCTION OF PARASITICS

A. REDUCTION OF COLLECTOR RESISTANCE

Cutoff frequency f_T, which is largely determined by vertical transport parameters consisting of delay components in the emitter (τ_E), base (τ_B), and collector (τ_C, τ_{CSCL}) regions, can be described as

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_C + \tau_B + \tau_{CSCL}$$
$$= \frac{kT}{qI_c}C_{EB} + \left(\frac{kT}{qI_c} + R_C + R_E\right)C_{CB} + \gamma\frac{W_B^2}{D_n} + \frac{W_{CSCL}}{2v_{SAT}} \quad (1)$$

The base transit time can be reduced by thinning the base width and increasing the germanium concentration, as demonstrated by the experimental results in Fig. 5. Increasing the doping level of the SIC implantation shifts the onset of base widening to higher current densities. It also reduces the collector transit time.

Reducing the collector resistance can improve the f_T because it reduces the charging and discharging time of the collector-base capacitance (C_{CB}) [30]. The measurement results shown in Fig. 10, which were performed using (1), indicate that the collector resistance (R_C) is proportional to the inverse number of f_T. The collector resistance was extracted from the I_C against V_{CE} characteristics by taking the slope of the lines drawn. The collector resistance is varied by changing the length of the STI between the internal transistor and the collector plug, and the structure and layout invention to reduce the Rc improved the f_T by 45 GHz. Fig. 11 shows a schematic cross section of the SiGe HBT. The sheet resistance of the NBL formed by Sb ions implantation of 2×10^{15} cm^{-2} was 38 Ω/□ and that of a collector plug formed by phosphorus ions implantation of 5×10^{15} cm^{-2} was 20 Ω/□. Separation length of the STI dividing the collector plug and the intrinsic base region was shrunk to reduce the collector resistance (Rc) from 50 Ω in the case of a distance (L_{CB}) of 1.6 μm to 38 Ω in the case of 0.65 μm. The Rc can be reduced to 20 Ω by removing the 0.35-μm-deep STI region between the collector plug and the intrinsic base. A previous work [23] indicated that a steeper NBL profile is needed to increase the f_T to 200 GHz. Instead of applying a steep profile, we opted to remove the STI between the collector and the base to push up the f_T.

B. REDUCTION OF BASE RESISTANCE

In the self-aligned structure of Hitachi's SiGe HBT, the base poly-Si electrode makes contact with the intrinsic base region through the cavity under the base poly-Si at the processing step of SiGe selective epitaxial growth. This base contact cavity is formed by side-etching the SiO_2/Si_3N_4 stack layers using a solution of hot phosphoric acid. The schematic process flow of the p-SiGe layer between the i-SiGe poly grown from a base poly-Si and the i-SiGe layer grown from a Si substrate is shown in Fig. 12. The coverage of the epi-layers in this narrow 55-nm cavity is insufficient at the 10 Torr growth pressure in the LPCVD because the thickness of the i-SiGe layer in the cavity tends to be thinner than that outside the cavity. SEG layers are grown at a growth pressure of 10 Torr to become convex, so we used a pressure lower than 5 Torr to form a flat i-SiGe layer for making sufficient base contact [14].

The characteristics of the SEG help suppress base contact resistance. Fig. 13 shows the time dependency of SiGe growth thickness and the difference of incubation time on Si substrate/base poly-Si. The start point of SiGe-poly growth on boron-doped poly-Si was later than that of the SiGe-epi growth on the Si-substrate. This late incubation time suppressed the thickness of the poly-SiGe growth from the base electrode and resulted in a short distance of the link region that must be covered by boron diffusion.

A shallow emitter width by applying a fine 0.13-μm lithography technology can reduce base resistance. Fig. 14 shows the emitter width (W_E) dependency of the base resistance (R_B) and the collector-base capacitance (C_{CB}). The emitter length (L_E) was 1.0 μm. The W_E shrunk from 0.2 μm to 0.08 μm suppressed the base resistance by 35 % and the collector-base capacitance by 15%. Fig. 15 compares two generations of the SiGe HBTs of a 0.18-μm based HBT [14] and a 0.13-μm based SiGe HBT. The 0.13-μm SiGe HBT shown in Fig. 15(b) applied the 0.13-μm SiGe BiCMOS technologies geometrically enhanced from the previous 0.18-μm SiGe BiCMOS technology. Boron concentration reached the maximum level to suppress base resistance. Extrinsic base resistance could be reduced by applying a shallow emitter width and strengthening the base contact.

By reducing the collector resistance (Rc) by removing the STI between the internal transistor and the collector plug, and by including a higher 27.4 % germanium concentration in the i-SiGe layer, we were able to achieve an f_T of 253 GHz and a BV_{CEO} of 1.5 V (Fig. 16). A range for the current gain (h_{FE}) was from 1000 to 2500. Elimination of the STI between the internal transistor and the collector plug shall increase the C_{CB}, because the thickness of a dielectric oxide layer between a base poly-Si electrode and a collector region becomes thin. Increase of the C_{CB} was minimized by reducing the area size of a base poly-Si electrode. Suppression of the base resistance and collector-base capacitance improved the f_{MAX} to 325 GHz. The high performance HBT had no collector leakage or crystal defect problems. These results demonstrate that this technology has reached the production level for application to optical and mm wave communication systems.

IV. CONCLUSION

The device performance of Hitachi's SiGe HBT has been steadily improved from the previous 0.18-μm based device, which achieved an f_T of 201 GHz and an f_{MAX} of 227 GHz, to the current 0.13-μm based SiGe HBT, which achieves an f_T of 253 GHz and an f_{MAX} of 325 GHz. Germanium and boron concentrations in the SiGe SEG layers of a self-aligned HBT have been successfully increased with no surface deterioration during epitaxial growth under an HCl free condition. A high boron concentration of 2.4×10^{20} cm^{-3} and a high germanium concentration of 27.4 % were able to spontaneously realize an f_T of 253 GHz and a $BV_{CEO}$of 1.5 V. Combining the self- aligned structure and the 0.13-μm process based on the previous 0.18-μm process node suppressed the base resistance and collector-base capacitance to increase the f_{MAX} to 325 GHz. An even higher f_T can be expected in the future by increasing the germanium concentration to 30 % with a 10 % germanium buffer layer to suppress 3-D

crystal growth. This technology can continuously improve the performance of optical and mm wave communication systems due to the excellent production characteristics of the SiGe BiCMOS process.

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