SiGe HBT Technology with f_T/f_{max} of 300GHz/500GHz and 2.0 ps CML Gate Delay

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Abstract

A SiGe HBT technology featuring $f_T/f_{max}/BV_{CEO}$=300GHz/500GHz/1.6V and a minimum CML ring oscillator gate delay of 2.0 ps is presented. The speed-improvement compared to our previous SiGe HBT generations originates from lateral device scaling, a reduced thermal budget, and changes of the emitter and base composition, of the salicide resistance as well as of the low-doped collector formation.

Introduction

Still growing needs for faster data communication rates and new application areas up to 1 THz raise the question how far traditional semiconductor devices can satisfy these markets. The European project DOTFIVE addresses this challenge by striving towards SiGe HBTs with a maximum oscillation frequency f_{max} of 500 GHz, a value that exceeds the performance of best production technologies available at the project start in 2008 by about a factor of two. On this way, new device concepts and an aggressively scaled double-polysilicon technology facilitated a new record value for CML ring oscillator (RO) gate delays τ of 2.5 ps (1) and f_{max} values of 400-425 GHz (2), (3), (4). Based on these device capabilities, new levels of high-frequency circuit performance were realized with respect to power consumption (5), noise figure (6), complexity (7) or output power (8).

Here, we demonstrate further substantial progress of the high-speed performance of SiGe HBTs achieving the target level of the DOTFIVE project. The reported performance improvement of our HBT module with differential base epitaxy and self-aligned emitter base architecture (9) is based on lateral device scaling as well as modifications of the base profile, the annealing regime, the salicide sheet resistance, the emitter deposition, and the selectively implanted collector. Starting from the reference status of this technology (1st generation D51) with f_{max}/τ~300GHz/3.1ps, we describe the modifications led to an intermediate level (2nd generation D52) of f_{max}/τ~400GHz/2.5ps after the half period of DOTFIVE and finally to the current version D53 with f_{max}/τ~500GHz/2.0ps.

Device Fabrication

The basic HBT process flow was presented first in (9). General features of the device structure are sketched in Fig. 1. A recent version of this HBT module is implemented in our 0.13µm BiCMOS technology corresponding to the initial DOTFIVE generation D51 (10). The HBT development of this work is performed in our 0.25µm SG25H1 BiCMOS technology (11) environment, including shallow trench isolation, a deep-trench-free implanted collector well, a poly-resistor, 5 metal layers, and a 1fF/µm^2 MIM capacitor. The technological mod-

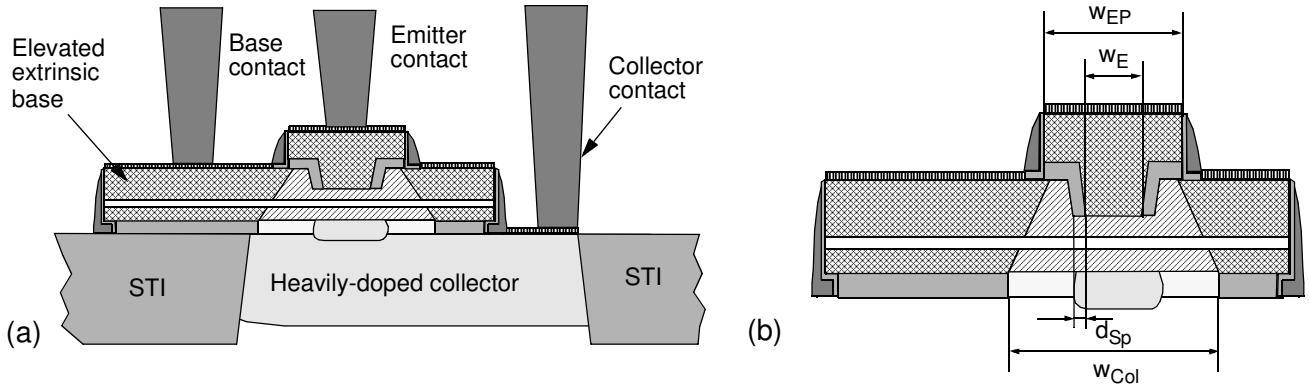

Fig. 1. Schematic cross section of the HBT under investigation (a) with key dimensions modified from generation to generation (b).

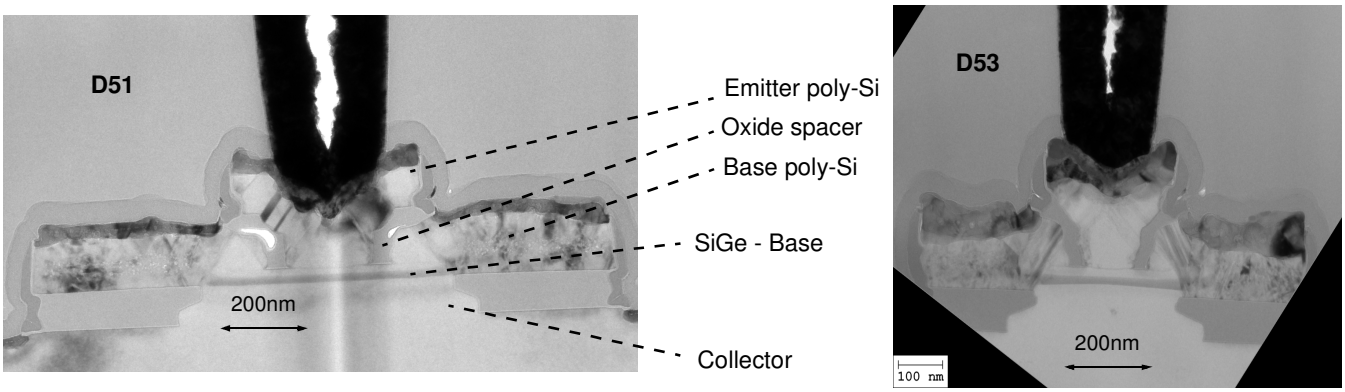

Fig. 2. TEM cross sections of the 1st (D51) and the 3rd (D53) HBT generation.

Table 1. Process changes for the 2nd (D52) and the 3rd (D53) process generation.

D51-> D52	Implications for device parameters	D52-> D53	Implications for device parameters
Modified base profile -> higher B dose -> higher Ge content	- Lower R_{SBi} - Higher base current density - Only minor change of I_C	SIC implantation before base epi -> thicker collector buffer -> higher SIC dose	- Lower R_{SBi} - Lower R_B - Reduced base width -Reduced Kirk effect
RTP spike temperature reduced	- Narrower base width	RTP spike temperature reduced	- Narrower base width
Salicide sheet resistance reduced	- Lower extrinsic base resistance	Smaller emitter-base spacer width	- Lower extrinsic base resistance
Higher emitter doping concentration	- Lower R_E		
Substrate rotated by 45°	~5% higher I_C in small HBTs, R_{SBi} unchanged		
Smaller emitter-base spacer width	- Lower extrinsic base resistance		

Table 2. Changed sizes of key HBT dimensions.

	D51 nm	D52 nm	D53 nm
Emitter window width w_E	180	160	120
Emitter poly width w_{EP}	460	375	290
Collector window width w_{Col}	560	510	310
Emitter-base spacer width d_{Sp}	45	35	30

ifications introduced for D52 and D53 are listed in Table 1 including the implications for the device parameters. For D52 and D53, the Ge content and the B dose of the SiGe:C base profile were increased in such a way that the collector current density was maintained while lowering the base sheet resistance. The final spike anneal was reduced from 1100°C to 1070°C for the migration to D52 and further to 1050°C for the D53 generation. Also the width of the emitter-base oxide spacer was scaled down from generation to generation by fine-tuning the combination of wet and dry etching applied to form the emitter-window inside-spacers. Moreover, the salicide sheet resistance was reduced by 50% and a higher emitter doping was established for D52 and D53. Additionally, the selectively-implanted collector (SIC) formation was changed in the D53 flow. Originally, it was implanted through the base layer after opening the emitter-window. Now, the SIC is implanted before base deposition applying the emitter-window layer. TEM pictures of our 1st and 3rd SiGe HBT generations document a significant scaling of important device dimensions (Fig. 2). For example, the emitter-window width was shrunken by about 33% and the width of the collector window by about 45%. Device dimensions relevant for the RF parameters are summarized in Table 2 for the different device generations.

RF Characterization

Because of the relevance for this work, we describe first the techniques used for the RF characterization. To extract the cut-off frequency f_T and the maximum oscillation frequency f_{max}, *s*-parameters were measured on wafer up to 110GHz (network analyzer 8510 XF). SOLT calibration with an impedance standard substrate (ISS) precedes the HF measurements. The quality of the extraction procedure for f_T and f_{max} is illustrated in Fig. 3. f_T and f_{max} extrapolated from the small-signal current gain h_{21} and the unilateral gain U, respectively, with -20 dB/frequency decade are plotted vs. the extrapolation frequency up to 110 GHz. The f_T, f_{max} values given in other diagrams are determined at 40 GHz. The circle fit of s_{11} for a device operating

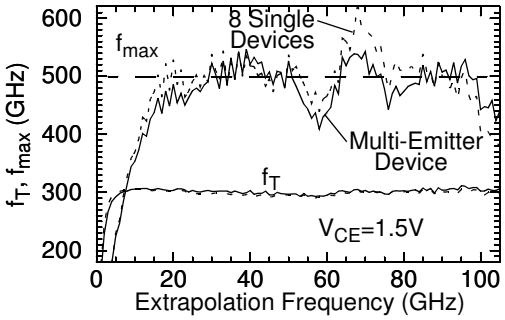

Fig. 3. Transit frequency f_T and maximum oscillation frequency f_{max} extrapolated from various frequency points with -20dB per frequency decade measured for 8 single emitter devices in parallel and a multi-emitter HBT with 8 emitters. Total effective emitter area for both is $8x(0.12x0.96)\mu m^2$. T=300K.

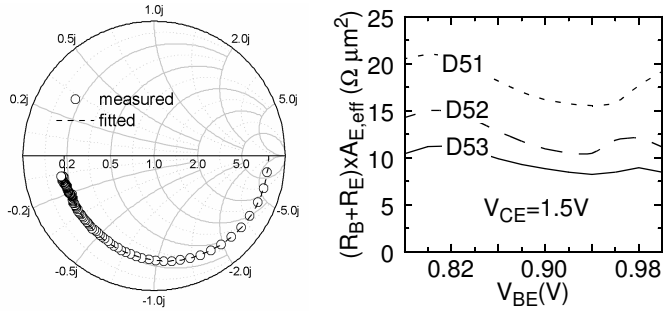

Fig. 4. Measured s_{11} at V_{BE}=0.92V from 1to 110GHz and circle fit plotted in a Smith chart for a 8-emitter device prepared in D53 (left). V_{BE} dependence of R_B+R_E extracted from s_{11} circle fit for the HBT generations D51-D53 (right).

at peak f_T is used to quantify R_B. An example including the bias dependence of R_B is presented in Fig. 4. Here, we do not subtract R_E because of missing standard measuring conditions. For the CML ring oscillator (RO) measurements, we used a configuration with 53 stages at 300mV voltage swing as in (12).

Device Results

For the HBT generations D51-D53, Gummel and output characteristics as well as $f_T(j_C)$ and $f_{max}(j_C)$ curves are shown in Fig.s 5, 6 and 7. In these graphs the current values are normalized to the effective emitter area $A_{E,eff}$ to facilitate an easy comparison. Device parameters in Table 3 indicate a continuous decrease of normalized C_{BC} and R_B values and an increase of f_T from D51-D53 explaining the improved f_{max} values and, partially, the reduced gate delays τ (Fig. 8). As can be seen in Fig. 7, for D53 the f_T and f_{max} decay and therefore the onset of the Kirk effect is shifted towards higher current densities. An enhanced dose of the selective collector implant (SIC) is responsible for this effect delivering an additional reduction of the minimum gate delay (Fig. 8). The new base profile with higher Ge content and lower R_{SBi} combined with a lower final spike anneal, introduced first in D52, affects positively not only R_B and f_T. It decreases the current gain due to a higher I_B resulting in a higher BV_{CEO} compared to D51. From D52 to D53 the process sequence of the SIC was rearranged (Table 1). Beside the further reduced RTP spike temperature, this change has contributed essentially to improve further R_B and f_T and consequently f_{max}. Due to the absence of a SIC implant through the base and slightly higher I_Cs, BV_{CEO} was lowered to 1.6V. The effect of only lateral scaling on f_{max} can be estimated from Table 3. It includes also data of HBTs fabricated in D53 using the relaxed layouts of D52 and D51. The data indicate that about 30% of the achieved f_{max} improvement can be attributed to device scaling while about 70% of the advance are due to the vertical doping profile and reduced specific resistances.

Conclusions

In conclusion, we have demonstrated that f_{max} values of 500GHz, f_T of 300GHz and gate delays of 2ps can be realized in a SiGe HBT technology. This performance demonstrates the potential of SiGe HBTs for arising applications such as sub-mm-wave imaging and ultra-high data rate communications.

Acknowledgment

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References

(1) A. Fox et al., "SiGe HBT module with 2.5ps gate delay," *IEDM Tech. Dig*., pp. 731-734, 2008.

(2) P. Chevalier et al. , "A conventional double-polysilicon FSA-SEG Si/SiGe:C HBT reaching 400GHz f_{max}," *Proc. BCTM,* pp.1-4, 2009.

(3) S. Van Huylenbroek et al., "A 400GHz f_{max} fully self-aligned SiGe:C HBT architecture," *Proc. BCTM*, pp. 5-8, 2009.

(4) T. Lacave et al., "Vertical profile optimization for +400GHz f_{max} Si/SiGe:C HBTs," *Proc. BCTM in press*, 2010.

(5) H. Knapp et al., "168GHz dynamic frequency divider in SiGe:C bipolar technology," *Proc. BCTM,* pp.190-193, 2009.

(6) E. Öjefors et al., "A 160GHz low-noise downconverter in a SiGe HBT technology," *EuMC in press*, 2010.

(7) U. R. Pfeiffer, E. Öjefors, and Y. Zhao, " A SiGe quadrature transemitter and receiver chipset for emerging high-frequency applications at 160GHz," *ISSCC Dig. Tech. Papers*, pp. 416-417, 2010.

(8) E. Öjefors, B. Heinemann, and U. R. Pfeiffer, "A 325GHz frequency multiplier chain in a SiGe HBT technology," *RFIC*, pp. 91-94, 2010.

(9) H. Rücker et al., "SiGe:C BiCMOS technology with 3.6 ps gate delay," *IEDM Tech. Dig*., pp. 121-124, 2003.

(10) H. Rücker et al., "A 0.13µm SiGe BiCMOS technology featuring f_T/f_{max} of 240/330GHz and gate delays below 3ps", *Proc. BCTM*, pp. 166-169, 2009.

(11) B. Heinemann, R. Barth, D. Knoll, H. Rücker, B. Tillack, and W. Winkler, "High-performance BiCMOS technologies without epitaxially-buried subcollectors and deep trenches," *Semicond. Sci. Technol.,* vol. 22, pp. 153-157, 2007.

(12) B. Heinemann et al., "A low-parasitic collector construction for high-speed SiGe:C HBTs," *IEDM Tech. Dig.*, pp. 251-254, 2004.

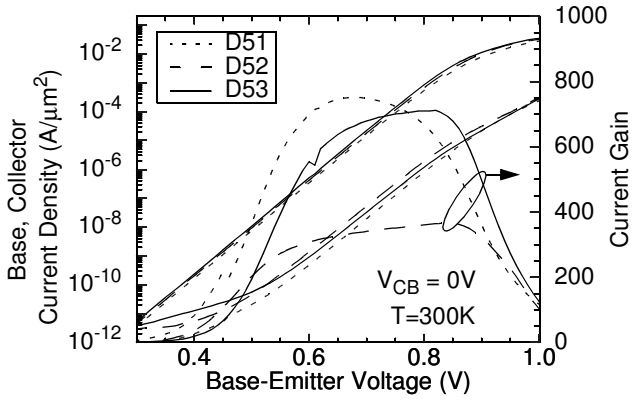

Fig. 5. Gummel plots of 8-emitter devices normalized to the effective emitter area $A_{E,eff}$ (see Table 3) for the HBT generations D51, D52, and D53.

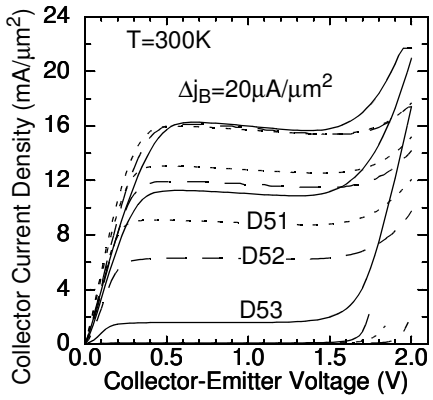

Fig. 6. Output characteristics of 8-emitter devices normalized to the effective emitter area $A_{E,eff}$ (see Table 3) for the HBT generations D51 (dotted), D52 (dashed), and D53 (solid).

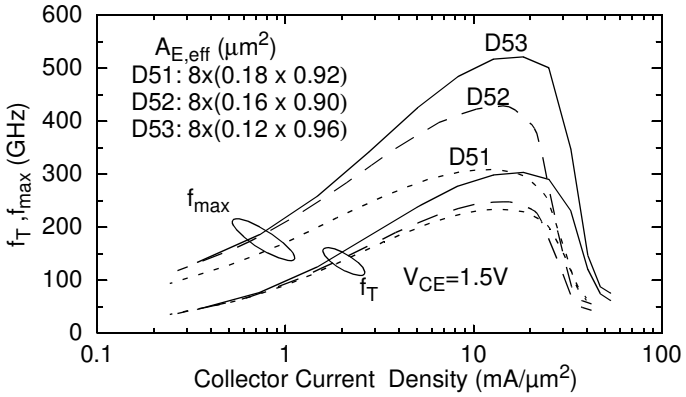

Fig. 7. Transit frequency f_T and maximum oscillation frequency f_{max} vs. collector current normalized to $A_{E,eff}$ for the HBT generations D51-D53. Deembedded small-signal current gain h21 and unilateral gain U vs. frequency were used for extrapolation of f_T and f_{max} at 40GHz with -20dB per frequency decade at V_{CE}=1.5V, T=300K.

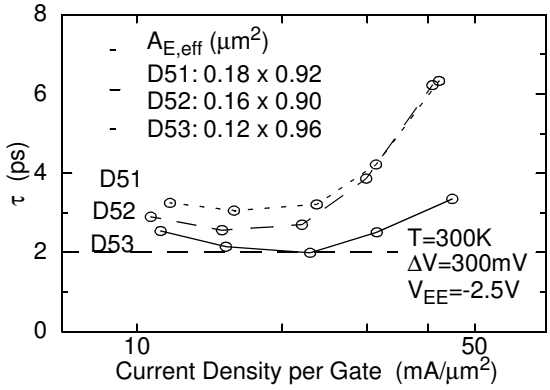

Fig. 8. CML ring oscillator gate delay τ vs. current per gate normalized to $A_{E,eff}$ for oscillators consisting of 53 stages with single emitter HBTs fabricated in D51-D53. Measured at V_{EE}=-2.5V, ΔV=300mV and T=300K.

Table 3. Device parameters of the HBT generations D51-D53. In addition, parameters are listed for devices with D53 process flow and typical layout (LO) dimensions of D51 and D52.

			D51	D52	D53		
	Unit	Measuring conditions			LO53	LO 52	LO51
$A_{E,eff}$	μm²		8x(0.18x0.92)	8x(0.16x0.90)	8x(0.12x0.96)	8x(0.145x0.89)	8x(0.165x0.90)
f_T	GHz	V_{CE}=1.5V	235	250	300	300	300
f_{max}	GHz	V_{CE}=1.5V	300	400	500	490	440
τ	ps	V_{EE}=-2.5V, ΔV=300mV	3.1	2.5	2.0	2.2	2.25
BV_{CEO}	V	I_B reversal, V_{BE}=0.7V	1.7	1.8	1.6	1.6	1.6
BV_{EBO}	V	j_E=10μA/μm²	2.0	1.45	1.7	1.7	1.7
BV_{CES}	V	j_C=0.5μA/μm²	5.1	5.7	5.2	5.2	5.25
$R_E x A_{E,eff}$	Ω μm²	flyback	2.38	2.44	2.12	2.42	2.72
$(R_B+R_E)x A_{E,eff}$	Ω μm²	s11 circle fit, V_{BE}=0.92V	15.6	10.5	8.4	8.6	10.3
$C_{CB}/A_{E,eff}$	fF/μm²	s parameter	18.0	16.4	15.1	17.1	16.6
$C_{BE}/A_{E,eff}$	fF/μm²	s parameter	16.9	18.9	21.8	20.9	19.4
R_{SBi}	kΩ		3.5	2.3	2.6	2.6	2.6