Ultra-low-power SiGe HBT Technology for Wide-range Microwave Applications

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***Abstract* — Ultra-low power SiGe HBT was developed for wide-range microwave applications. The key technologies of the SiGe HBT are based on well-controlled SiGe / Si epitaxial growth techniques with low-temperature chemical vapor deposition (CVD), which give several important features of the low-power SiGe HBT. The prominent features are a robustly designed n^+-n^--p^+ emitter-base junction and a narrow base, realized by an epitaxially grown emitter and a low-temperature thermal cleaning prior to the emitter growth. These features were found to decrease both an emitter junction capacitance (C_{JE}) and a carrier transit time in base (τ_B) in a great extent. The low-temperature CVD also contributed to the reduction of a collector junction capacitance (C_{JC}) by controlling a mono-poly interface in the collector. The effective decrease of C_{JE}, τ_B, and C_{JC} has increased a cutoff frequency (f_T) at a wide range of a collector current density (J_C). As a result, Jc of the SiGe HBT decreased more than 60% compared to published data, at a wide f_T range from 30 to 200 GHz.**

***Index Terms* — Heterojunction bipolar transistors, epitaxial growth, impurity profile, Si spacer, emitter capacitance, collector capacitance, corrector current density.**

I. INTRODUCTION

Next generation wireless communication systems require various properties such as a higher broadband performance to provide high speed data transmission, or low-power-consumption, low-cost, and multifunctional properties for compact transceiver front ends in hand held units. The recent development of high-speed SiGe hetero junction bipolar transistor (HBT) technology offers low-cost, high-speed, and multifunctional solutions for such systems because of its potential for integrating high-speed RF microwave circuits and CMOS base-band circuits into a single chip [1]. For the microwave wireless communications such as next generation mobile phone or fixed wireless access (FWA), the frequency range of the interest is around 6 to 40 GHz, corresponding to 30 to 200 GHz cutoff frequency (f_T) of the SiGe HBT. Since there exists a growing demand for low power solutions due mainly to widely spread mobile communication systems, SiGe HBT needs to operate at such a wide of f_T with very low collector current density (J_C). In other words, f_T increase is needed at a wide range of J_C.

The most effective method for increasing f_T peak value of the SiGe HBT is the reduction of a carrier transit time in base (τ_B) by scaling the vertical profile [2, 3, 4]. On the other hand, a reduction of an emitter junction capacitance (C_{JE}) and a collector junction capacitance (C_{JC}) becomes more effective to increase f_T as J_C becomes lower. Hence, in order to obtain low-current transistor action at the wide f_T range, simultaneous reduction of C_{JE}, C_{JC}, and τ_B is necessary. Since τ_B reduction is likely to increase C_{JE} [4] because of the high impurity concentration at the junction, obtaining high f_T at a wide range of J_C was very difficult.

In the present study, we have developed the low-temperature SiGe HBT process based on well-controlled SiGe / Si epitaxial growth techniques with chemical vapor deposition (CVD) [5], and successfully reduced C_{JE}, τ_B, and C_{JC}, by achieving an abrupt n^+-n^--p^+ junction, a narrow base, and shrinkage of a collector area. As a result, we could decrease the collector current density (J_C) more than 60 % at the wide f_T range from 30 to 200 GHz.

II. FABRICATION PROCESS

Figure 1 shows a structure and corresponding epi-profile of SiGe HBT fabricated in this study. In this structure, n^- SiGe / Si collector and p^+ SiGe base are non-selectively grown on a patterned structure by

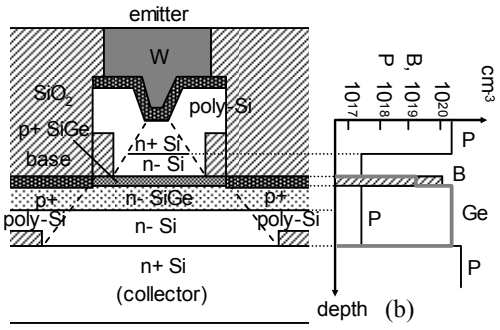


Fig. 1 (a) : Schematic cross section, and
(b) : epi-profile
of fabricated SiGe HBT.

chemical vapor deposition. After opening the emitter-window, n^- Si spacer and n^+ Si emitter are consecutively grown by CVD. The structure has three features that reduce C_{JE}, τ_B, C_{JC}, respectively. First, the n^- Si spacer contributes to decrease C_{JE}. Optimization of the low pressure CVD (LP-CVD) condition realized an abrupt n^+-n^--p^+ structure, and enabled the Si spacer to be fully depleted during the transistor action. Secondary, low-temperature emitter epitaxy is expected to decrease τ_B by keeping an abrupt boron profile in the base. In this study, we have optimized H_2 thermal cleaning condition prior to the emitter growth, and decreased the cleaning temperature down to 700 °C in order to suppress the boron diffusion in the base. Thirdly, optimization of the ultra-high vacuum CVD (UHV-CVD) condition during the collector growth can decrease C_{JC} as described below. Figure 2 shows TEM image around the collector edge of SiGe HBT fabricated by using optimized growth condition. In the figure, collector shape in case of using the conventional growth condition is also indicated by broken line as a reference. Compared to the conventional condition, the optimized condition shows steeper taper angles of at mono-poly interface. This feature effectively

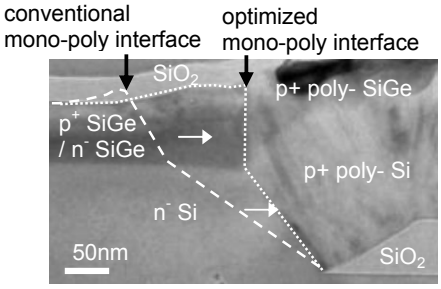


Fig. 2 TEM images around the collector edge of SiGe HBT grown by optimized UHV-CVD condition. Mono-poly interface in case of conventional UHV-CVD condition is indicated by broken line as a reference.

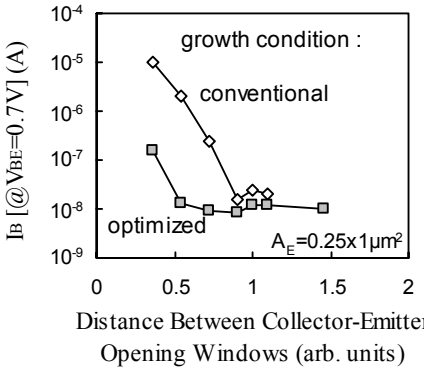


Fig. 3 Base currents (I_B) of SiGe HBTs fabricated by different growth conditions as a function of the distance between collector-emitter opening windows.

enlarges the area tolerance between the opening windows of the collector and the emitter. Figure 3 shows base current of SiGe HBTs as a function of a distance between collector and emitter window edges. Because of the expansion of poly-Si regions into emitter opening window, the occurrence of the base current leakage can be seen in the SiGe HBT fabricated with the conventional growth condition as the edge-distance becomes smaller. However, the current leakage is substantially suppressed in the case of using the optimized condition. Therefore, shrinkage of the collector opening window becomes possible by the adoption of the optimized growth condition, which leads to small C_{JC}.

In order to evaluate each effect quantitatively, two types of SiGe HBTs were fabricated in this study, i.e., the SiGe HBT for decreasing J_C at high f_T (HS_HBT : f_T >100 GHz), and SiGe HBT for decreasing J_C at middle of low frequency range (LC_HBT : 30 < f_T <100 GHz). The typical emitter size in this study is 0.25 x 1 μm^2.

III. Results and Discussions

A. C_{JE} reduction

Figure 4 shows the intrinsic C_{JE} (C_{JE_int}) of the SiGe HBT (HS_HBT) plotted with emitter-base voltage (V_{EB}). In the figure, C_{JE_int} of the conventional SiGe HBT with poly-Si emitter is also shown as a reference. Here, note that f_T of both SiGe HBTs shown in Fig. 4 were designed to be as high as 200 GHz. In Fig. 4, a reduction of C_{JE} can be seen in HS_HBT compared to the conventional SiGe HBT at any value of the voltage range. Moreover, the degree of the reduction becomes larger as V_{EB} approaches to -1 V that is the same condition during the transistor action. The result shows that the insertion of Si spacer enables us to effectively reduce C_{JE} while keeping high f_T.

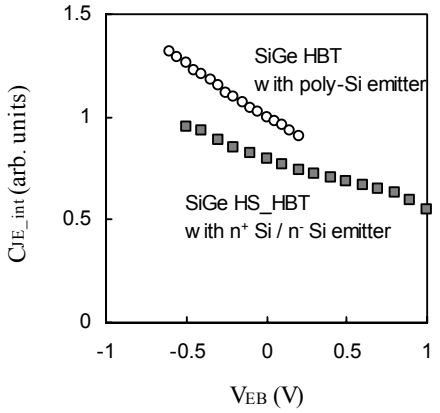


Fig. 4 C_{JE_int}-V_{EB} characteristics of SiGe HBTs.

B. τ_B reduction

Figure 5 shows f_T – J_C characteristics of the SiGe HBTs (HS_HBT) with different base thickness. The monotonous increase of f_T peak can be seen with the decrease of the base width. It is also found that f_T higher than 200 GHz is obtainable in spite of the insertion of n^- Si spacer. The results suggest that the effective decrease of τ_B was enabled by the suppression of impurity diffusion in the base, and J_C at a certain value of f_T prominently decreased especially at the frequency range higher than 100 GHz.

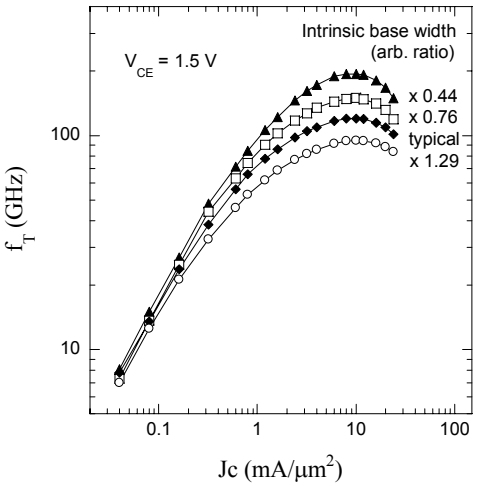


Fig. 5 f_T-J_C characteristics of SiGe HBTs with various base widths.

C. τ_C reduction

Figure 6 shows the C_{JC} - V_{CB} characteristics with various area size of the extrinsic collector. Here, the reduction of the extrinsic collector area size down to 40 % was enabled by using the controlled mono-poly interfaces shown in Fig. 2 (b). Since the extrinsic collector area consists of p^+ poly-Si extrinsic base n^+ buried collector, the effect of extrinsic collector size shrinkage can be seen as a prominent C_{JC} reduction in Fig. 6. Consequently, 30 % decrease of C_{JC} was confirmed at the collector-base voltage of 0.6 V, which is equal with the voltage during the transistor action.

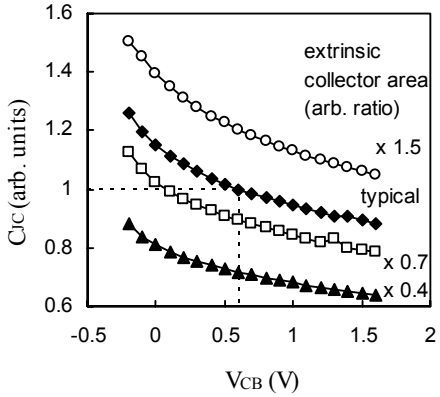


Fig. 6 C_{JC}-V_{EB} characteristics of SiGe HBTs with various extrinsic collector areas.

D. J_C reduction at a wide range of f_T

f_T - J_C characteristics of the optimized HS_HBT and LC_HBT is shown in Fig. 7. In the figure, the published data of the SiGe HBT with 200 GHz of f_T peak [6] is also shown as a reference. Compared to the reference data [6], both HS_HBT and LC_HBT show prominent reduction of J_C at a wide range of f_T, i.e., 60 % J_C reduction was achieved at f_T over 100 GHz (HS_HBT), 70 % J_C reduction was obtained at f_T range between 30 GHz and 100 GHz (LC_HBT). For example, f_T of 50 GHz was obtained at Jc as low as 0.2 mA / μm^2.

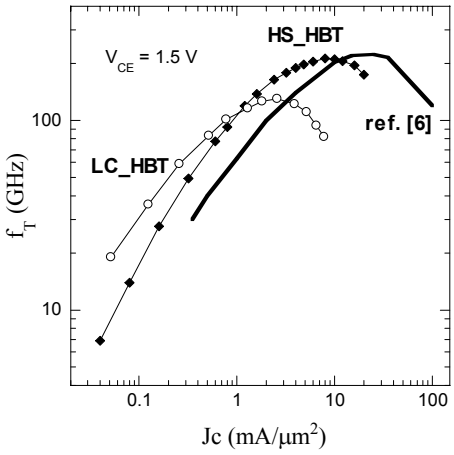


Fig. 7 f_T-J_C characteristics of SiGe HBTs.

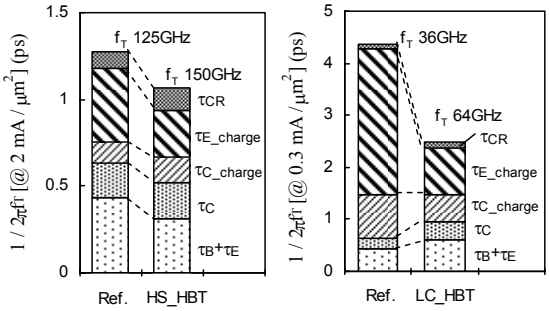
To find a clear relation between f_T and J_C, we have divided the inverse of f_T into each element expressed by a following equation [4]:

$$\frac{1}{2\pi f_T} = \tau_B + \tau_E + \tau_C + \tau_{C\_charge} + \tau_{E\_charge} + \tau_{CR} \quad (1)$$

where τ_B is the electron transit time in base, τ_E and τ_C are electron transit times in an emitter-base and a collector-base depletion region, respectively. τ_{C_charge} and τ_{E_charge} are charge-discharge time constants in the collector-base and the emitter-base depletion region, respectively. τ_{C_charge} and τ_{E_charge} are proportional to C_{JC} and C_{JE}, respectively, and inversely proportional to a collector current (I_C). τ_{CR} is a CR time constant defined by C_{JC} and collector resistance. In these time constants, τ_{C_charge} and τ_{E_charge} can be extracted from f_T-I_C curve. τ_E, τ_C and τ_{CR} can be calculated by using the values of impurity concentration, the emitter/collector capacitance, and

the emitter/collector resistance. τ_B is calculated by subtracting the other constants from $1/2\pi f_T$. The calculated time constants are shown in Fig. 8. In Fig. 8 (a), the time constants at J_C = 2 mA / μm^2 are compared between HS_HBT and our previous SiGe HBT [7] with 210 GHz of f_T, whereas Fig. 8 (b) compares LC_HBT and the previous SiGe HBT at J_C = 0.3 mA / μm^2. In Fig. 8 (a), the reduction of both τ_B and τ_{E_charge} can be seen in HS_HBT, indicating the effect of narrow base and low C_{JE}. In Fig. 8 (b), reduction of both τ_{E_charge} and τ_{C_charge} can be seen in LC_HBT, attributed to the effect of n$^-$ Si spacer and the corrector area shrinkage, respectively. Since LC_HBT has a thicker n$^-$ Si spacer compared to HS_HBT, the reduction of τ_{E_charge} is as low as 70 % which leads the drastic increase of f_T in spite of a slight increase in $\tau_B + \tau_E$ due to an increased carrier transit time in emitter-base depletion region.

As a conclusion, a combination of the low-temperature emitter epitaxial process and the mono-poly interface control in the collector epitaxial process was found to effectively decrease the collector current density more than 60 % at a wide range of the cutoff frequency, which opens the way for SiGe HBT to the higher frequency microwave band applications.



(a) (b)

Fig. 8 Time constants of two HBTs at collector current densities of (a) 2 mA/μm^2, and (b) 0.3 mA/μm^2, compared with the HBT in ref. [7].

IV. SUMMARY

The well-controlled process of ultra-low power SiGe HBT was established for low-power higher frequency microwave band applications. The low-temperature emitter epitaxial process has successfully decreased carrier transit time in base and a charge-discharge time constant in the emitter-base depletion region by realizing abrupt impurity profiles with low-impurity-density Si spacer between an emitter and a base. The mono-poly interface control during the collector growth also contributed to the charge-discharge time constant in the collector-base depletion region by offering a margin of shrinking the collector area. Combining these effects, we could effectively reduce the collector current density more than 60% compared to the published data, at wide range of a cutoff frequency between 30 to 200 GHz.

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