SiGe HBTs Featuring f_T>400GHz at Room Temperature

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***Abstract* — This paper presents the results of investigations on process thermal budget reduction in order to increase the operation frequency of SiGe HBTs. We describe the variations of *dc* and *ac* characteristics of the devices with the spike annealing temperature. Record peak f_T values of 410GHz and 640GHz are reported at room and cryogenic temperatures respectively.**

***Index Terms* — Heterojunction bipolar transistor (HBT), silicon-germanium (SiGe), thermal budget, activation, diffusion, cut-off frequency, terahertz.**

I. Introduction

Si/SiGe:C Heterojunction Bipolar Transistors (HBTs) now feature both transit frequency f_T and maximum oscillation frequency f_{max} exceeding 200GHz at room temperature [1], [2]. Recent works have even reported half-terahertz cut-off frequencies at cryogenic temperatures [3], [4]. Thus, SiGe HBTs are now able to address millimeter-wave applications up to 100GHz [5]. Moreover, the interest in emerging terahertz (THz) applications is growing in the electronic community. Despite the significant progress which had been made in improving HF performances of III-V HBTs [6], there is a huge challenge to reach terahertz performances in a low-cost and highly integrated silicon manufacturing platform.

This work focuses on the increase of f_T above the current state-of-the-art by optimizing the vertical doping profiles. Complementary investigations on lateral dimensions to improve f_{max} will be performed in the future. One of the main limitations to increase f_T is the diffusion of doping species during some high temperature process operations, the main being the CMOS source/drain activation annealing (~1100°C). This leads to a limitation of f_T to ~300GHz for the 0.13-µm CMOS compatible HBTs developed in-house [1]. Hence, a major development axis is the reduction of the thermal budget during device fabrication. The paper first describes the low temperature (low-T) process, pointing out the modifications made on the reference BiCMOS process. Second, we present the impact of thermal budget variations on static behavior and technological parameters of HBTs. Then, we show high-frequency characteristics measured both at room and cryogenic temperatures. We finally conclude and discuss the perspectives of this study.

II. Low Temperature Process

For this study, we used a fully self-aligned double-polysilicon emitter-base structure using a selective epitaxial growth (SEG) of a SiGe:C base. The process flow is detailed in [7]. However, several steps have been modified in order to reduce the thermal budget after the boron in-situ doped base deposition. Fig.1 presents the process temperature differences between a reference HBT process flow and the one initially defined for this study.

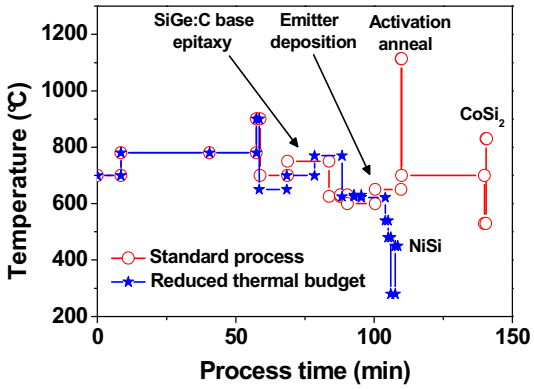

Figure 1: Thermal budget vs. cumulative process time for a standard and a low-T SiGe HBT fabrication process

The fabrication is similar to the standard process until the base deposition. The thickness of the boron in-situ doped SiGe:C layer has been reduced from 20 to 15nm, the Germanium content being 10% at emitter side and 25% at collector side. An other important modification is that we replaced the arsenic-doped polysilicon by a phosphorous in-situ doped polysilicon to form the emitter. This leads to a lower emitter resistance R_E thanks to a better activation at low temperature [8]. The furnace deposition of the oxide/nitride stack protecting the non-silicided areas (Siprot) has been replaced by low-T depositions (540°C SACVD oxide & 480°C PECVD nitride). For the first experiments, the final CMOS activation annealing (~1100°C) has been removed from the process flow. However, a spike annealing at a lower temperature was performed in most of the following investigations. Finally, the conventional cobalt silicide

$CoSi_2$ has been replaced by a nickel silicide NiSi requiring a lower annealing temperature (450°C for NiSi vs. 830°C for $CoSi_2$).

Thanks to these process optimizations, the thermal budget stays under 700°C after the base deposition (without the spike annealing). This prevents dopants diffusion and allows the transistor to preserve reduced vertical dimensions. A TEM cross-section of the device is shown in Fig. 2. We kept the reference layout which can be optimized by a lateral shrink in order to minimize parasitic resistances and capacitances.

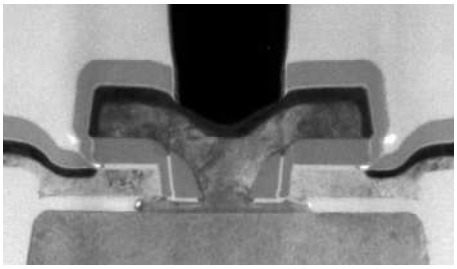

Figure 2: TEM cross-section of a 0.13×3.6µm² HBT

III. Spike Annealing Temperature Impact

We first fabricated SiGe HBTs using the low-T process flow without final activation annealing. Functional devices have been obtained but with a non-ideal base current behavior at middle injection visible in Fig.3. This can be attributed to the presence of recombination centers and hydrogen traps in the emitter-base depletion region. Regarding HF performances, the transit frequency has not been significantly improved versus the reference process (f_T ~270GHz) and the maximum oscillation frequency f_{max} remains below 200GHz because of high base resistance values. To further understand the impact of the process thermal budget on *dc* and *ac* characteristics, spike annealings from 950°C to 1080°C were investigated.

A. Currents and current gain β

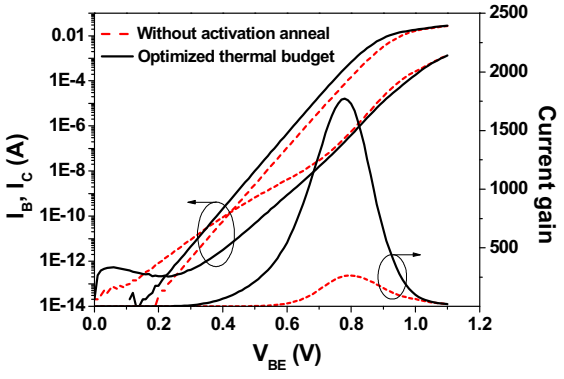

Figure 3: Gummel plots and current gain of 0.13×3.6µm² HBTs with and without the optimized thermal budget

Fig. 3 shows Gummel plots and current gain β of two 0.13×3.6µm² HBTs processed with and without a 1000°C final spike annealing. The non-ideality of the base current at middle injection strongly decreases after the spike annealing. This shows the necessity to exceed a certain temperature in order to remove defects which degrade devices performance and reliability. Moreover, a band-to-band tunneling is visible on the base current at low injection (V_{BE}<0.2V). The observation of this phenomenon is directly linked to the higher dopants concentrations at the emitter-base junction due to phosphorus and boron diffusion [9]. Finally, we observe a significant collector current increase which leads to a strong improvement of the current gain β (×8).

B. Extrinsic base resistance

In a low temperature integration scheme, the base resistance is probably the most critical electrical parameter because it will dramatically limit the maximum oscillation frequency. The three components of the total base resistance R_B are shown in Fig.4. Both the extrinsic and intrinsic base resistances have been investigated in order to optimize our devices.

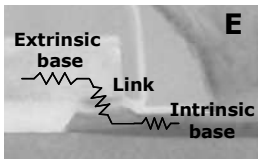

Figure 4: TEM cross-section showing R_B components

Fig. 5 presents the variations of boron implanted polybase (extrinsic base) and phosphorous in-situ doped polyemitter sheet resistances with the spike annealing temperature. We observe a 30% decrease (from 430 to 300Ω/sq) of the unsalicided polybase resistance when the annealing temperature increases from 950°C to 1080°C. This can be explained by a constant increase of boron activation in this temperature range. The link resistance will be also improved with the temperature increase due to boron diffusion from the polybase to the intrinsic base.

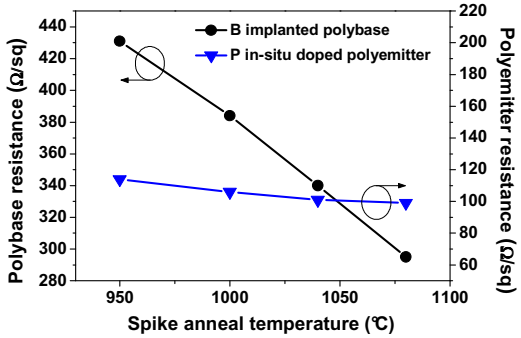

Figure 5: Polybase and polyemitter sheet resistances vs. spike annealing temperature

The low spike temperature dependence of the polyemitter sheet resistance confirms a quasi complete phosphorus activation at low temperature (~100Ω/sq).

C. Intrinsic base resistance

At first order, the intrinsic base resistance R_{Bi} depends on the boron and germanium profiles, the dopants activation and the emitter pinching. Simulations have shown that the boron diffusion induced by the spike annealing leads to an improvement of the sheet resistance due to mobility enhancement. Measurements of R_{Bi} in Fig. 6.a confirm this behavior with spike temperatures lower than 1000°C. But at higher temperatures, R_{bi} increases due to the onset of pinching by emitter dopants. These results demonstrate that the minimum of R_{Bi} is achieved for a ~1020°C spike annealing in our process conditions. The evolution of R_B* (technological parameter depending on R_{Bext}, R_{Link} and R_{Bi}) vs. R_{Bi} for different vertical profiles is plotted in Fig. 6.b. Although R_{Bi} is degraded by the emitter pinching at high temperatures, the base resistance is improved thanks to the better boron activation in the extrinsic base and thanks to the boron diffusion in the base link from the highly doped polybase. As a consequence, the minimum of R_B* is obtained for a higher spike temperature than the minimum of R_{Bi}.

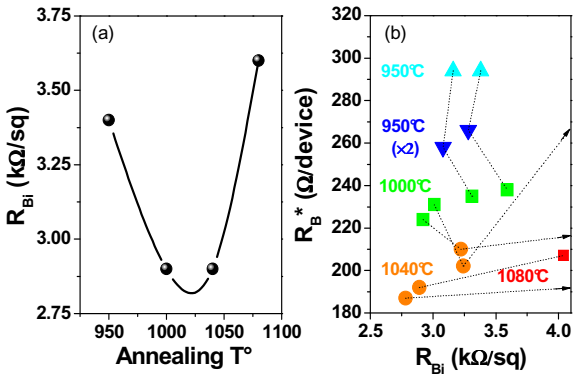

Figure 6: R_{bi} vs. annealing T° (a) and R_B* vs. R_{bi} for various annealing temperatures and vertical profiles (dot lines) (b)

IV. Dynamic Performances

Cut-off frequencies f_T and f_{max} of HBTs have been extracted from S-parameter measurements up to 110GHz and 45GHz at room and cryogenic temperatures respectively. Two different HBT layouts have been investigated. The first one is the reference CBEBC layout featuring shallow trenches (STI) between emitter-base and collector areas. The second is the "one-active" C_BE^BC cellular layout with out-of-plane base contacts described in [10] and requiring a fragmented emitter. The variations of the transit frequency f_T versus collector current density J_C are shown in Fig. 7 at 294K and 35K for a 0.13×3.6µm² CBEBC and a 5×(0.17×1.2)µm² C_BE^BC HBT.

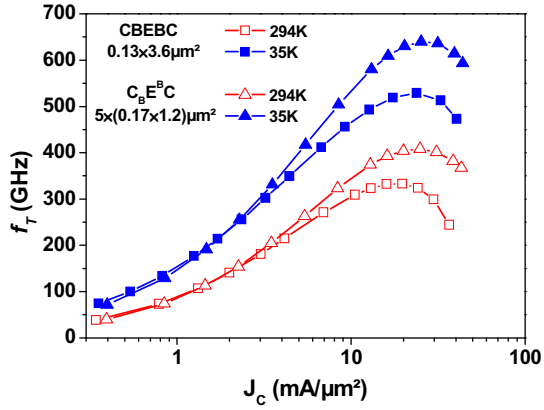

Figure 7: Transit frequency f_T vs. J_C measured at 294K and 35K for low thermal budget SiGe HBTs (V_{CB}=0.5V)

State-of-art peak f_T values of 340GHz (f_{max}=260GHz) at 294K and 535GHz (f_{max}=350GHz) at 35K occurring at J_C around 20mA/µm² are achieved with the reference layout. Regarding the C_BE^BC HBT, record f_T values of 410GHz and 640GHz were measured at 294K and 35K respectively, the collector current density J_C at peak f_T, being larger than 20mA/µm². To the authors' knowledge, this is the first demonstration of a SiGe HBT transit frequency above 400GHz at room temperature [11], [12]. Transistors parameters at 294K and 35K are summarized in Table I.

TABLE I
TRANSISTORS PERFORMANCES SUMMARY AT 294K AND 35K

Parameters	Reference layout		One-active layout		Unit
	294K	35K	294K	35K	
f_T	340	535	410	640	GHz
f_{max}	260	350	150	185	GHz
J_C at peak f_T	18	23	25	28	mA/µm²
BV_{CEO}	1.45	1.48	1.15	1.19	V
$\tau_{EC,min}$	0.47	0.30	0.39	0.25	ps
$\tau_{EC,0}$	0.37	0.29	0.26	0.21	ps

The absence of STI between emitter-base and collector areas for the "one-active" HBTs leads indeed to both an increased collector doping and a reduced collector resistance R_C. Then, the minimum delay of the device $\tau_{EC,min}=1/2\pi f_{T,max}$ is about 20% shorter than for the reference CBEBC HBTs (0.39 vs. 0.47ps at 294K and 0.25 vs. 0.30ps at 35K). The emitter-base architecture being the same for the two devices, the improvement of f_T is directly linked to the decrease of R_C and τ_C (collector transit time). As expected, f_{max} is strongly degraded by the base-collector capacitance which is three times larger compared to the reference layout.

Various process conditions (collector doping, base width and doping, germanium profile) have also been investigated in this study. Fig. 8 shows main f_T/BV_{CEO} trade-offs achieved with low thermal budget SiGe HBTs at room and cryogenic temperatures for the reference CBEBC layout and the one-active C_BE^BC layout.

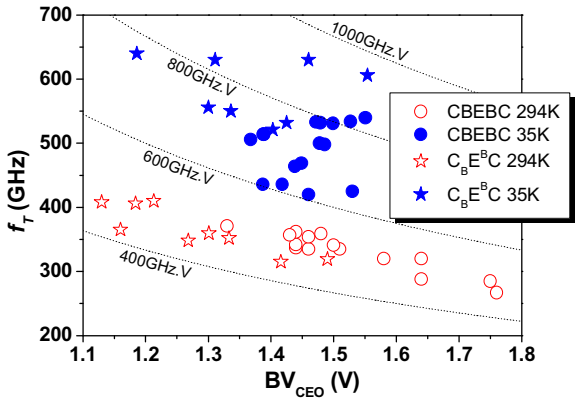

Figure 8: f_T / BV_{CEO} trade-offs achieved in this study at room and cryogenic temperatures

f_T/BV_{CEO} trade-offs from 285GHz/1.75V to 370GHz/1.35V have been obtained at room temperature with the 0.13×3.6µm² CBEBC HBT. This leads to impressive f_T.BV_{CEO} products of 530GHz.V at 294K and 840GHz.V at 35K. Concerning the one-active C_BE^BC layout, record f_T.BV_{CEO} products of 640GHz.V and 910GHz.V at 294K and 35K respectively, have been achieved.

TABLE II
TRANSISTORS PARAMETERS COMPARISON (A_E=0.13×3.6µm²)

Parameters	Measurements conditions	Reference process	Low-temp process	Unit
f_T	V_{CB}=0.5V	260	360	GHz
f_{max}	V_{CB}=0.5V	340	245	GHz
J_C at peak f_T		14	23	mA/µm²
β	V_{BE}=0.75V	1500	3800	-
V_{AF}		270	81	V
BV_{CEO}	V_{BE}=0.7V	1.55	1.48	V
BV_{CBO}		5.3	5.2	V
C_{BE}	V_{BE}=V_{CE}=0V	9.5	10.9	fF
C_{BC}	V_{BE}=V_{CE}=0V	8.2	9.4	fF
R_{Bi}		2.0	3.7	kΩ/sq
R_B	V_{BE}=0.87V, V_{CE}=0V	17	85	Ω
R_E	V_{BE} from 0.8V to 0.9V	4.3	5.1	Ω

Table II reports the main parameters of 0.13×3.6µm² CBEBC HBTs fabricated with the reference process and the low thermal budget process developed in this study. We observe an inversion of the f_T/f_{max} trade-off. The current gain β is more than two times higher with the low-T process thanks to a larger collector current. The slight increase of junction capacitances is explained by the more aggressive vertical profiles. The higher intrinsic base resistance (3.7kΩ/sq vs. 2.0kΩ/sq) is due to a thinner base width and a lower boron diffusion. As expected, there is a strong increase of R_B (85 vs. 17Ω), which is responsible for the f_{max} degradation. This confirms the major contribution of the extrinsic base and link resistances in the total base resistance R_B.

V. CONCLUSIONS & PERSPECTIVES

We have presented and explained the evolution of *dc* and *ac* characteristics of SiGe HBTs with the annealing temperature. The objective to improve the transit frequency f_T has been successfully achieved by optimizing the vertical profile of the transistor. Record peak f_T values of 410GHz and 640GHz were measured at 294K and 35K respectively. To the authors' knowledge, this is the first demonstration of a SiGe HBT featuring f_T > 400GHz at room temperature. However, f_{max} of these low thermal budget HBTs is limited by both the base resistance and the base-collector capacitance since no lateral shrink was applied for this study. A first perspective of this work is then to modify the transistor design rules in order to get both f_T and f_{max} > 400GHz. A second one is the integration of such a device in an advanced CMOS node, 65nm and 45nm being two interesting nodes for the thermal budget compatibility.

ACKNOWLEDGEMENT

The authors wish to thank the staff of 200mm Si plants in STMicroelectronics Crolles and Rousset, and CEA-LETI Grenoble involved in the various aspects of this work.

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