High-speed SiGe HBT Technology and Applications to mm-wave Circuits

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Abstract. **A SiGe bipolar technology for high frequency applications is presented. A transit frequency of 206 GHz, a maximum oscillation frequency of 200 GHz and a ring oscillator gate delay time of 3.9 ps have been obtained. With a 110 GHz dynamic frequency divider, a 86 GHz static frequency divider, a 52 GHz dual modulus 256/257 prescaler and a 98 GHz VCO state of the art high frequency circuits could be realized in this SiGe technology.**

I. Introduction

Recent advances in SiGe bipolar technology enabled impressive transistor parameters like maximum oscillation frequencies [1] and transit frequencies [2] in excess of 300 GHz and gate delay times down to 3.6 ps [3]. Therefore, even very high frequency applications like wireless LANs at 60 GHz, optical communication at 80 Gbit/s and radar systems around 77GHz, which can now only be realized in expensive III-V technologies, seem to become feasible in a low cost silicon based technology. To address these markets we have developed a SiGe bipolar technology with 200 GHz transit frequency and 3.9 ps ring oscillator gate delay time. In addition several key circuit building blocks (e.g. frequency dividers, prescaler, VCO) have been designed and fabricated to investigate the potential of SiGe bipolar technology for these demanding application fields.

II. Transistor Structure

Our transistor has a double-polysilicon self-aligned transistor configuration to achieve small device parasitics. In this device concept the SiGe base is integrated by selective epitaxial growth. The transistor fabrication process is described in detail in [4]. Carbon is incorporated in the SiGe base for reducing undesirable boron outdiffusion and for achieving steep doping profile gradients. Furthermore, we have replaced the conventional polysilicon emitter by a heavily doped monocrystalline emitter contact. This avoids an interfacial oxide between n^+-emitter contact and active silicon area, which is difficult to control in conventional polysilicon emitter HBTs, and guarantees a small emitter resistance. A TEM cross section of the emitter-base configuration is shown in fig. 1. The effective emitter width is 0.18 µm.

The SIMS doping profile of the fabricated transistors is shown in fig. 2. By the self-aligned collector implantation a collector doping level of $1x10^{18}$ cm^{-3} has been employed. The Ge content is steeply graded across the base and the maximum Ge fraction is 25%. In the neutral base a boron spike with a concentration of $3 \cdot 10^{19}$ cm^{-3} is grown to enable the low base sheet resistance of 3.0 kΩ/□. At the emitter side the base is lowly doped with a concentration of $1x10^{18}$ cm^{-3} in order to obtain a small emitter-base capacitance. The boron peak is surrounded by carbon with a concentration of $3 \cdot 10^{19}$ cm^{-3} to suppress undesirable boron diffusion. In combination with low thermal budget processing very steep boron doping profile gradients have been achieved resulting to a final metallurgical base width of only 27 nm.

III. Electrical Results

Fig. 3 shows the typical transfer characteristics of transistors with an emitter area of 0.18 x 2.8 μm^2. For a base-emitter voltage of 0.8 V the current gain is 400. Also shown in fig. 3 is the transfer characteristic of a transistor array which is configured with 7000 transistors connected in parallel. The yield of these arrays is typically 85%. Fig. 4 gives the common emitter output characteristics. The open base emitter-collector breakdown voltage is 1.8 V and the base-collector breakdown voltage is 5.8 V. Fig. 5 shows the transit frequency versus the collector current for different base collector voltages V_{BC}. The transit frequency reaches its maximum of 206 GHz at V_{BC}=0 and a collector current density of 8 mA/μm^2. The maximum oscillation frequency has been extrapolated from Masons unilateral gain at 20 GHz with -20 dB/dec role off. Fig. 6 shows the dependency of the maximum oscillation frequency on collector current. The maximum oscillation frequency peaks at 200GHz.

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CML ring oscillators with a differential voltage swing of 400 mV have been used to evaluate the potential of our SiGe technology for high frequency circuit applications. The dependency of the gate delay time on switching current is shown in fig. 7. At a switching current density of 8 $mA/\mu m^2$, a minimum gate delay time of 3.9 ps has been achieved. Table 1 summarizes the most important transistor parameters. The trade offs between these transistor parameters have been optimized to enable demanding mm-wave circuit applications.

IV. Circuit Results

Table 2 shows the results of various state of the art circuits which have been fabricated in our SiGe technology. The dynamic frequency divider [5] uses the principle of regenerative frequency division and has a divide ratio of 2. The circuit operates with a supply voltage of -5 V at a total supply current of 62 mA. The dynamic frequency divider was measured on wafer with a single ended input signal. Fig. 8 shows the minimum input power versus the input frequency. The dynamic divider operates from 35 GHz to 110 GHz which is the highest frequency that our measurement equipment can provide.

The static frequency divider [5] in table 2 has a divide ratio of 32 and consists of 5 master-slave flip-flops. This divider is based on the E^2CL circuit principle. The circuit operates with a supply voltage of -5 V and consumes 180 mA. The measurements on the static frequency divider were performed on wafer using a single ended input signal. Fig. 9 shows the minimum input power versus the input frequency. The circuit operates up to a maximum input frequency of 86 GHz. Such frequency dividers are key circuit elements in a wide variety of application fields as for example in optical communications and measurement equipment.

Table 2 also shows the results of a dual-modulus prescaler. The circuit has selectable divide ratios of 256 and 257 and operates up to a maximum input frequency of 52 GHz. Such dual-modulus prescalers are essential building blocks for frequency synthesisers. The dual modulus prescaler is based on a widely-used architecture which consists of a synchronous divide by four/divide-by-five stage at the input which is followed by an asynchronous six stage divider [6]. Fig. 10 shows the required minimum input power versus input frequency. The maximum input frequency of the prescaler in both divide-by-256 and divide-by-257 modes is 52 GHz. This is the highest operating frequency reported for a dual-modulus prescaler so far. The amplitude of the output signal is larger than 1 V_{pp}. The circuit has been optimized for low power consumption and consumes only 36 mA from a 3.3V supply.

Voltage controlled oscillators (VCOs) are key components in many applications ranging from optical communication systems to automotive radar sensors. To demonstrate the high-speed potential of SiGe technology a VCO has been designed for very high operating frequency. The fundamental-mode VCO [7] in table 2 is based on the common collector Collpitts oscillator and uses the negative resistance oscillator model. The VCO consumes 12 mA and operates with a supply voltage of -5 V. The fundamental-mode oscillator can be tuned from 95.2 GHz to 98.4 GHz. The measured output power is about -9 dBm, however due to losses in the measurement setup, the actual output power is about -6 dBm. The measured output spectrum of the circuit is shown in fig. 11 at a center frequency of 98 GHz.

V. Conclusion

We have developed a high performance SiGe bipolar technology for future high frequency applications. The transistors have a selectively grown narrow and highly doped SiGe:C base and monocrystalline emitter contacts. A transit frequency of 206 GHz, a maximum oscillation frequency of 200 GHz and a ring oscillator gate delay time of 3.9 ps are achieved. With a 86 GHz static frequency divider, a 110 GHz dynamic frequency divider, a 52 GHz dual modulus prescaler and a 98 GHz fundamental-mode VCO excellent circuit results have been achieved. These results show that demanding application fields like 77 GHz automotive radar and 80 Gbit/s optical data communication which seemed to be reserved for the III-V semiconductor technologies in the past, will become feasible in low-cost SiGe technology in a highly integrated manner.

Acknowledgement

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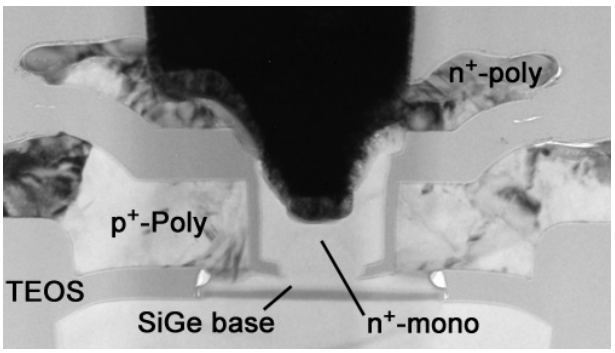

Fig. 1 TEM cross section of the emitter-base complex of a transistor with effective emitter width of 0.18 µm

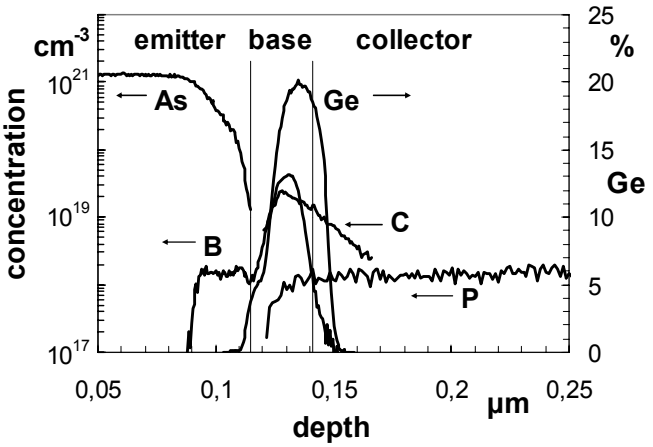

Fig. 2 Final doping profile of the transistors

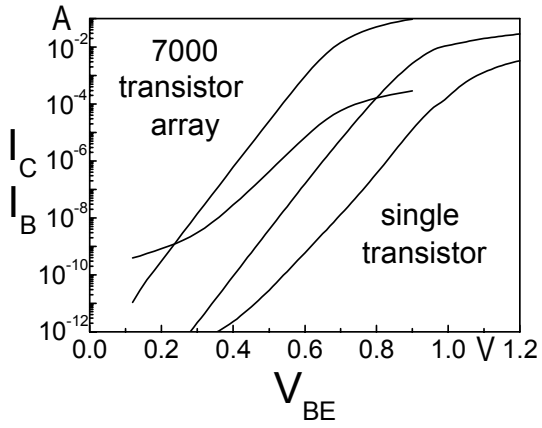

Fig. 3 Transfer characteristics of a transistor with $A_E = 0.18 \times 2.8\ \mu m^2$ and a transistor array with $A_E = 7000 \times 0.18 \times 2.8\ \mu m^2$

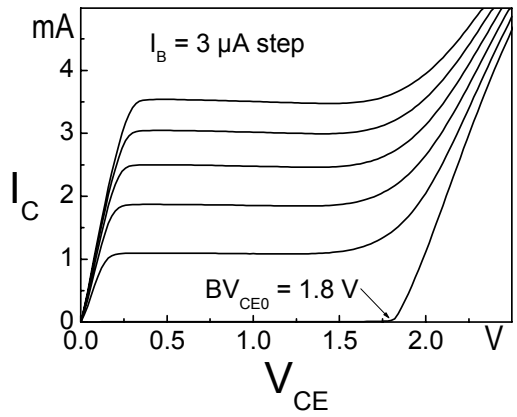

Fig. 4 Output characteristics of a transistor with $A_E = 0.18 \times 2.8\ \mu m^2$

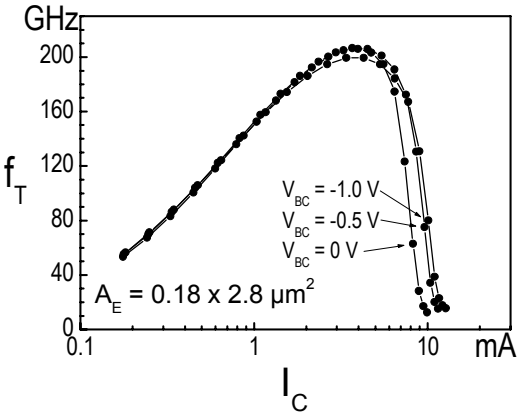

Fig. 5 Transit frequency f_T vs. collector current I_C

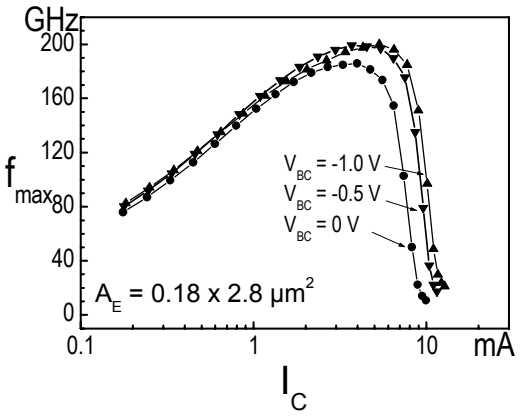

Fig. 6 Maximum oscillation frequency f_{max} vs. collector current I_C

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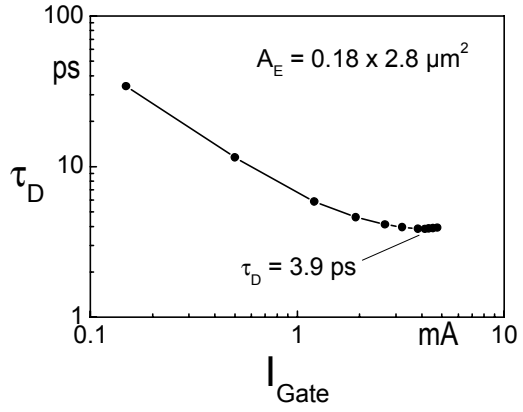

Fig 7 CML gate delay τ_D vs. collector current per gate I_{gate}

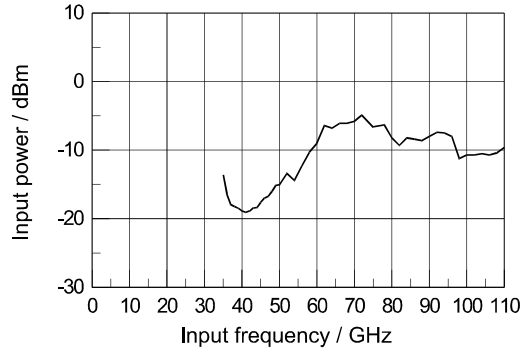

Fig. 8 Input sensitivity of the dynamic frequency divider

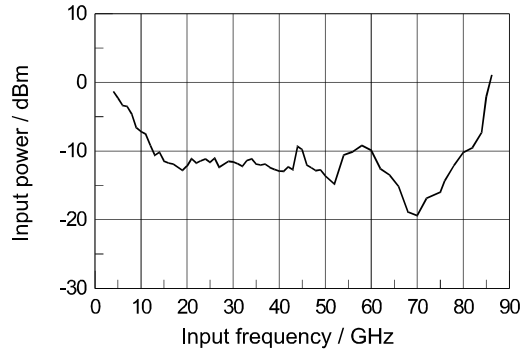

Fig. 9 Input sensitivity of the static freuqency divider

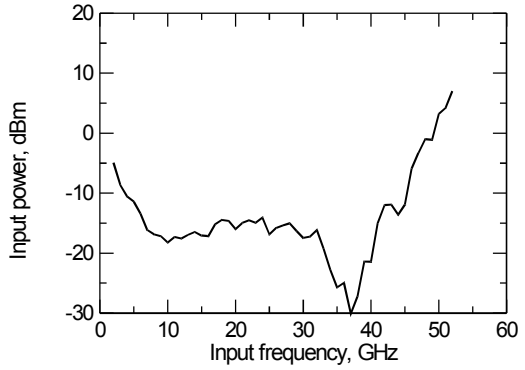

Fig. 10 Input sensitivity of the dual-modulus prescaler

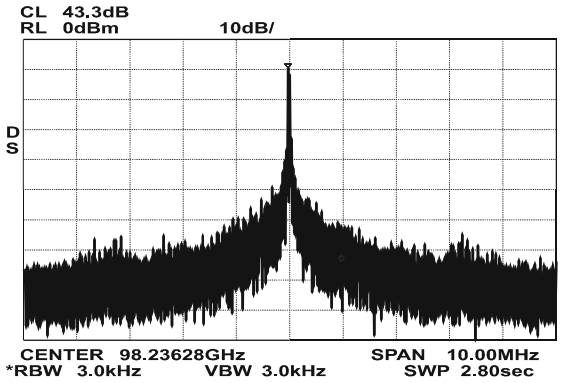

Fig. 11 Output spectrum of the VCO at 98 GHz center frequency

A_E	0.18 x 2.8 µm²
β	400
R_{BI}	3.0 kΩ/□
BV_{CE0}	1.8 V
BV_{CB0}	5.8 V
C_{EB}	7.6 fF
C_{BC}	5.7 fF
C_{CS}	6.6 fF
R_B	65 Ω
R_E	4 Ω
f_T	206 GHz
f_{max}	200 GHz

Table 1. Transistor parameters

	static frequency divider [5]	dynamic frequency divider [5]	dual-modulus pre-scaler	VCO [7]
frequency range	86.2 GHz	35 to 110 GHz	≤ 52 GHz	95.2 to 98.4 GHz
divide ratio	32	2	256,257	-
supply current	180 mA	62 mA	36 mA	12.2 mA
supply voltage	-5 V	-5 V	-3.3 V	-5.0 V
output power	-	-	-	-9.6 to -8.6 dBm

Table 2 Data of fabricated high-frequency circuits