R820T
High Performance Low Power Advanced Digital TV Silicon Tuner Datasheet

Rafael Micro

Suite 808, Building 53, No.195, Sec.4, Chung Hsing Road, Chutung, HsinChu 310, Taiwan , R.O.C.
310 台灣新竹縣竹東鎮中興路四段 195 號 53 館 808 室

Tel: 886-3-5820868 Fax: 886-3-5820968 www.rafaelmicro.com

■ Ordering Information

Part Number	Description	Package Type
R820T	Digital TV Silicon Tuner	QFN 24

Contact Information:
Suite 808, Building 53, No. 195, Sec. 4, Chung Hsing Road
Chutung, HsinChu 310,Taiwan, R.O.C. www.rafaelmicro.com
Tel: 886-3-5820868 Fax: 886-3-5820968
Sales (Taiwan): 886-3-5820868 ext. 211 marshall.lee@rafaelmicro.com
Sales (China): 86-1360-2679953 jaff.wu@rafaelmicro.com
Application Engineering : 886-3-5820868 ext. 235 vincent.huang@rafaelmicro.com

Revision History

Revision	Description	Owner	Date
1.0	Preliminary Release	Vincent Huang	2011/9/14
1.1	Modify reference schematic	Vincent Huang	2011/11/16
1.2	Modify reference schematic	Vincent Huang	2011/11/30

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R820T

High Performance Low Power Advanced Digital TV Silicon Tuner

General Description

In heritage from Rafael Micro's state-of-the-art architecture, the R820T digital silicon tuner achieves the lowest power consumption and the smallest font factor. R820T offers unmatchable RF performance for all digital broadcast television standards including DVB-T, ATSC, DMB-T, ISDB-T,. With innovative AccuTune™ and TrueRF™ mechanisms, R820T provides superior performance in sensitivity, linearity, adjacent channel immunity, and image rejection. The chip embeds a smart power detector to optimize different input power scenarios as well as the spurious free dynamic range.

The R820T is a highly integrated silicon tuner that builds in low noise amplifier (LNA), mixer, fractional PLL, VGA, voltage regulator and tracking filter, eliminating the need for external SAW filters, LNA, balun, and LDO. Thanks the LNA architecture, R820T offers the lowest cost and high performance solution for digital TV application. On-chip LDO, high performance LNA, and small package enable R820T the perfect solution for both cost and font factor sensitive applications.

With proprietary GreenRF techniques, R820T achieves both high performance and the lowest power consumption which perfectly compliant with the worldwide trend. The R820T comes in a small and thin QFN RoHs compliant package.

Features

- Support all digital TV standards: DVB-T, ATSC, DTMB and ISDB-T.
- Lowest BOM cost WITHOUT external SAW filters, LNA, balun, LDO, and adjustable parts.
- Low cost Single-In Digital TV Application
- Compliant with EN 300 744, Nordig 2.2, D-BOOK 7.0, ARIB B21, ABNT 15604, ATSC A74 and GB20600-2006
- Compliant with EN-55020, EN55013 and FCC
- Ultra low power consumption < 178mA
- Single power supply 3.3V
- 2-wired I2C interface
- 24-pin 4x4 QFN lead-free package

Applications

- Terrestrial Digital TV
- Desktop/Laptop PCTV, Mini-card, and USB peripherals
- Set Top Box
- Portable Media Player
- Automobile TV

Figure A: Example of DTV reception for PCTV Applications

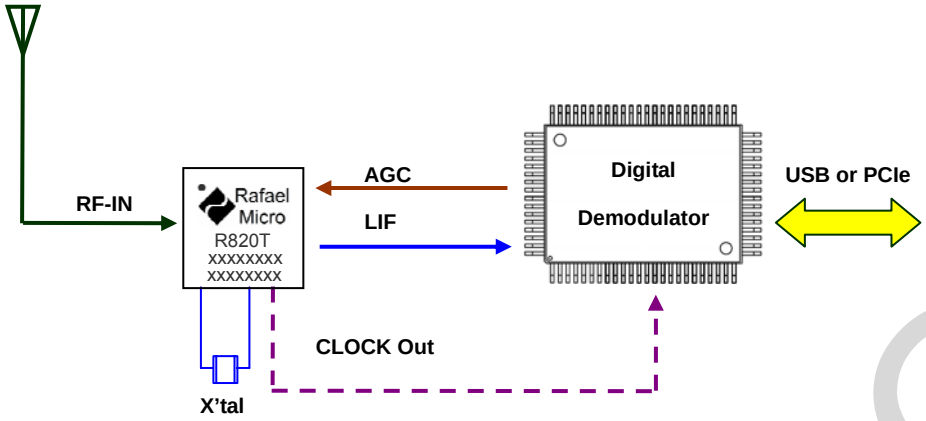


Figure B: Example of Set Top Box Applications

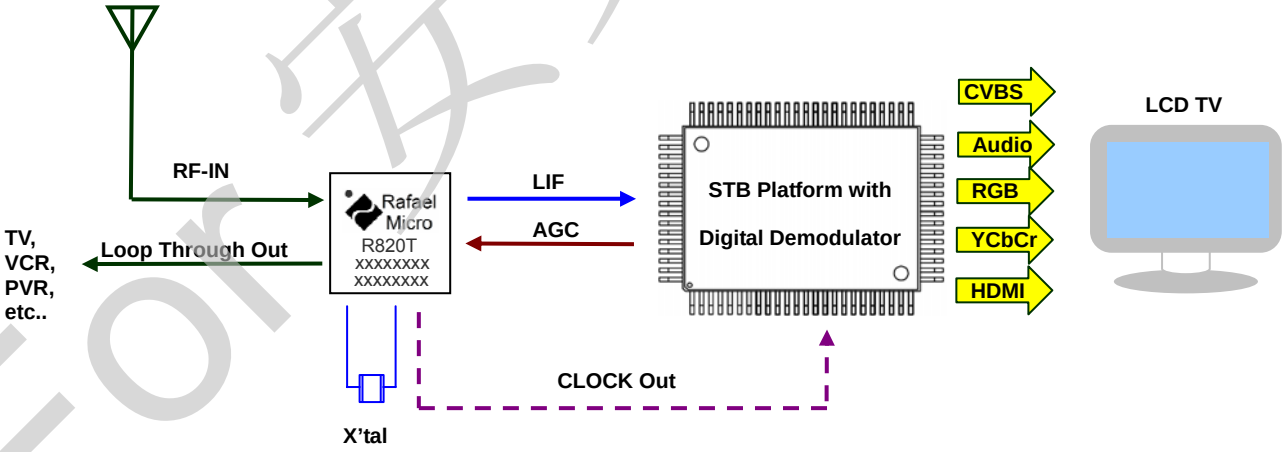
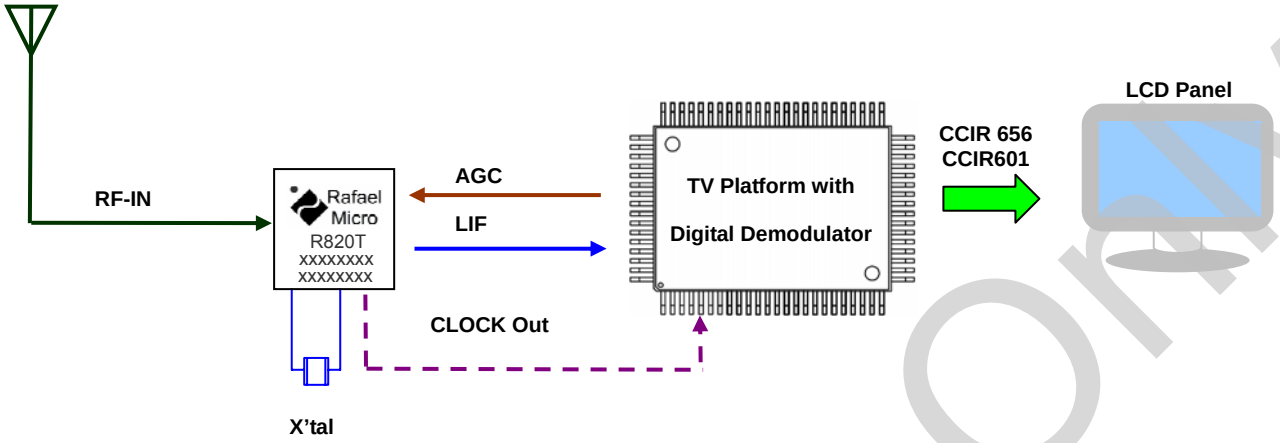
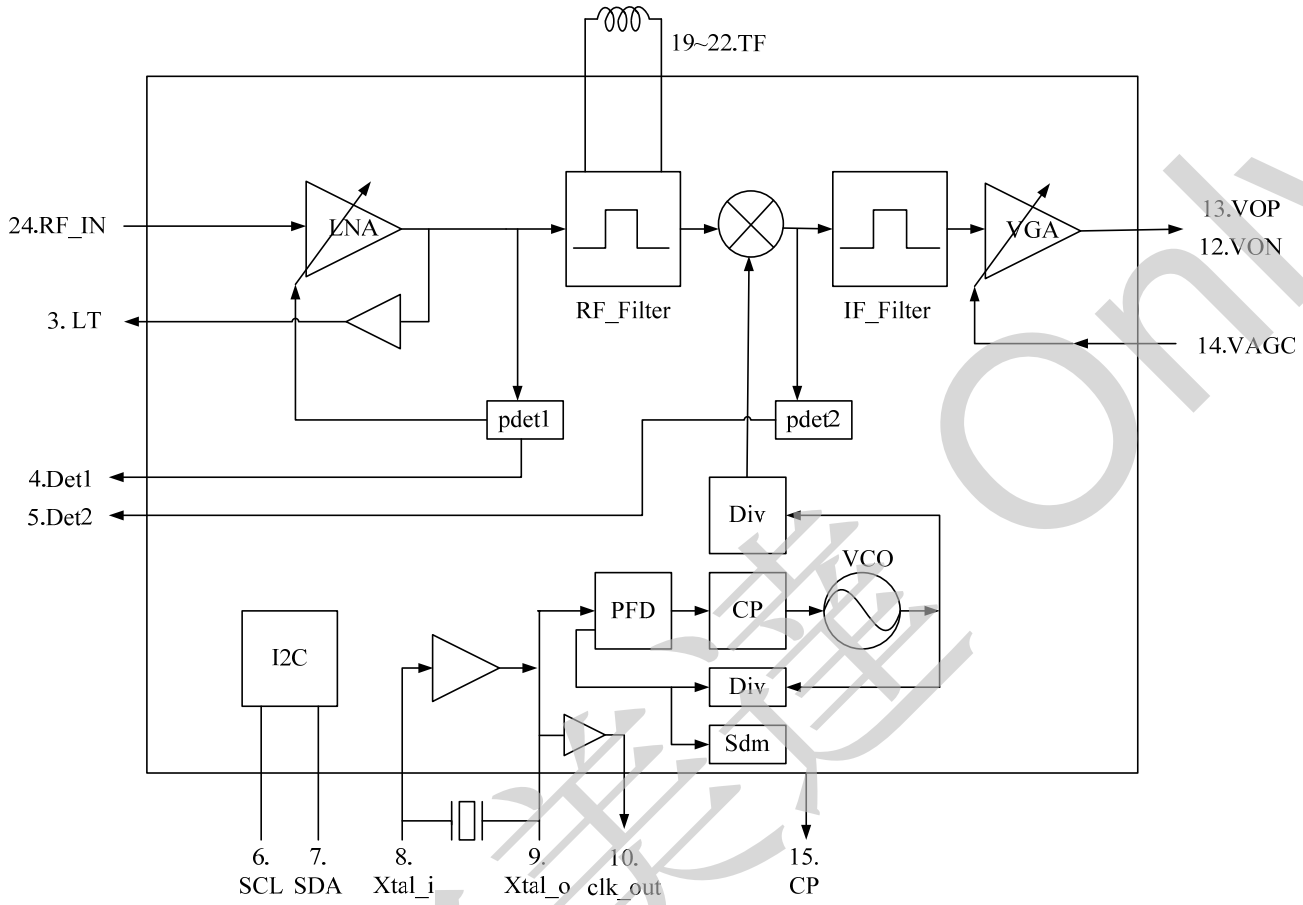


Figure C: Example of LCD TV Applications



Functional Block Diagram

Figure D: Simplified R820T Block Diagram



■ Quick Reference Data

Typical figures

- ■ Frequency range: 42 to 1002 MHz
- ■ Noise figure : 3.5 dB @ RF_IN
- ■ Phase noise: -98 dBc/Hz @ 10 kHz
- ■ Current consumption: ＜178 mA @ 3.3V power supply
- ■ Max input power: +10 dBm
- ■ Image rejection: 65 dBc

note: [dBm]=[dBuV on 75Ω] -108.75dB

Contents

Figure

Table

1 Electrical Parameters

1.1 DC Parameters

Table 1-1 : Electrical DC Parameters

Parameters	Condition	Units	Min	Typical	Max
VCC Input voltage		V	3.0	3.3	3.6
Operation Temperature		°C	-20	25	85
Sleeping Mode Current	LT OFF	mA		9	
Standby Mode Current	LT ON	mA		64	
Total Current Consumption	After Programming	mA		178	195

1.2 AC Parameters

Table 1-2 : Electrical AC Parameters

Parameters	Condition	Units	Min	Typical	Max
Input Return Loss[1]	S11	dB		-10	
Operation Frequency Range		MHz	42		1002
Voltage Gain		dB	85		95
AGC Range		dB		104	
Noise Figure	@ Max Gain	dB		3.5	
IIP3	LNA Max Gain	dBm		-7.5	
	LNA Min Gain	dBm		+35	
Image Rejection		dBc		65	
Phase Noise	1K	dBc		-91	
	10K	dBc		-98	
	100K	dBc		-109	
CSO	110 Channel at 75dBuV	dBc		-67	
CTB		dBc		-65	
Multiple Crystal Frequency Spurious	Refer to RF-In	dBm		-120	
RF in to Loop through gain [1]		dB		0	
Loop through Return loss[1]		dB		-13	
Sensitivity	FFT:8k,QPSK,CR:1/2	dBm		-97.5	
	FFT:8k,16QAM,CR:1/2	dBm		-91.5	
	FFT:8k,64QAM,CR:3/4	dBm		-81.5	
Adjacent Channel Rejection	FFT:8k,64QAM,CR:7/8	dBm		-79.5	
	Analog Interference at DVB-T Signal	dBc		-47	
Max. Input Power	FFT:8k,64QAM,CR:7/8	dBm		+10	
IF Output Level	Swing	Vp-p		1	2
	Impedence		Differential 2kΩ//5pF		
PLL Locking time		ms			5

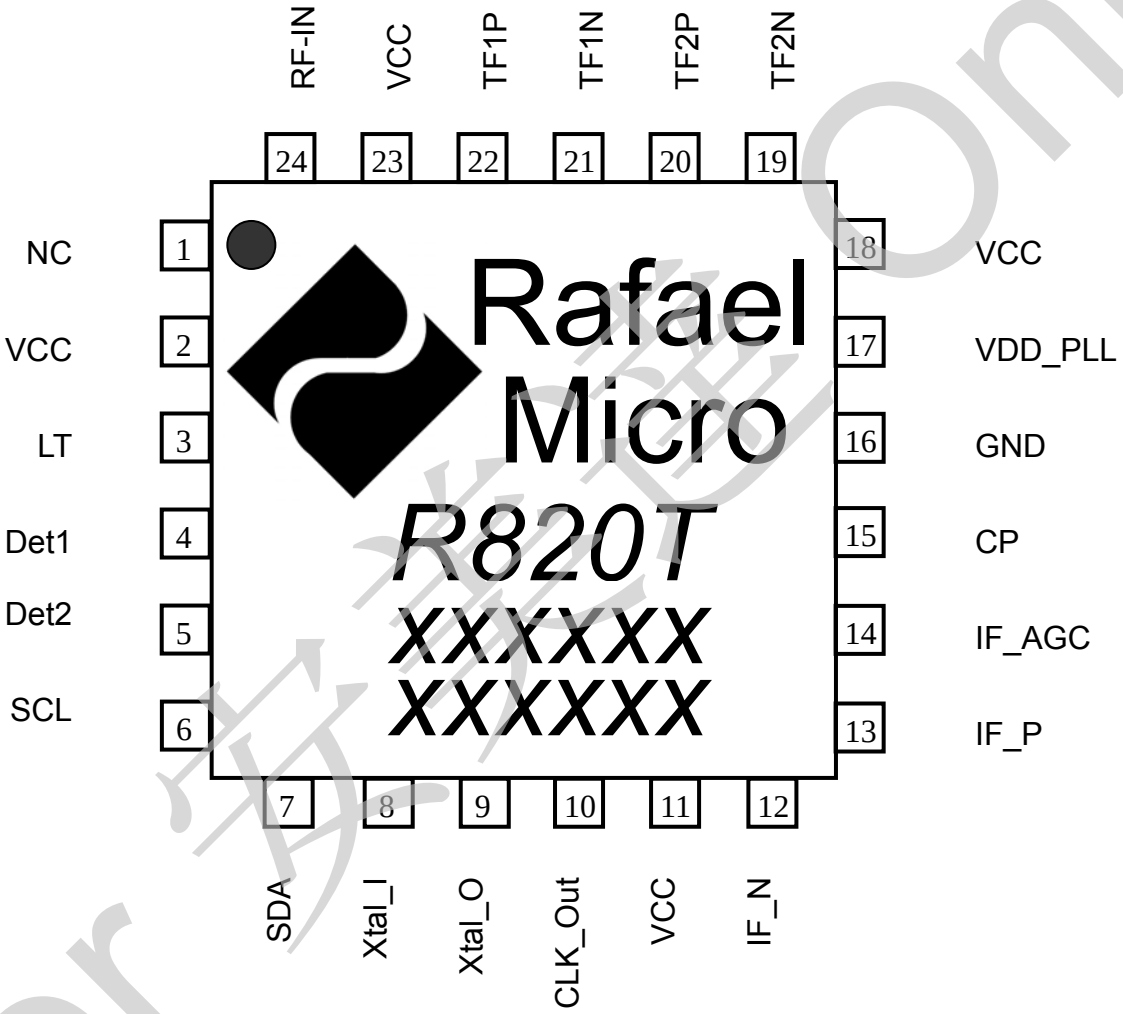
Notes:

1. Network Analyzer Measurement Power : -20dBm

2 Pin Description

Pin Allocation

Figure 2-1 : Pin Allocation (note: E-Pad is GND)



Pin Assignment

Table 2-1 : Summary List of Pin Assignment

Pin Number	Symbol	Description
24	**RF_In**	RF Input
1	**NC**	Not Connect
2,11,18,23	**VCC**	Tuner 3.3V voltage input
3	**LT**	Loop through output
4,5	**Detx**	Power detector decoupling capacitor
6	**SCL**	I2C bus, clock input
7	**SDA**	I2C bus, data input/ output
8	**Xtal_I**	Crystal oscillator Input
9	**Xtal_O**	Crystal oscillator Output
10	**CLK_Out**	Clock output for sharing Crystal oscillator
12	**IF_N**	IF output
13	**IF_P**	IF output
14	**IF_AGC**	IF automatic gain control input
15	**CP**	PLL charge pump
17	**VDD_PLL**	PLL 2V supply output decoupling
19,20,21,22	**TFxx**	Tracking filter, the detail as Figure 2-1: Pin Allocation.
16	**GND**	Ground
0	**GND**	Exposed pad

3 Programming and Registers

3.1 I2C Series Programming Interface

The programmable features of the R820T are accessible through an I2C compatible serial interface. Bi-directional data transfers are programmed through the serial clock (SCL) and serial data lines (SDA) at a standard clock rate of 100 KHz and up to 400KHz.

Data Transfer Logic

The I^2C control byte includes a fixed 7-bit slave address ID and a read/write (R/W) bit. Fixed I^2C slave address ID 0011010 (0x1A) is used for default setting. The R/W bit is set 0 for write and 1 for read (Table 3-1). Write mode and read mode will be further explained in the following sections.

I^2C Write/Read Address

Table 3-1 : I^2C Read / Write Address

I^2C Mode	I^2C Address(Bin)							R/W	Address (Hex)
	MSB						LSB		
Write Mode	0	0	1	1	0	1	0	0	0x34
Read Mode	0	0	1	1	0	1	0	1	0x35

Write Mode

When the slave address matches the I^2C device ID with write control bit , I^2C start interprets the following first byte as first written register address. These following bytes are all the register data (page write I^2C control). Register 0 to Register 4 are reserved for internal use only and can be written by I^2C write command.

Figure 3-1 : The Typical Write Mode Sequence

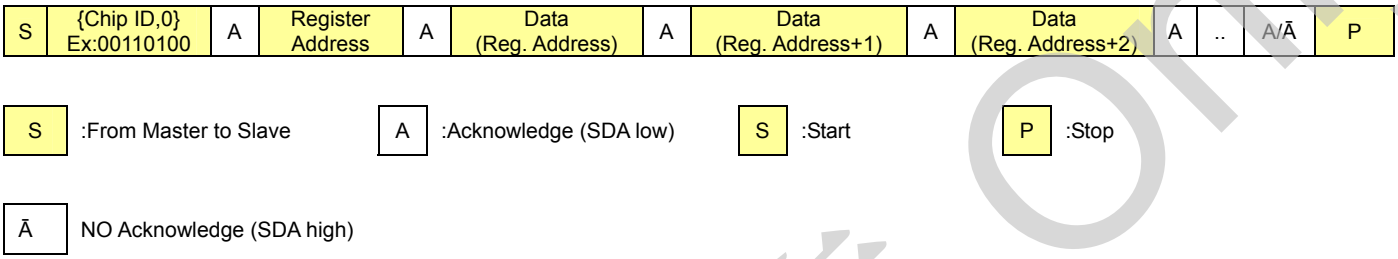
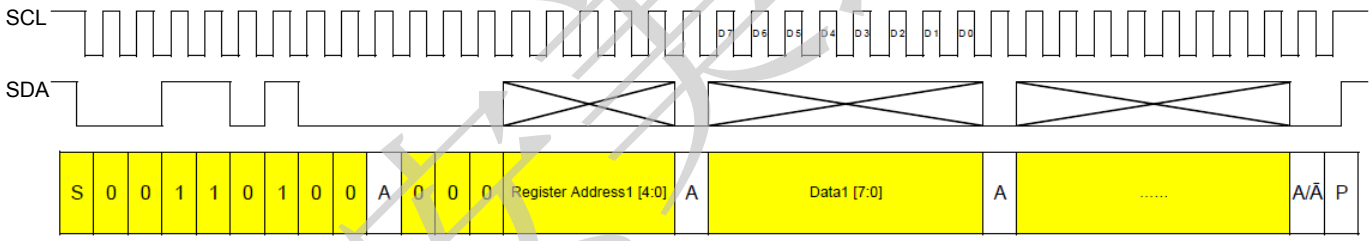


Figure 3-2 : An Example of Write Mode Procedure



Read Mode

When the slave address matches the I^2C device ID with read control bit, data are immediately transferred after ack command. Reading data transmission begins from core register 0 to final register until “P”(STOP) occurs. The data is transmitted from LSB to MSB, and the data of register 0 (0x96) is fixed as reference check point for read mode.

Figure 3-3 : The Typical Read Mode Sequence

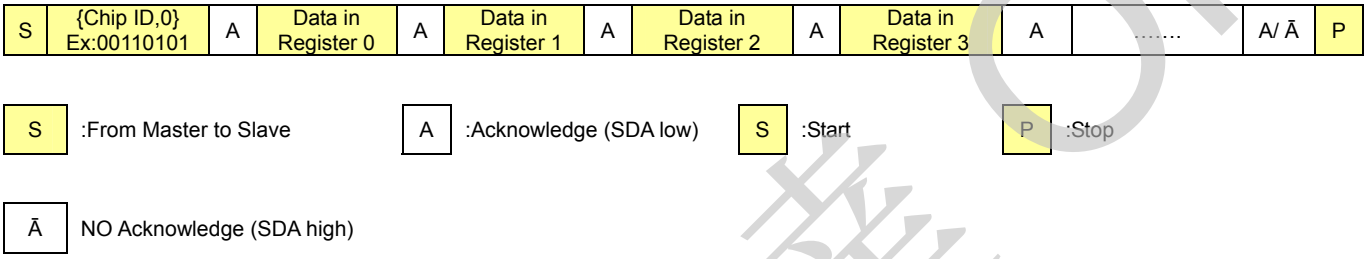
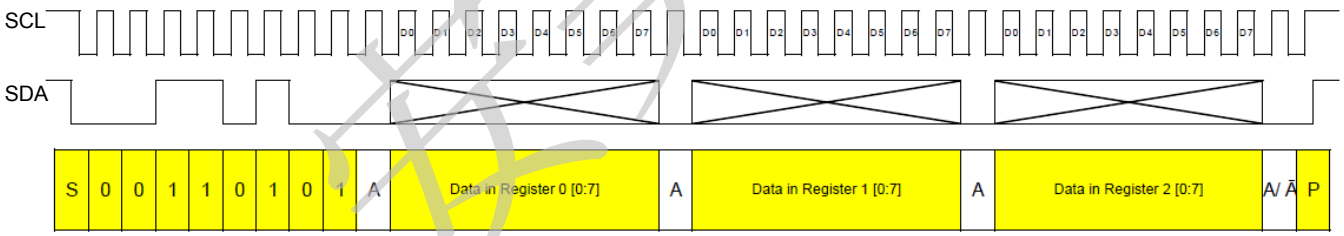


Figure 3-4 : An Example of Read Mode Procedure

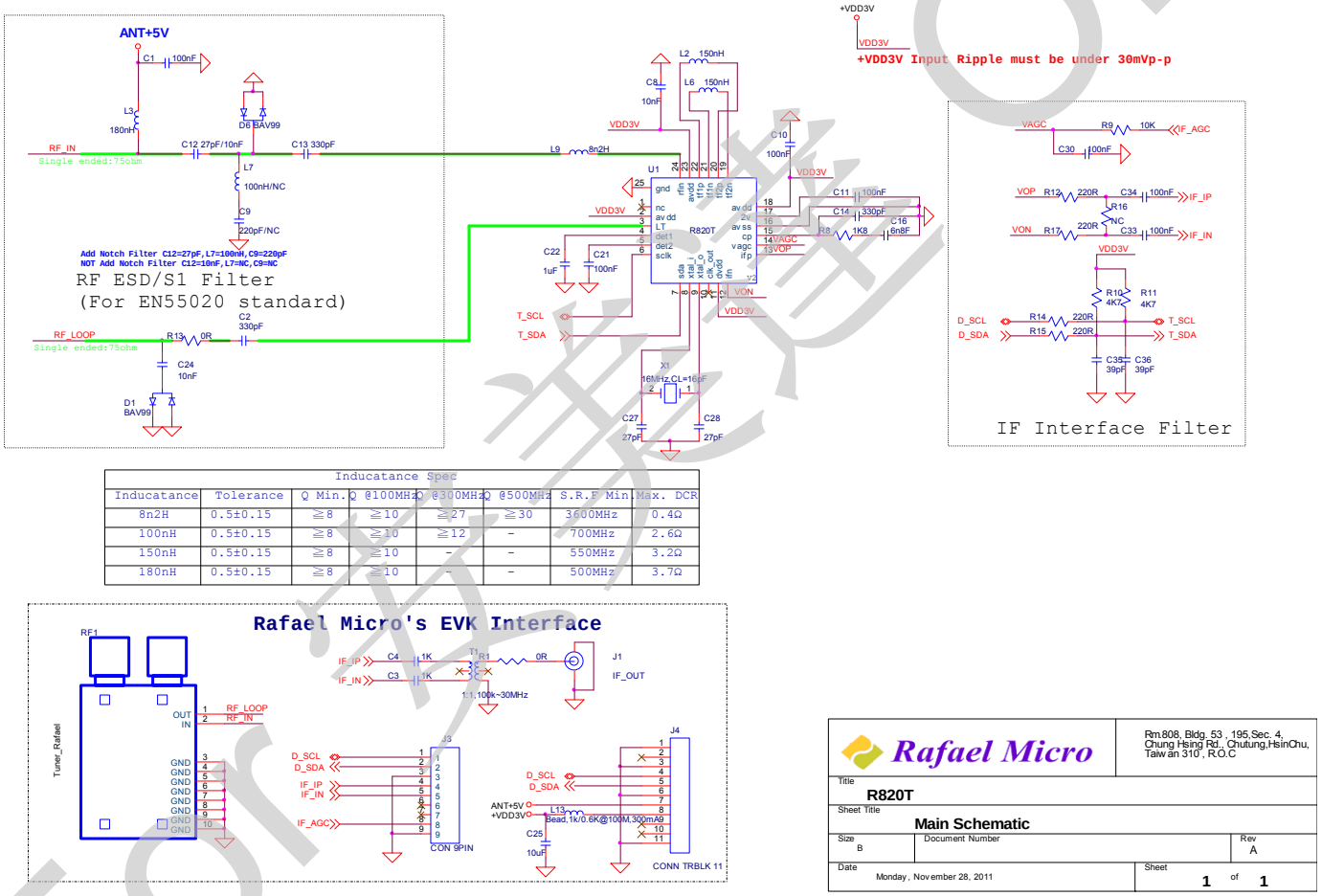


4 Application Information

4.1 Application Circuit

Please contact Rafael Micro System Integration Engineering for the detailed application circuit and BOM list. For different system applications, Rafael Micro provides customized engineering services to from reference design, RF layout, Gerber file, to PCB review. These engineering services are recognized as a great value to shorten time to market cycle.

Figure 4-1 : Reference Application Schematic



Inducatance Spec						
Inducatance	Tolerance	Q Min.	Q @100MHz	Q @300MHz	Q @500MHz	S.R.F Min.	Max. DCR
8n2H	0.5±0.15	≧8	≧10	≧27	≧30	3600MHz	0.4Ω
100nH	0.5±0.15	≧8	≧10	≧12	-	700MHz	2.6Ω
150nH	0.5±0.15	≧8	≧10	-	-	550MHz	3.2Ω
180nH	0.5±0.15	≧8	≧10	-	-	500MHz	3.7Ω

4.2 Application Notes

Please contact Rafael Micro Application Engineering for the detailed layout application note. The following guidelines together with proper implementation should be considered in board level layout to achieve the best performance.

1. To improve ESD/EOS reliability, RF input port and I2C bus needs an ESD protection circuit.
2. Minimize the RF trace from RF connector to device RF input pin..
3. RF traces should be protected with ground traces and guard rings.
4. Shielded connectors should be used with all shields connected to the ground plane with low impedance connections.
5. Minimize the ground path to device E-pad for the crystal.
6. Place crystal should be far away from RF traces.
7. Crystal traces should be protected with ground traces and guard rings.
8. The crystal amplifier oscillator has a dedicated power supply pin (Pin11), which should be carefully decoupled to ground with minimal lead lengths in order to minimize board noise from coupling into the reference clock.
9. System clocks and frequently switched signals should not be routed close to the crystal and RF trace.
10. Place AGC filter and CP filter circuits as close to the device as possible.
11. Minimize the CP filter ground path to device E-pad.
12. System digital traces should be routed away from RF traces.
13. Place ceramic DC bypass capacitors as close to the device as possible. This will insure that the power goes through the capacitors before power goes through the VIAs to the power plane
14. If possible power and ground should be on separate dedicated layers.

4.3 IF Frequency

R820T receives RF signal and feed through internal low-noise amplifier, power detector, band-pass filter, and image rejection filter. The mixer down-converts the RF signal to a low-IF frequency, which depends on channel bandwidth in different applications. The standard IF filters are implemented for 6/7/8 MHz channel bandwidths.

.

Table 4-1 : IF Frequency Table

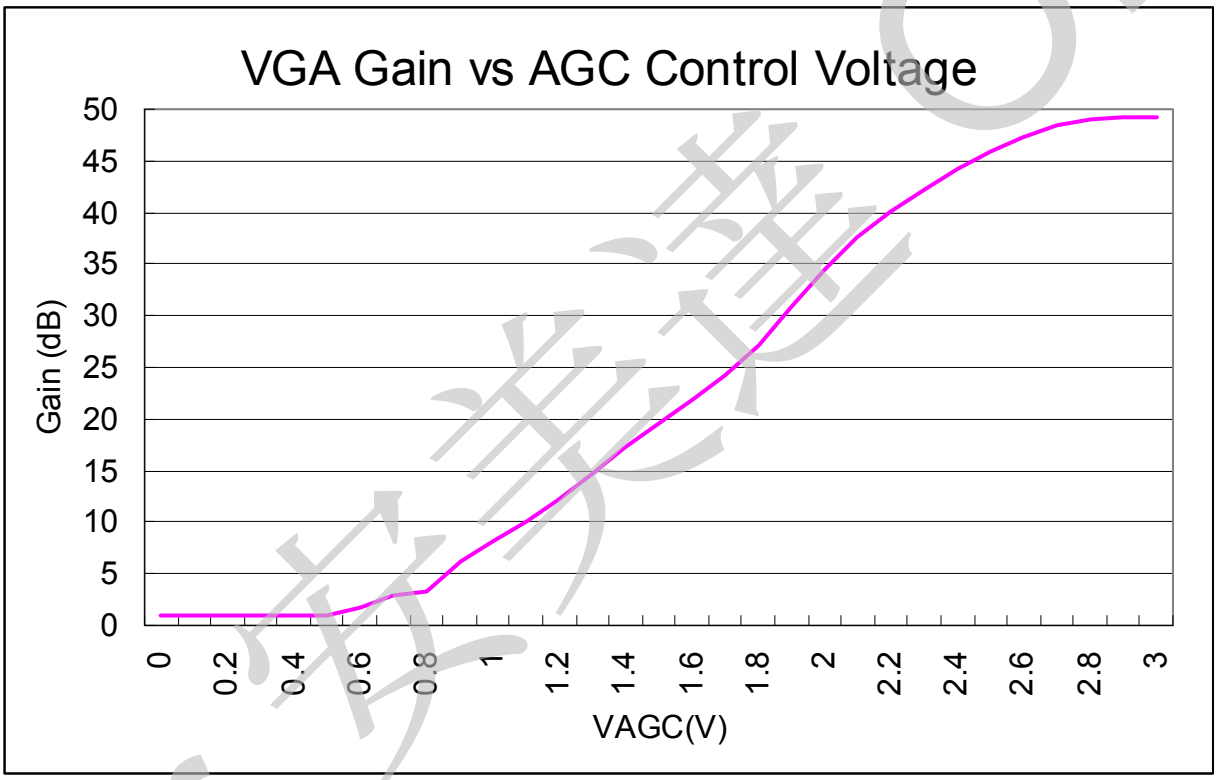
	TV Standard	Channel BW	Center Frequency
1	ATSC (Digital)	BW = 6MHz	Fcenter= 4.063MHz
2	DVB-T (Digital)	BW = 6MHz	Fcenter= 3.57MHz
3	DVB-T (Digital)	BW = 7MHz	Fcenter= 4.07MHz
4	DVB-T (Digital)	BW = 7MHz	Fcenter= 4.57MHz
5	DVB-T (Digital)	BW = 8MHz	Fcenter= 4.57MHz
7	ISDB-T (Digital)	BW = 6MHz	Fcenter = 4.063MHz
8	DTMB (Digital)	BW = 8MHz	Fcenter = 4.57MHz

4.4 AGC Control

The R820T has built-in RFAGC to achieve the optimal SNR while minimizing distortion. When RF input power increases, the internal power detector is activated to attenuate internal LNA gain in an optimal level. On another hand, when RF input power decreases, internal power detector will increase internal LNA gain to achieve good picture quality.

The IFVGA control is available for the demodulator to control the gain of output VGA. R820T provides a wide range of IFVGA gain from +1dB to +48dB. Demodulator AGC output voltage range from 0.6V to 2.5V.

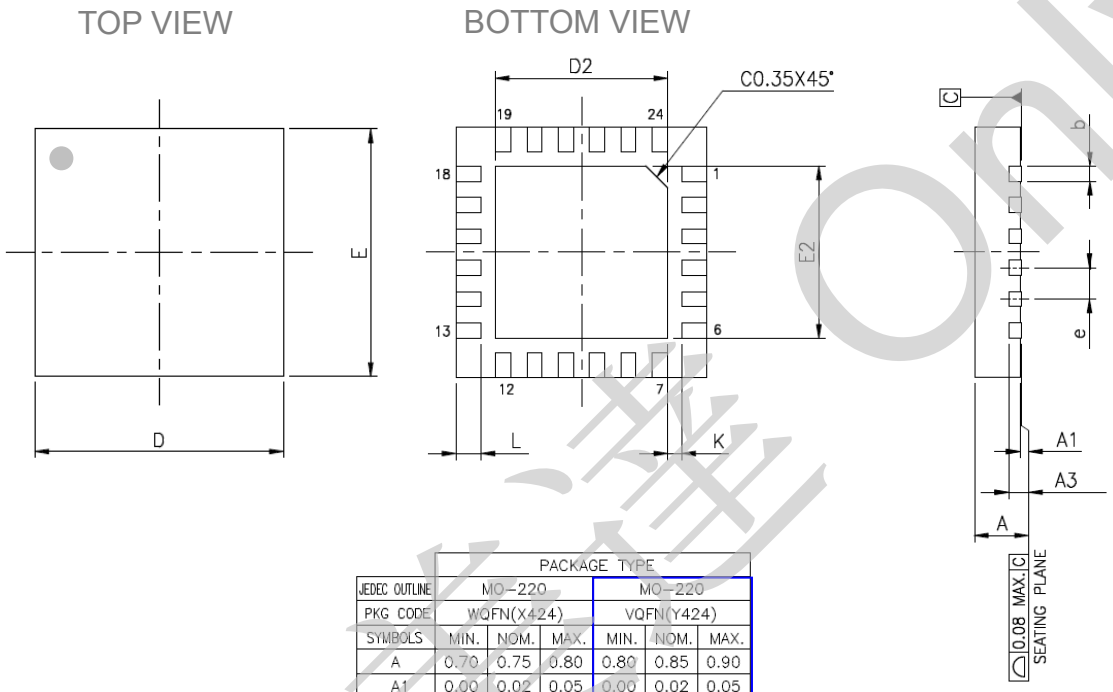
Figure 4-2 : VGA Gain vs AGC control Voltage



5 Package Dimensions and Outline

The R820T is packaged by a Lead-Free 4x4 24-pin Quad Flat No-Lead (QFN) package. The detail package dimensions are listed in Figure 5-1.

Figure 5-1 : Package Dimensions and Outline



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

		E2			D2			L			LEAD FINISH		JEDEC CODE
	PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
	112X112 MIL	2.15	2.25	2.30	2.15	2.25	2.30	0.35	0.40	0.45	V	X	W(V)GGD-8
	113X113 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.35	0.40	0.45	X	V	W(V)GGD-6
	114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
8	115X115 MIL	2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8
	120X120 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.275	0.325	0.375	V	X	W(V)GGD-8

Note:

Before soldering to system board, R820T need to be baked at 125°C for more than 8 hours to eliminate moisture contamination.

6 Crystal Requirements

6.1 Crystal Specifications

The default crystal frequency for R820T is 16 MHz. The R820T is well accompanied with traditional DIP package crystal. To reduce component count and font factor, a low profile SMD package crystal is recommended. Please contact Rafael Micro application engineering for other crystal frequencies (12, 20, 20.48, 24, 27, 28.8, 32 MHz) applications.

Table 6-1 : Crystal Specifications

Parameter	Min	Typical	Max	Units
Frequency Range		16		MHz
ESR			50	Ω
Frequency accuracy		± 30	± 50	ppm
Load Capacitor (CL)		16		pF
Input level to XTAL_P pin when using external clock	120		3300	mVp-p

6.2 Clock Output Swing

The R820T clock output swing is programmable through I2C interface. The IC provides a clock output signal in triangle waveform with output voltage typical at 2.0Vp-p. The output voltage specification assumes an off-chip load impedance of 16pF/ 10MΩ.

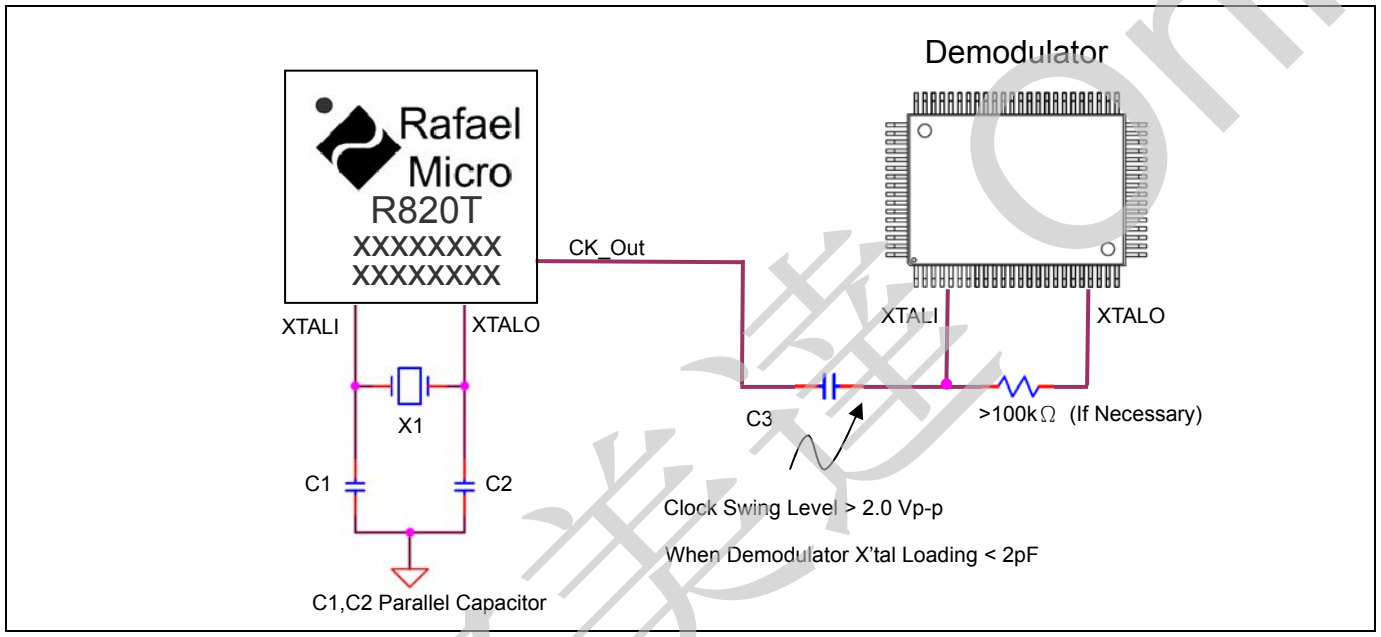
Table 6-2 : Clock Output Specifications

Parameter	Min	Typical	Max	Units
Clock Output Swing (16pF // 10MΩ)		2.0		Vp-p

6.3 Crystal Parallel Capacitors and Share Crystal

Crystal parallel capacitors are recommended when a default crystal frequency of 16 MHz is implemented. Please contact Rafael Micro application engineering for crystal parallel capacitors using other crystal frequencies. For cost sensitive project, the R820T can share crystal with backend demodulators or baseband ICs to reduce component count. The recommended reference design for crystal loading capacitors and share crystal is shown as below.

Figure 6-1 : Crystal Parallel Capacitors and Share Crystal



Note:

Crystal X1=16MHz/ CL=16pF

Bypass capacitor C3=10nF

Crystal parallel capacitors C1=C2=27pF

7 Hardware Tolerance Specifications

To achieve better RF performance, hardware tolerance for tracking filter inductors and RF input inductors is highly recommended in the R820T reference design..

Table 7-1 : Value and specification of Tracking filter inductors and RF input inductors
(Reference Figure 4-1: Reference Application Schematic)

Reference	L (nH)	Tolerance	Q Min.	L, Q test frequency	Q at 100 MHz	Q at 300 MHz	Q at 500 MHz	S.R.F. Min.	DCR Max.
L3,	180	0.5 +/- 0.15	8	100 MHz	10	-	-	500 MHz	3.7 ohm
L7	100	0.5 +/- 0.15	8	100 MHz	10	12	-	700 MHz	2.6 ohm
L2,L6	150	0.5 +/- 0.15	8	100 MHz	10	-	-	550 MHz	3.2 ohm
L9	8.2	0.5 +/- 0.15	8	100 MHz	10	27	30	3600MHz	0.4 ohm

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310 台灣新竹縣竹東鎮中興路四段 195 號 53 館 808 室
Tel: 886-3-5820868 Fax: 886-3-5820968
www.rafaelmicro.com