BK4815N

Analog Two Way Radio IC

Features

- World wide band: 128 ~ 590 MHz
- 12.5/25 kHz channel spacing
- On chip 5 dBm RF PA
- 3.0 V to 3.6 V power supply
- CTCSS tone receiver with up to parallel eight frequency detector
- 23/24 bit programmable DCS code
- Standard DTMF and programmable in-band dual tone
- SELCALL and programmable in-band single tone
- 1.2/2.4 kbps FSK data modem with either F2D or F1W modulation type
- Frequency inversion scrambler
- Voice activated switch (VOX) and time-out timer
- RF Signal strength measurement and signal quality measurement
- TX Audio signal strength indication and RX audio signal strength indication
- 3-wires interface with MCU with maximum 8 Mbps clock rate
- QFN 4x4 32-Pin package

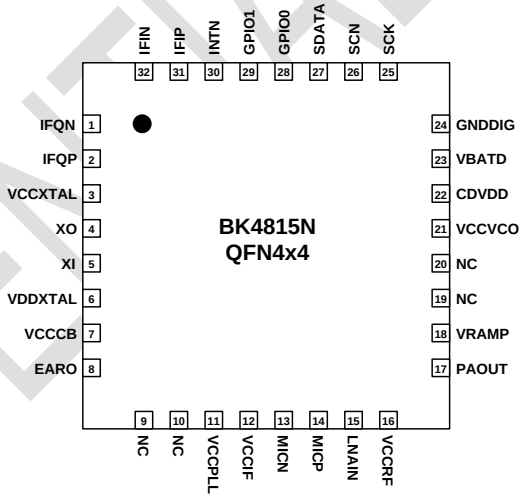
Applications

- Personal Radio Service
- Baby Monitor
- Toys

General Description

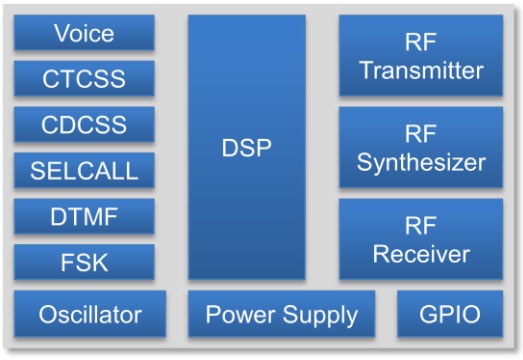
The BK4815N is a half duplex TDD FM transceiver operating from 124 MHz to 560 MHz band for worldwide personal radio. Besides speech communication, the BK4815N on-chip FSK data modem supports F2D and F1W emission to be used in both FRS and DPMR band for text message and GPS information exchange.

The BK4815N is a complete, small form factor solution optimized for low-power, low-cost, and highly integrated mobile and portable consumer electronic devices, requiring only a few external decoupling capacitors and an external inductor for input matching.



QFN 32 Pin Assignments (Top View)

Functional Block Diagram



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1 Functional Description

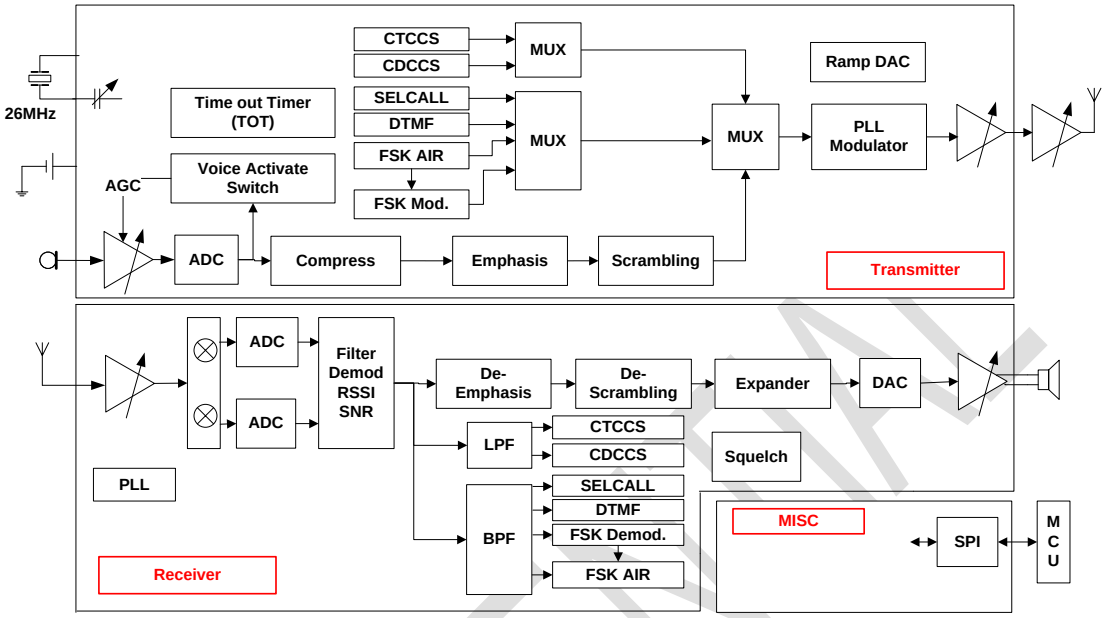

Figure 1. Functional Block Diagram

1.1 Overview

The BK4815N integrates high performance PLL, ADC, DAC, and advanced digital signal processing capability on a single chip. The digital low-IF image rejection architecture enables it to work with a very simple MCU as a two way radio communication system. On-chip flexible and precise continuous and discrete tone generator and detector enable a secure link and digital signaling.

1.2 RF Transceiver

BK4815N includes an integrated RF transceiver which is compliant with the specification most country in the world. The RF transceiver requires the following external components to operate:

1) A 26MHz crystal;
2) Simple input matching and output matching;
3) Several SMD capacitors for decoupling and DC blocking.

1.2.1 FM Receiver

The receiver implements a low-IF image rejection architecture, which is composed with two parts: RF front-end and IF part. The RF front-end comprises a LNA and a quadrature mixer. The IF part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a high precision analog-to-

digital converter(ADC). The block diagram of the FM receiver is shown in Figure 2.

At the RF front-end part, the LNA is a differential low-noise amplifier with single-ended input. The LNA is followed by a quadrature mixer that down-converts the RF signal directly to IF signal. Low-IF image rejection architecture is implemented in order to eliminate the external SAW filters. The value of IF frequency(f_{IF}) can be programmed either 88kHz or 137kHz through 3-wire SPI interface(*REG13[0]*). The RF front-end part can be power up by set *REG12[14]* to 0.

At the IF part, the down-converted in-phase IF signal (IF/I) and quadrature-phase IF signal(IF/Q)are first filtered by the BPF, and then amplified by the VGA. The VGA provides variable gain with 21dB dynamic range, and could be controlled through3-wire SPI interface(*REG103[6:4]*).The Sigma-Delta ADC sample analog IF signal from VGA, and convert it to digital IF signal. Then the digital signal will be send to DSP for second down-conversion and audio processing. The IF part can be power up by set *REG12[13]* to 0.

To avoid serious distortion with high-level input power, AGC function is added to automatically adjust the gain of LNA and the gain of VGA. AGC function can be enabled by set *REG103[15]* to 0.

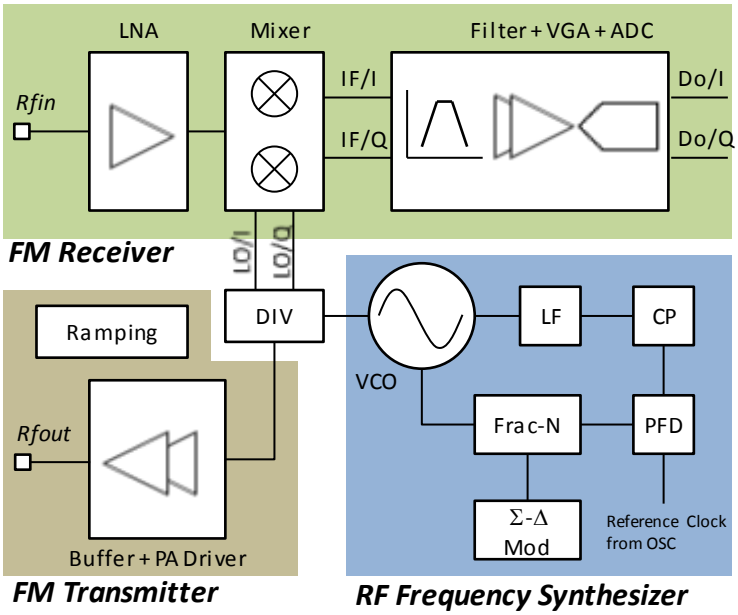

Figure 2. Radio Block Diagram

1.2.2 FM Transmitter

The transmitter is a single-ended amplifier including a buffer, a PA driver and a ramping-control block. The block diagram of the transmitter is shown in Figure 2. Due to FM modulation is of constant envelope, the amplifier works in saturated mode to save current consumption.

A ramping-control block is implemented to avoid unwanted spurious signals when the transmitter is power up. Ramping function can be enabled by set *REG109[12]* to 1. If ramping function is enabled, a ramping table should be filled by writing ramp values into *REG42* in turn. The best ramping curve is raised cosine.

The output power of FM transmitter can be programmed from -20dBm to +5dBm through 3-wire SPI interface(*REG109[15:13]*).

The transmitter can be power up by set *REG12[9]* to 0.

1.2.3 RF Frequency Synthesizer

An RF synthesizer is implemented to generate local oscillator(LO) signals. It includes a voltage controlled oscillator(VCO), a fractional-N divider(frac-N), a phase-frequency detector(PFD), a charge pump(CP) and a loop filter(LF). The RF synthesizer is shared for RX mode and TX mode. The block diagram of the synthesizer is shown in Figure 2.

In RX mode, the RF frequency synthesizer generates unmodulated LO signal. And the unmodulated LO signal is then divided by an integer N_{div} for down-conversion mixer in the FM receiver. In TX mode, FM modulation is realized in the RF frequency synthesizer. Modulated VCO output is divided by an integer N_{div}. The value of N_{div} can be programmed to 8/12/16/24 through 3-wire SPI interface(*REG4[8:7]*).

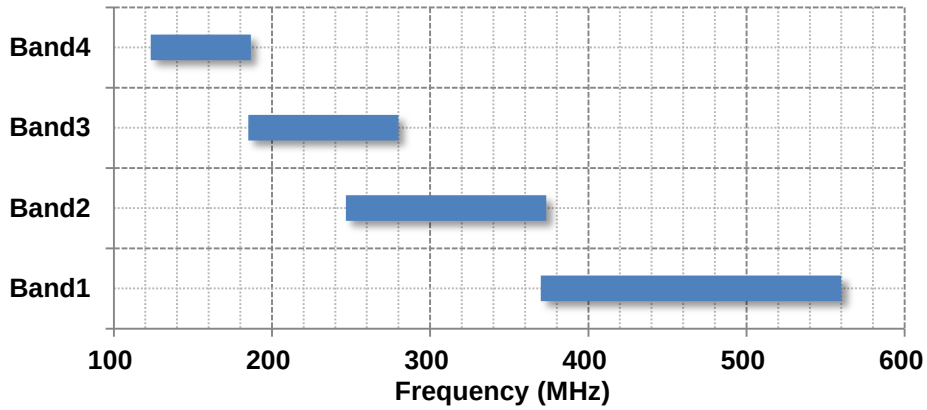

Figure 3. Frequency Cover Range of RF Synthesizer

In RX mode, the locked frequency of the synthesizer is equal to N_{div} x (f_{wanted}-f_{IF}). While in TX mode, the locked frequency of the synthesizer is equal to N_{div} x f_{wanted}.

Channel selection is also implemented by programming the value of fraction-N through 3-wire SPI interface (*REG113/REG114*). On power up or channel reselection, the synthesizer takes less than 0.3m sec to settle.

For BK4815N, the default crystal is 26MHz. The frequency tolerance of the crystal should be within ±2.5ppm to keep a reliable communication.

The synthesizer can be power up by set *REG12[8]* to 0.

1.2.4 Input/output Matching

Since the LNA input and the PA output are of single-ended, external balun is not necessary. Both the input matching and the output matching can be implemented using low-cost discrete inductors and capacitors. The schematic of input/output matching is shown in Figure 4.

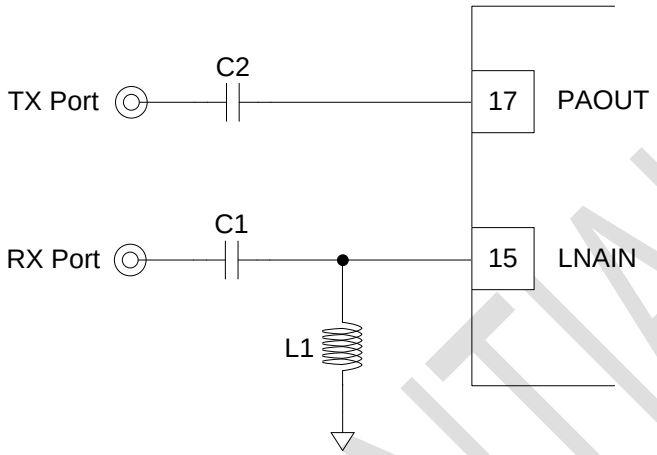

Figure 4. Schematic of Input/Output matching

As for input matching, capacitor C1 is used for DC-blocking. The recommended value of C1 is 4.7pF. The DC voltage at PIN15 is about 0V in RX mode. Inductor L1 is used for impedance transformation. The recommended value of L1 is 47nH for 409.75MHz band, and is 33nH for 446.00625MHz/462.5625MHz band.

As for output matching, capacitor C2 is used for DC-blocking, too.

1.2.5 Crystal Oscillator

BK4815N integrates a low-power amplitude-regulated 26MHz crystal oscillator. The 26MHz crystal oscillator not only provides the reference frequency for the RF synthesizer, but also provides clock for digital part. The circuit diagram of the 26MHz crystal oscillator is shown in Figure 5.

The 26 MHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal datasheet. Figure 5 on next page shows how the crystal is connected to the 26 MHz crystal oscillator. C1 and C2 are ceramic SMD (Surface Mount Device) capacitors connected between each crystal terminal and ground. Cvar is an adjustable capacitor for frequency calibration.

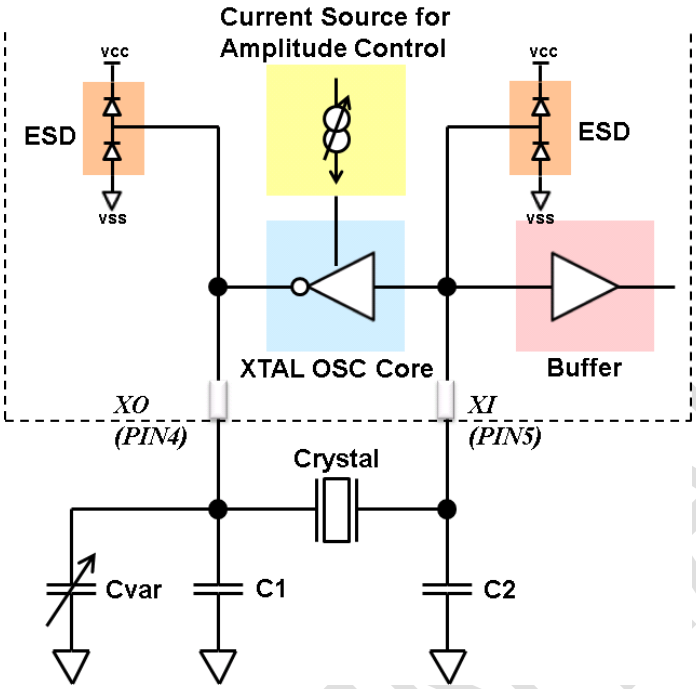

Figure 5. Circuit Diagram of the 26MHz Crystal Oscillator

$$C_{load} = \frac{C_1' \times C_2'}{C_1' + C_2'}$$
$$C_1' = C_1 + C_{var} + C_{par}$$
$$C_2' = C_2 + C_{par}$$

in which, Cpar is parasitic capacitance including PCB trace capacitance and pin input capacitance. The value of Cpar is about 1pF.

The 26MHz crystal oscillator can be power up by set *REG12[6]* to 0.

1.2.6 On-chip Voltage Regulator Decoupling

BK4815N contains 2 low-dropout regulators (LDO):

1) One LDO for XTAL oscillator in FM receiver. This LDO needs an external SMD capacitor to reduce noise on power supply for better noise figure. The output voltage of this LDO is about 1.2V, and the typical value of this SMD capacitor is 100nF.
2) One LDO for digital part. This LDO needs an external SMD capacitor to reduce spurious signal from digital part. The output voltage of this LDO is about 1.2V, and the value of this SMD capacitor should be no less than 1uF.

The configuration of these 2 LDOs is shown in Figure 6.

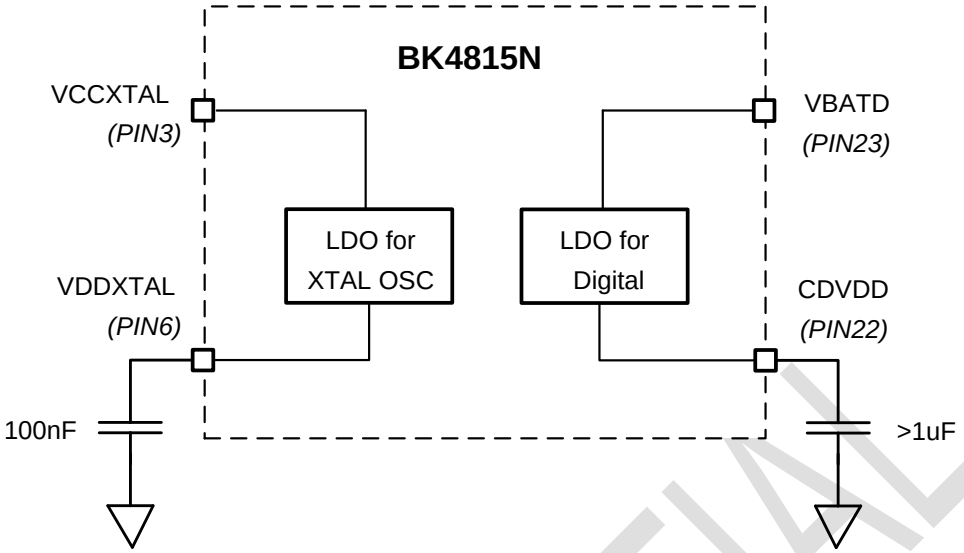

Figure 6. Configuration of Low-dropout Regulators

1.2.7 Power Supply Decoupling

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application.

1.3 TX Baseband

1.3.1 Audio

TX audio path has the following blocks:

1) Digital AGC to automatically adjust microphone gain (*REG44, REG45*) before ADC;
2) Digital compressor to extent signal dynamic range (*REG17*);
3) Volume control with 1 dB step from -25 dB to 6 dB (*REG18*);
4) Optional pre-emphasis filter, 0 dB at 1 kHz and +6 dB per octave (REG18);
5) Audio scrambling with programmable scrambling frequency (REG20);
6) 300 Hz high pass filter to avoid interference to sub-audible signal, which has 30 dB attenuation for frequency below 250 Hz with respect to signal at 1 kHz (*REG18*);
7) Low pass filter with typical 3 kHz corner (*REG18*);
8) Limiter to avoid unwanted out-of-band emission (*REG19*);
9) Flexible block execution order (*REG18*).

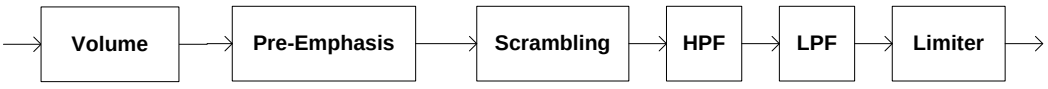

Figure 7. TX Audio Block Diagram

The microphone gain can be control through *REG44* and *REG45*.

When AGC is enabled, the microphone gain is automatically controlled by internal AGC algorithm. At this scenario, the real time microphone gain setting can be read by *REG21[5:0]*. Combined with the real time microphone gain (*REG21 [5:0]*) and the digital detected microphone signal level (*REG21*), the absolute microphone signal level at microphone input can be calculated, but please note the *REG21[15:8]* and *REG21[5:0]* have difference unit.

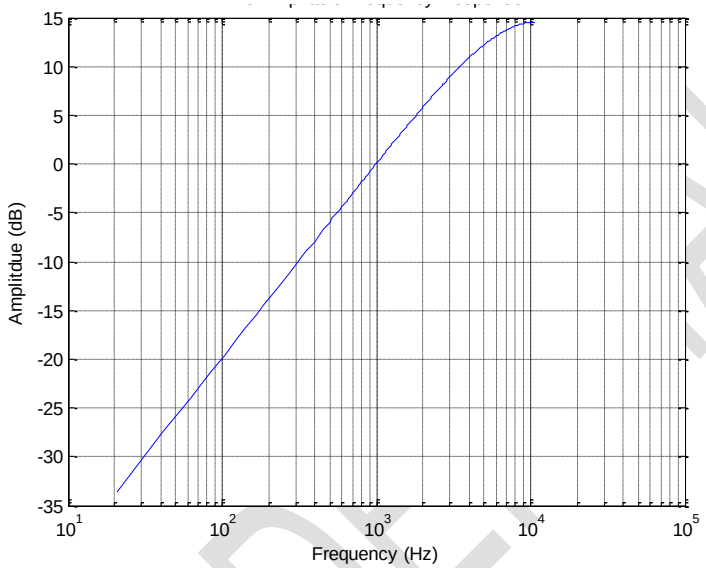

Figure 8. Frequency Response of Pre-emphasis Filter

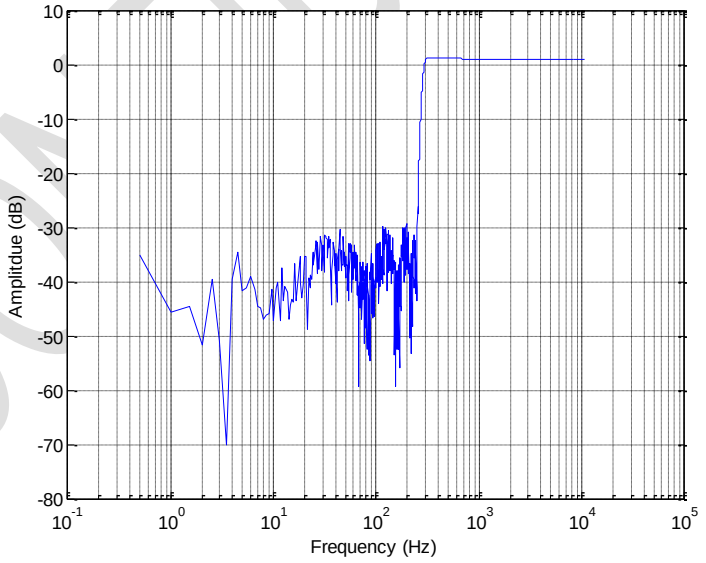

Figure 9. Frequency Response of 300Hz High Pass Filter

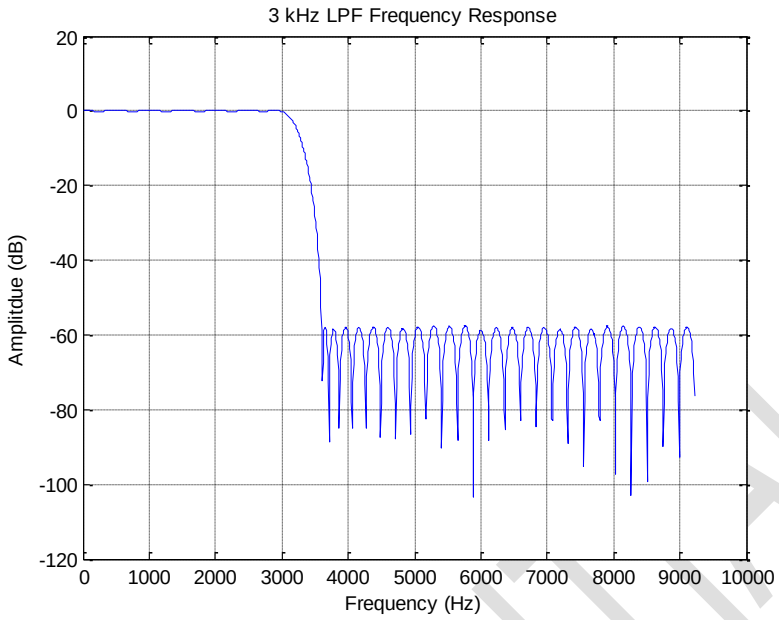

Figure 10. Frequency Response of Low Pass Filter

1.3.2 VOX

Voice activated switch (VOX) detects the received audio signal level (*REG21[7:0]*) and microphone PGA gain (*REG21[5:0]*). If the received audio signal level is greater than a programmable threshold (*REG22[13:6]*) and the microphone PGA gain is greater than a programmable threshold (*REG22[5:0]*), and this status last for 128 samples, the VOX will output 1 and the VOX interrupt bit will be set (*REG116*). VOX can be enabled by set *REG22[15]* to 1.

1.3.3 In-band Signaling

There are three types of in-band signaling: DTMF, SELCALL, and FSK (and FSK_AIR). Together with audio signal, they are total of four kinds of in-band signaling, of which only one can be sent at a time (*REG40*). The deviation of in-band signaling is programmable (*REG40*).

1.3.3.1 DTMF

DTMF is a dual tone signaling, it has programmable high band and low band frequency. The high band frequency can be programmable from 1209 Hz to 1633 Hz (*REG25*). The low band frequency can be programmable from 697 Hz to 941 Hz (*REG24*). The twist can be programmable from 0 to 15 dB with 1 dB resolution (*REG26*). The suggested DTMF tone table is given below.

Table 1. Standard DTMF Table

DTMF Symbol		High Frequency (Hz)			
		1209	1336	1477	1633
Low Frequency (Hz)	697	1	2	3	A
	770	4	5	6	B
	852	7	8	9	C
	941	E	0	F	D

1.3.3.2 FSK

FSK is a high data rate signaling, which supports 1200 bps data mode at 12.5 kHz channel spacing and 2400 bps data mode at 25 kHz channel spacing. The frame structure of the data package is given below.

Pre-amble	Sync Word	Addr	Type	Size	CRC A	Payload	CRCB
16 bit	16 bit	Byte0	Byte1	Byte2	Byte3	0-127 Word	2/4 Byte

Figure 11. Frame Structure of Data Mode

User can write head field including Address/Type/Size/CRCA and the corresponding payload (*REG28, REG30*), and it will automatically calculate the CRC and packetize the data. Optional scrambling can be added to Address and subsequent bytes, and the scrambling seed is programmable (*REG32*).

Data receiver will automatically finish synchronization and data extraction that Address/Type/Size/CRCA and Payload can be read out through MCU interface.

The final over the air data package type can be setting with Type byte.

1) Type 0: Only head, no payload
2) Type 1: Head with payload
3) Type 2: Head with FEC encoded payload
4) Type 3: Head with FEC and interleaved encoded payload
5) Type 4: Free format that no automatic CRC insertion, CRCA is a user writable byte

The payload write is through an 8 words (1 word = 2 bytes) FIFO, if the word number in FIFO is shorter than a threshold that a write operation requires, it will give an interrupt to MCU that MCU must refill the FIFO (REG31).

Note: if use type 3, the number of payload is restricted. The allowed payload number is either odd number less than 8 or even number greater than 9. Payload number 8 and 9 is not allowed for type 3.

The FSK packet can be transmitted either directly through FM modulation (FSK AIR) for DPMR band or with a MSK modulated sub-carrier (FSK modem) then to FM modulation for FRS band.

1.3.3.3 SELCALL

SELCALL is a single tone signaling, the frequency can be programmable from 400 Hz to 3000 Hz (*REG34*). To get high sensitivity the suggested tone frequency (EIA frequency group) is given below.

Table 2. EIA single tone frequency setting

Tone Number	0	1	2	3	4	5	6	7
Tone Frequency (Hz)	600	741	882	1023	1164	1305	1446	1587
Tone Number	8	9	A	B	C	D	E	F
Tone Frequency (Hz)	1728	1869	2151	2435	2010	2295	495	No Tone

1.3.4 Sub-audible Signaling

Sub-audible signaling includes both CTCSS and CDCSS. For CTCSS, the frequency is programmable with 18 bit resolution, and it can be set to have a 0/120/180 degree phase shift. For CDCSS, it supports user programmable 23/24 bits CDCSS code(*REG1[12], REG38, REG39*), and the transmitted CDCSS code can be inversed.

Table 3. Reference CTCSS Frequency

Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
67.0	**85.4**	**103.5**	**127.3**	**156.7**	**192.8**	**241.8**
71.9	**88.5**	**107.2**	**131.8**	**162.2**	**203.5**	**250.3**
74.4	**91.5**	**110.9**	**136.5**	**167.9**	**210.7**	
77.0	**94.8**	**114.8**	**141.3**	**173.8**	**218.1**	
79.7	**97.4**	**118.8**	**146.2**	**179.9**	**225.7**	
82.5	**100.0**	**123.0**	**151.4**	**186.2**	**233.6**	
Non-Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
62.5	**69.3**	**183.5**	**196.6**	**206.5**		
64.7	**159.8**	**189.9**	**199.5**	**229.1**		

1.4 RX Baseband

The RX baseband output is the FM demodulator output, whose amplitude can be scaled (*REG66*), and subsequent filter coefficient is selected according to the in-band signal type (*REG66*) and sub-audible signal type (*REG66*).

1.4.1 Audio

Audio path has blocks below.

1) De-emphasis filter, 0 dB at 1 kHz and -6 dB per octave (*REG72*);
2) Audio de-scrambling with programmable scrambling frequency (*REG72*);
3) Low pass filter with 1.5 kHz corner (*REG65[15:14]* = 3) or 3.1 kHz corner (*REG65[15:14]* = 2);
4) 15 dB volume control range with 1 dB per step (*REG73[3:0]*);
5) Hard mute or soft mute control based on receive signal quality (*REG73*);
6) Flexible block execution order (*REG72*);

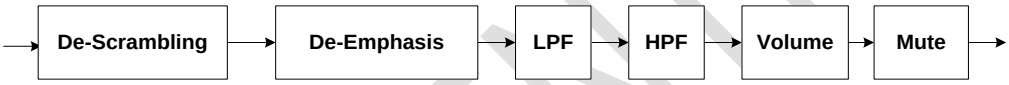

Figure 12. TX Audio Block Diagram

The RX signal strength before volume control module can be read out through REG74.

1.4.2 In-band Signaling

1.4.2.1 DTMF

DTMF decoder can detect up to 16 DTMF symbols simultaneously (*REG78*). High band tone frequency and low band tone frequency of each symbol can be programmed individually (*REG77*). When the decoder finds a symbol match, it will set corresponding bit and the found symbol address (*REG78*), and an interrupt will be issued.

1.4.2.2 FSK

In FSK AIR mode, the slicer output of FM demodulator will be FSK symbol. In FSK mode, the FM demodulator output is taken as a sub-carrier, and will be demodulated with a FSK demodulator.

FSK receiver will search the sync word to establish synchronization with FSK transmitter. When it is synchronized and CRCA check is passed, a FSK head received interrupt (*REG116*) will be issued and it will continue to receive the payload. The payload data will be written to an 8 words FIFO, and when the data word number in FIFO is greater than a threshold that the FIFO needs to read out, it will issue an interrupt (*REG116*) and MCU should read out all data bytes in FIFO immediately (*REG82, REG83*). After all payload of one packet is received, the CRCB check result will be set (*REG83*) and a receive-finished interrupt will be issued to MCU that MCU should check this bit to

know whether the read out payload is valid or invalid that should be discarded.

Note: With free format type (type 4), the “ FSK head received interrupt” will be given out immediately when it found the sync word , thus, this interrupt is earlier than that in other mode.

1.4.2.3 SELCALL

SELCALL decoder can detect up to 16 SELCALL symbols simultaneously (*REG87*). Frequency of each symbol can be programmed individually (*REG86*). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (*REG87*), and an interrupt will be issued.

There is an optional high pass filter to filter out signal below 400 Hz (*REG87*), and user can bypass this filter to receive SELCALL symbol with frequency below 400 Hz.

1.4.3 Sub-audible Signaling

CTCSS decoder can detect up to 8 CTCSS symbols simultaneously (*REG92*). Frequency of each symbol can be programmed individually (*REG91*). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (*REG92*), and an interrupt will be issued.

REG89 [15:4] to 0xFF8 can improve the sensitivity and stability, at the cost of much longer response time. In practical use, user can set the *REG89 [15:4]* small to improve the response time, and after the CTCSS is found, user can change it to be larger to avoid link lose. It applies same for the *REG90* where user can set the margin smaller initially and set them larger after the tone is found.

CTCSS decoder has an optional high pass filter to filter out DC signal (*REG92*), which can be used to get better RF frequency offset and low frequency noise immunity.

The CTCSS can detect 120/180 degree phase shift (*REG93*).

CDCSS decoder uses the same setting as CDCSS encoder, and has also an optional DC block filter (*REG94*). It can recognize the CDCSS code is exactly same or inversed (*REG93*).

1.5 SPI Interface

The BK4815N has 3-wires SPI interferace. These 3 wires are SCK(*PIN25*), $\overline{\text{SCN}}$(*PIN26*), SDATA(*PIN27*) for data exchange. SCK and $\overline{\text{SCN}}$ are input pins, while SDATA is bi-direction pin.

BK4815N always latch data at the SCK rising edge and output its data at SCK falling edge.

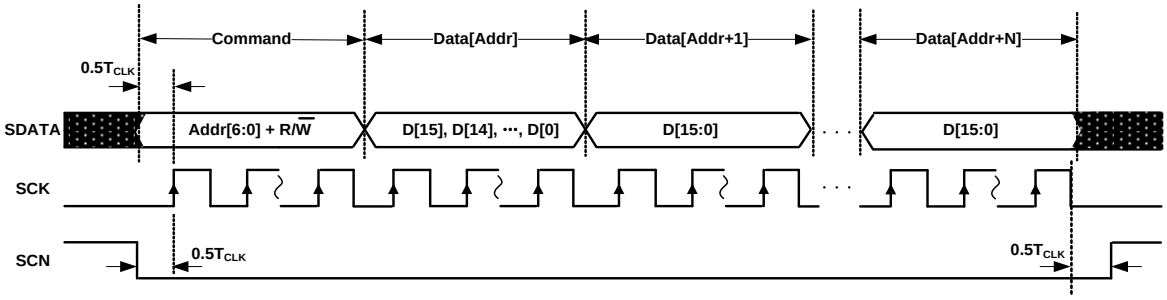

Figure 13. Three-wires Interface Timing

1.6 Power Management

Table 4. Power Control for Different Operational States

Blocks	Control Register	TX	RX	Idle
Digital Supply	REG12[2]	0	0	1
RC Calibration	REG12[3]	0	0	1
Central Bias	REG12[4]	0	0	1
BB DAC	REG12[5]	1	0	1
XTAL Oscillator	REG12[6]	0	0	1
Supply for Synthesizer	REG12[7]	1	0	1
RF Synthesizer	REG12[8]	0	0	1
PA Driver	REG12[9]	0	1	1
TX Audio	REG12[10]	0	1	1
RX Audio	REG12[11]	1	0	1
RX ADC	REG12[12]	1	0	1
RX IF	REG12[13]	1	0	1
RX Front-end	REG12[14]	1	0	1
RX Bias	REG12[15]	1	0	1
Digital State	REG112[14]	1	0	0
Digital Clock Enable	REG112[15]	1	1	0
Current		52 mA	60 mA	8 uA

When switching from TX or RX mode to idle mode, register should be update in order of *REG12*, and *REG112*. Please refer to the application note for detailed operation.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which BK4815N can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect BK4815N's reliability. Table 5 specifies the absolute maximum ratings for BK4815N.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-0.3	—	+3.6	V
I/O pin voltage	V_{IO}	-0.3	—	V_{DD}+0.3	V
Storage Temperature	T_S	–20	25	85	°C

2.2 Recommended Operating Conditions

The operating conditions are the physical parameters that BK4815N can operate within. The operating conditions for BK4815N are defined in Table 6.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	—	3.6	V
Operating Temperature	T_O	–10	25	60	°C

Notes:
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD}=3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
For QFN4x4 24pin package, VDD range is 2.6-3.6V.
The range of operating temperature mainly depends on the specification of the crystal. The frequency tolerance of the crystal should be within +/-2.5ppm during all operating conditions.

2.3 Power Consumption Specification

Table 7. Power Consumption Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current (RX Mode)	I_{RX}	REG12=0x0603 REG112=0xA000	—	60	—	mA
Supply Current (TX Mode)	I_{TX}	REG12=0xF823 REG112=0xE000	—	52	—	mA
Power Down Current	I_{PD}	REG7=0xFFFF REG112[15]=0	—	8	—	μA

2.4 Receiver Characteristics

Table 8. Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Frequency	F_{OP}	1	383	—	590	MHz
		2	255	—	394	
		3	192	—	295	
		4	128	—	197	
Sensitivity	RXSENS	5, 8, 9	-124	-123	-122	dBm
Adjacent Channel Selectivity	ACS	6, 8	63	64	65	dB
Blocking	BLK	7, 8	81	82	84	dB
Inter-modulation	IMD	8	61	62	63	dB
Audio						
Earpiece output level	EARO	9		146		mVrms
SINAD	ASNR	9,10		37		dB
Amplitude response	ARES		-3		3	dB
Audio noise floor	ANF			-81		dBm
CTCSS						
CTCSS sensitivity	CTSEN			-121		dBm
CTCSS response time	CTRES		75		125	ms
Frequency range	SAF		62.5		250.3	Hz
DCS						
CDCSS sensitivity	CDSEN			-122		
CDCSS response time	CDRES			171		ms
Code length	CLEN		23		24	Bit
Bit rate	BRATE			134.4		Hz
SELCALL						
SELCALL sensitivity	SELSEN			-121		dBm
SELCALL response time	SELRES			30		ms
Frequency range	IBSF		400		3000	Hz
DTMF						
DTMF sensitivity	DTSEN			-122		dBm
DTMF response time	DTRES			20		ms
High band frequency range	FH		1209		1633	Hz
Low band frequency range	FL		697		941	Hz
FSK data modem (F3E and F2D)						
FSK sensitivity (1E-3 BER)	FSKSEN			-122		dBm
FSK Best PER (32 bytes payload)	FSKBEST			0.1	1	%
Over the air data rate	BAUD		1200		2400	bps

Test Condition:
1. Band 1 (REG4[8:7]=0x0)
2. Band 2 (REG4[8:7]=0x2)
3. Band 3 (REG4[8:7]=0x1)
4. Band 3 (REG4[8:7]=0x3)
5. 12 dB SINAD
6. 1st adjacent channel (±12.5kHz)
7. Frequency offset > 1MHz
8. According to ETSI standard (EN 300 296-1 V1.4.1)
9. 1kHz tone, 1.5kHz deviation
10. -50dBm input power

2.5 Transmitter Characteristics

Table 9. Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Frequency	F_{OP}	1	383	—	590	MHz
		2	255	—	394	
		3	192	—	295	
		4	128	—	197	
Output Power	POUT	5	-20	0	5	dBm
Adjacent Channel Power Rejection	ACPR 1st		67	68	69	dBc
Alternate Channel Power Rejection	ACPR 2nd		70	72	73	dBc
Microphone Sensitivity	MICSENS	6		9		mV
SINAD	TSINAD	7		49		dB

Test Condition:
1. Band 1 (REG4[8:7]=0x0)
2. Band 2 (REG4[8:7]=0x2)
3. Band 3 (REG4[8:7]=0x1)
4. Band 3 (REG4[8:7]=0x3)
5. Depend on output matching and register settings
6. 1.5kHz deviation
7. At sensitivity level

2.6 SPI Control Interface Characteristics

Table 10. SPI Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	8	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, SEN to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
SEN Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, SEN, SDIO, Rise/Fall Time	t_R , t_F		—	—	10	ns

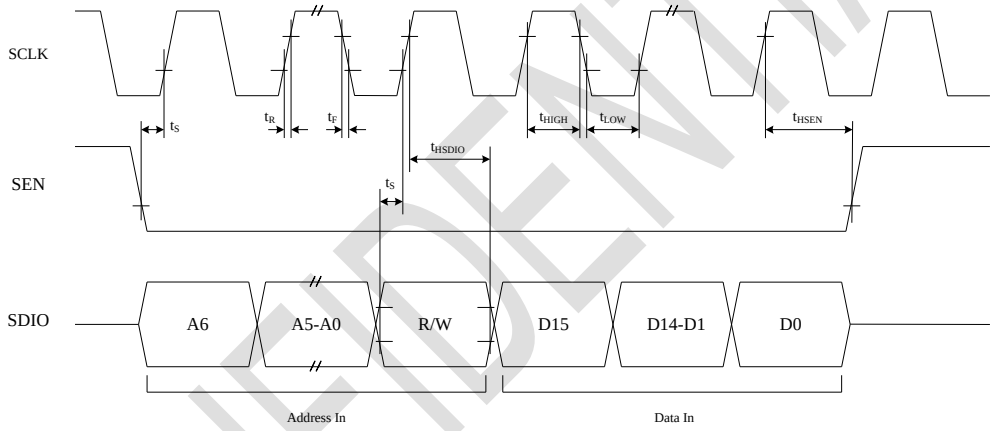

Figure 14. 3-Wire Control Interface Write Timing Diagram

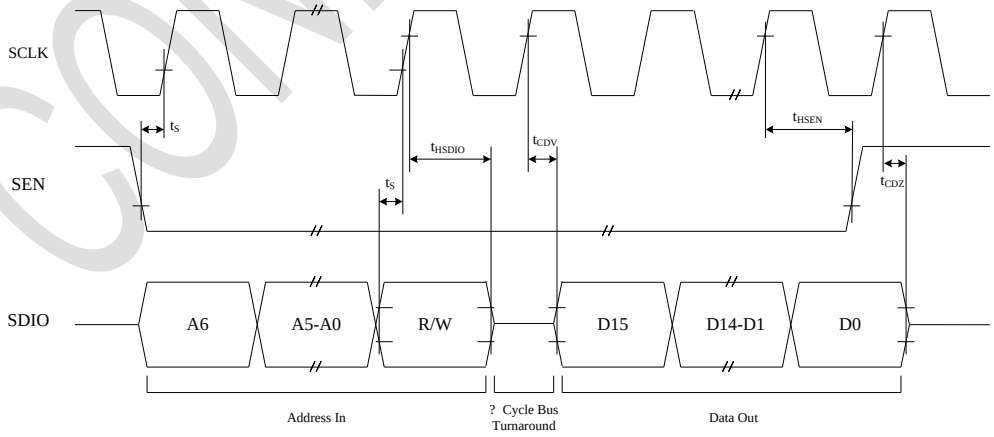

Figure 15. 3-Wire Control Interface Read Timing Diagram

3 Register Definition

Table 11. Interface Register Definition

(Default setting for 446.00625 MHz, IF = 137 kHz)

Address（DEC）	R/W	Default Setting	Sub-module	Description	
0	R	0x4815	Common	15:08	Device ID, read only
1	W/R	0x0000	Common	15	Channel spacing. 0: 12.5 kHz 1: 25 kHz
				14	FSK_AIR data rate. 0:1.2kbps 1:2.4kbps
				13	FSK Mode 0: FSK 1: FSK AIR
				12	DCS Mode 0: 23 bits 1: 24 bits
02 – 15	RF/Analog				
2	W	0x0019			
3	W	0x0027			
4	W	0xB641		08:07	VCO to LO divider number 0: 8; 1: 16; 2: 12; 3: 24
5	W	0xF770			
6	W	0xF274			
7	W	0x08F0			
8	W	0xFF33			
9	W	0xC3FA			
10	W	0xA2A3			
11	W	0x8800		12	PLL calibration 1->0->1
12	W	0x0603(RX) 0xF823(TX) 0xFFFF(Idle)		15	RX central bias 1: Power down 0: Power up
				14	RX front-end 1: Power down 0: Power up

				13	RX IF 1: Power down 0: Power up
				12	RX ADC 1: Power down 0: Power up
				11	RX Audio 1: Power down 0: Power up
				10	TX Audio 1: Power down 0: Power up
				09	TX PA 1: Power down 0: Power up
				08	Synthesizer 1: Power down 0: Power up
				07	LDO for synthesizer 1: Power down 0: Power up
				06	XTAL oscillator 1: Power down 0: Power up
				05	IF DAC 1: Power down 0: Power up
				04	Central bias 1: Power down 0: Power up
				03	RC calibration 1: Power down 0: Power up
				02	Digital supply 1: Power down 0: Power up
13	W	0x03FD		00	IF Selection 0: 88kHz IF 1: 137kHz IF
14	W	0x5817		10	0: LO high injection 1: LO low injection
15	W	0x908B			
16	W	0x88F9			
17 – 63	Digital Registers for TX Mode				
17	W/R	0x5800	ADC Filter	15:14	Filter gain (1, 1+1/4, 1+1/2, 2）
18	W/R	0x415C	AUDIO	06:02	Gain(-25~6 dB / 1dB)
19	W/R	0x08A0	AUDIO	13:00	Audio limiter value. -val ~ +val

20	W/R	0x0000	AUDIO	15:13	Scrambling frequency 0: 2700Hz 1: 2800Hz 2: 2900Hz 3: 3000Hz 4: 3100Hz 5: 3200Hz 6: 3300Hz 7: 3400Hz
21	W/R	0x002E	AUDIO	15:08	Microphone signal level. (Read only)
				05:00	Real time microphone gain, same unit as REG44[5:0]
22	W/R	0x3200	VOX	15	Enable VOX (1)
				14	Speech detection speed 0: 1/512 1: 1/256
				13:06	MIC_Level threshold for VoX
				05:00	MIC Gain threshold for VoX
24	W/R	0x086C	DTMF	15:00	Low frequency. (freq/18466)*65536
25	W/R	0x13BA	DTMF	15:00	High frequency. (freq/18466)*65536
26	W/R	0x0000	DTMF	15:12	Twist (Unit: dB) 0~15dB. 1dB/step
28	W/R		FSK	15:08	Send address
				07:00	Size
30	W		FSK	15:00	Payload FIFO
31	W/R		FSK	15:13	FIFO Threshold
				12	FIFO needs refilling (Read Only) 1: Needs refilling 0: No needs refilling
				11	Clear TX FIFO (Write 1)
				03:00	Total words in write FIFO (Read Only)
32	WR		FSK	15	Enable scrambling (1)
				14:08	Scrambling initial value
				00	FSK Tx Bit Select 1: From GPIO1 0: From inner frame
34	W/R		SELCALL	15:00	SELCALL tone Frequency ((Freq/18466)*65536)
36	W/R		CTCSS	14:13	The high 2 bits of CTCSS frequency
				01:00	Phase change (Unit: Degree) 0: 0 1: 120 2: 180 3: 240
37	W/R		CTCSS	15:00	The low 16 bits of CTCSS frequency ((Freq/18466)*65536*4)

38	W/R		CDCSS	11:00	High 12 bits of CDCSS if it has 24 bits or high 11 bits of CDCSS if it has 23 bits
39	W/R		CDCSS	11:00	Low 12 bits of CDCSS
40	W/R	0x8820	IB_MUX SB_MUX	15	1: Enable in-band signal modulation 0: Disable in-band signal modulation
				14:13	In-band signal type 0: Audio 1: DTMF 2: FSK 3: SELCALL
				12:09	In-band signal deviation 0.1x ~ 1.6x
				07	1: Enable sub-audio 0: Disable sub-audio
				06	Sub-audio signal type 0: CTCSS 1: CDCSS
				05:02	Sub-audio signal deviation 0.05x ~ 0.2x
41	W/R	0x2050	IB_MUX TX_UP	15:10	Deviation Tuning 0: 0.5x 1: 1x 2: 2x 63: 63x
				09:00	IF limiter. Unsigned. Real limiter amplitude = 16*REG41<9:0>
42	W/R		RAMP	15:10	RAMP memory address
				09:00	RAMP data
43	W/R	0x403F	RAMP	15	RAMP up enable 1: Enable 0: Disable
				14	RAMP down enable 1: Enable 0: Disable
				05:03	RAMP up speed 0: 0.08 ms 1: 0.08*2 ms 6: 0.08*64 ms 7: 0.08*128 ms
				02:00	RAMP down speed, same as ramp up speed definition
44	W/R	0x8A2E	AUD_AGC		
45	W/R	0x1B80	AUD_AGC		
46 – 63	Digital Registers for Digital Walkie-Talkie				
46	W/R	0x0072	CS_FLT0_B2	Filter 0 Coefficence B2	
47	W/R	0x00D3	CS_FLT0_B3	Filter 0 Coefficence B3	
48	W/R	0x6C0D	CS_FLT0_A2	Filter 0 Coefficence A2	

49	W/R	0xD1D5	CS_FLT 0_A3	Filter 0 Coefficence A3	
50	W/R	0xF717	CS_FLT 1_B2	Filter 1 Coefficence B2	
51	W/R	0x0735	CS_FLT 1_B3	Filter 1 Coefficence B3	
52	W/R	0x6D72	CS_FLT 1_A2	Filter 1 Coefficence A2	
53	W/R	0xCD0B	CS_FLT 1_A3	Filter 1 Coefficence A3	
54	W/R	0xDDAC	CS_FLT 2_B2	Filter 2 Coefficence B2	
55	W/R	0x15D8	CS_FLT 2_B3	Filter 2 Coefficence B3	
56	W/R	0x6F82	CS_FLT 2_A2	Filter 2 Coefficence A2	
57	W/R	0xC723	CS_FLT 2_A3	Filter 2 Coefficence A3	
58	W/R	0xC7A5	CS_FLT 3_B2	Filter 3 Coefficence B2	
59	W/R	0x2206	CS_FLT 3_B3	Filter 3 Coefficence B3	
60	W/R	0x721B	CS_FLT 3_A2	Filter 3 Coefficence A2	
61	W/R	0xC235	CS_FLT 3_A3	Filter 3 Coefficence A3	
62	W/R	0x1141	CTRL	15:8	DDS frequency
				06	Digital walkie-talkie module input clock enable
				05:04	Digital walkie-talkie module output config 0: 73.864kHz 1: 73.864kHz*2 2: 73.864kHz*4 1: 73.864kHz*8
				02:00	Digital walkie-talkie module output gain 0: 1x 1: 2x 2: 4x 3: 8x 4: 16x 5: 32x 6: 64x 7: 128x
64 – 111	Digital Registers for RX Mode				
64	W/R	0x8000	RF_FLT	15:14	CIC gain 0: 1x 1: 1.25x 2: 1.5x 3: 2x
				13:12	New HPF (RF_FLT) Control 0: Bypass 1: Run 2: Hold

65	W/R	0xC000	MIXER	15:14	CS Filter Configuration: 0/1: Auto Selection 2: Broad Band 3: Narrow Band
				12	Channel Selection result (read only) 0: Braod Band 1: Narrow
66	W/R	0xD003	FM_DEM	12	Parallel Audio enable
				11	Parallel DTMF enable
				10	Parallel FSK enable
				09	Parallel SELCALL enable
				08	Enable CTCSS receive
				07	Enable CDCSS receive
				06	Impulse threshold 0: 0.5*pi 1:0.75*pi
67	W/R	0x2000	FM_DEM	13	1: REG67<12:0> is averaged value 0: REG67<12:0> is real-time value
				12:00	Ex-band noise
68	R		RSSISNR	15:14	SNR/RSSI/Exband_Noise update period (samples) 0: 512; 1: 256, 2: 128, 3: 64
				13:08	SNR indicator, 1 dB per step, 0 is minimum
				06:00	RSSI indicator, 1 dB per step, 0 is minimum
69	W/R	0x67FF	AFC	15	1: Disable AFC 0: Enable AFC
				14:13	AFC gain 0: 2x 1: 1x 2: 0.5x 3: 0.25x
				12:00	AFC threshold (Unit: Hz)
70	R		AFC	15	AFC rail 1: AFC indicator > AFC threshold 0: AFC indicator < AFC threshold
				14	Link state 1: Link is active 0: Link is lost
				13:00	AFC residue frequency offset (Hz)

71	W/R	0x0000	RSSI	13:08	SNR threshold for AFC
				07	AFC Direction 1: Inversed mode 0: Normal mode
				06:00	RSSI threshold for AFC
72	W/R	0xA002	BB_FLT	06:03	Scrambling frequency 0: 2700Hz 1: 2800Hz 2: 2900Hz 3: 3000Hz 4: 3100Hz 5: 3200Hz 6: 3300Hz 7: 3400Hz
				02:00	CTCSS_AMP 0: 8x 1: 4x 2: 2x 3: 8x
73	W/R	0x2600	AUDIO	15	1: Hard Mute (Only affect when REG73[10]=0)
				14:07	RX audio level (Read only)
				03:00	Volume 0: -9dB 1: -8dB 2: -7dB …… 15: 6dB
75	W/R	0x7A86	DTMF	15:05	DTMF detection speed Suggest value: 1960
76	W/R	0x6506	DTMF		
77	W		DTMF	15:12	DTMF symbol address
				11	DTMF Symbol frequency band 1: High band 0: Low band
				10:00	DTMF symbol low band or high band tone frequency =(Freq/4103)*4096
78	W/R		DTMF	14	DTMF symbol loss indication
				8	DTMF symbol found indication
				07:04	Address of found DTMF symbol
				03:00	DTMF symbol numbers in search table
79	R		FSK	15:08	Address
				06:00	Type
81	W/R	0xB200	FSK	15:05	Symbol detection speed Suggest value: 1424

82	R		FSK	15:00	Payload FIFO
83	W/R		FSK	15:13	FIFO Threshold
				12	FIFO needs reading out
				11	Write 1 to clear RX FIFO
				05	Free format type
				04	CRCB_OK 1: No error in payload 0: Error in payload, will be automatically updated at the end of new RX packet
				03:00	Total words in read FIFO
84	W/R	0xFC46	SELCALL	15:05	SELCALL detection speed Suggest value: 2018
85	W/R	0x78A6	SELCALL		
86	W		SELCALL	15:12	SELCALL Symbol Address
				11:00	SELCALL symbol frequency Value = (Freq/18466)*4096)
87	W/R	0x0000	SELCALL	14	HPF_BYPASS 1: Bypass 0: No bypass
				13	1: Found symbol is lost
				12	SELCALL HPF coefficient selection 0: First group 1: Second group
				07:04	The address of found SELCALL symbol
				03:00	SELCALL symbol numbers in search table
89	W/R	0xF7A0	CTCSS	15:04	CTCSS detection speed, for example: 0xFF8 for high sensitivity and >1 second response time 0xF7A for normal sensitivity and <100 ms response time
90	W/R	0x3C46	CTCSS		
91	W		CTCSS	15:13	CTCSSS symbol address
				12:00	CTCSSS symbol frequency Value = (Freq/18466)*65536*8
92	W/R	0x0000	CTCSS	14	1: Bypass HPF

				13	1: Found CTCSS symbol is lost
				11:08	High 4bits address of found CTCSS (for standard mode)
				07:04	The address of found CTCSS symbol
				02:00	CTCSS symbol numbers in search table
93	W/R	0x0000	CTCSS	08:02	Loss threshold(Time duration for loss report) 15: 11ms 31: 22ms 63: 55ms 127: 110ms
				01:00	CTCSS detect phase change 0: 0° 1:120°/240° 2:180° 3: Reserved
94	W/R	0x00E8	CDCSS	15	1: Bypass HPF
				14:08	Address of found CDCSS
				07:06	Synchronization Threshold 0: 32 1: 64 2: 128 3: 256
				02	Phase of found CDCSS 0: Normal 1: Inverse
				1	1: CDCSS loss
95	W/R		CDCSS	11:00	High 12 bits of CDCSS if it has 24 bits or high 11 bits of CDCSS if it has 23 bits
96	W/R		CDCSS	11:00	Low 12 bits of CDCSS
97	W/R		CDCSS	15:08	Number of CDCSS code to be searched
				06:00	Address of RX CDCSS (Should be wrote before REG95/96)
98	W/R	0x0005	CDCSS	03:01	DCS code match threshold (Last for N times) 0: 1 time 1: 2 times 2: 3 times…… 7: 8 times
				00	Slice calculation enable
99	W/R	0x0000	FSK_AIR	15	HPF bypass
				14	Inverse the FSK AIR output

				11:06	Coefficient A1
				05:00	Coefficient A2
100	W/R	0x0000	Receiver	07	0: Bypass new RSSI2 path 1: Run new RSSI2 path
				06:00	RSSI2, 1 dB/Step, 0 is maximum
101	R		RF AGC	15:08	AGC_H; IF RSSI high level indicator
				07:00	AGC_L; IF RSSI low level indicator
102	W/R	0x0000	Ex-band Noise	13	Link-Loss judgment selection : 1 : Ex-Noise 0: Rssi_SNR
				12:00	Baseband out-of-band noise level
103	W/R	0x431F	RF AGC	15	RX AGC 0: Enable 1: Disable
				14:08	RSSI Offset
				04	RF LNA gain selection 0: Low gain 1: High gain
				02:00	IF PGA gain selection 0: 0dB 1: 3dB 2: 6dB…… 7: 21dB
104	W/R	0x0000	RF AGC		
105	W/R	0x0000	RX Audio	15	1: Up enable
				14	1: Down enable
				09:00	End value (0~1023)
106	W/R	0x0000	RX Audio	15:09	Clock divide ratio DIV 0: 1 1: 2 2: 3…… 127: 128
				08:00	Start value (0~511)
107-11	RF / Analog				
107	W/R	0x3415	TX Audio		
108	W/R	0x6927	RX Audio	14:11	PGA gain 0: -24dB W/R 1: -22dB 2: -20dB…… 15: +6dB
109	W/R	0x4600(RX) 0x4700(TX)	Analog	15:13	PA output power control -20dBm~+6dBm(not linear)
				12	PA ramp up/down enable

				09	Synthesizer state control 1: By SPI 0: By DSP
				08	Synthesizer state 1: TX mode 0: RX mode
112-119	Control and Interrupt				
112	W/R	0xA000(RX) 0xE000(TX)	Operation Control	15	1: Power up digital section 0: Power down digital section
				14	Digital logic operation mode 1: TX mode 0: RX mode
				13	1: Normal work, 0: Software reset, it will not reset registers
113	W/R		Frequency control	15:00	High 16 bits of First Channel Frequency
114	W/R		Frequency control	15:00	Low 16 bits of First Channel Frequency
115	W/R		Interrupt MASK	15	1: Enable interrupt 0: Disable all interrupt
				14	Enable FSK transmit success interrupt
				13	Enable FSK transmitter FIFO need fill interrupt
				12	Enable FSK head receive success interrupt
				11	Enable FSK receiver FIFO need read interrupt
				10	Enable DTMF receive interrupt
				9	Enable SELCALL receive interrupt
				8	Enable CTCSS receive interrupt
				7	Enable CTCSS tone loss interrupt
				6	Enable link lost interrupt
				5	Enable CDCSS receive interrupt
				4	Enable CDCSS lost interrupt
				3	Enable VOX interrupt
				1	Enable FSK receive complete interrupt
116	W/R		Interrupt	15	1: Reset all flags to zeros

			flags (Active high) Set by hardware and reset by software (write 1 will clear interrupt bit to 0)	14	FSK transmit success interrupt
				13	FSK transmitter FIFO need fill interrupt
				12	FSK head receive success interrupt
				11	FSK receiver FIFO need read interrupt
				10	DTMF receive interrupt
				9	SELCALL receive interrupt
				8	CTCSS receive interrupt
				7	CTCSS loss interrupt
				6	Link lose interrupt
				5	CDCSS receive interrupt
				4	CDCSS lost match interrupt
				3	VOX voice detected interrupt
				1	FSK receive complete interrupt
117	W/R	0x0400	GPIO	11	1: Bypass gated clock
				10	0: Normal IF, low side injection 1: Inverse IF, high side injection
				09	1: Send CTCSS / CDCSS / DTMF / SELCALL / FSK or TX Audio to RX Audio
				08:06	Select the signal to RX Audio 0: CDCSS 1: CTCSS 2: SELCALL 3: DTMF 4: FSK 5: Audio 6: FSK AIR 7: Force to “0”
				05:03	GPIO1 mode control 0: Normal input 1: Output low 2: Output high Other: Invalid

				02:00	GPIO1 mode control 0: Normal input 1: Output low 2: Output high 3: Output CTCSS signal 4: Output CDCSS signal Other: Invalid
118	R		GPIO	1	GPIO1 input value
				0	GPIO0 input value
120-127	Enhanced Functions				
122	W/R	0x46A3	FSK	FSK bit rate setting = reference_clock/bit_rate	
				Default is: 26e6/1200	
123	W/R	0x0002	CDCSS	MSB 2 bits of CDCSS bit rate setting = reference_clock/bit_rate Default is: 26e6/134.4	
124	W/R	0xF826	CDCSS	LSB 16 bits of CDCSS bit rate setting = reference_clock/bit_rate Default is: 26e6/134.4	
125	W/R	0xED69	MIXER	IF DDS Setting, unsigned DDS_IF = REG125*2 = IF * 2^18 / (26MHz/88kHz)	
126	W/R	0xFFF5	Frequency control	RX IF frequency, signed, high 16 bits	
127	W/R	0x3568	Frequency control	RX IF frequency, signed, low 16 bits	

4 Pin Assignment

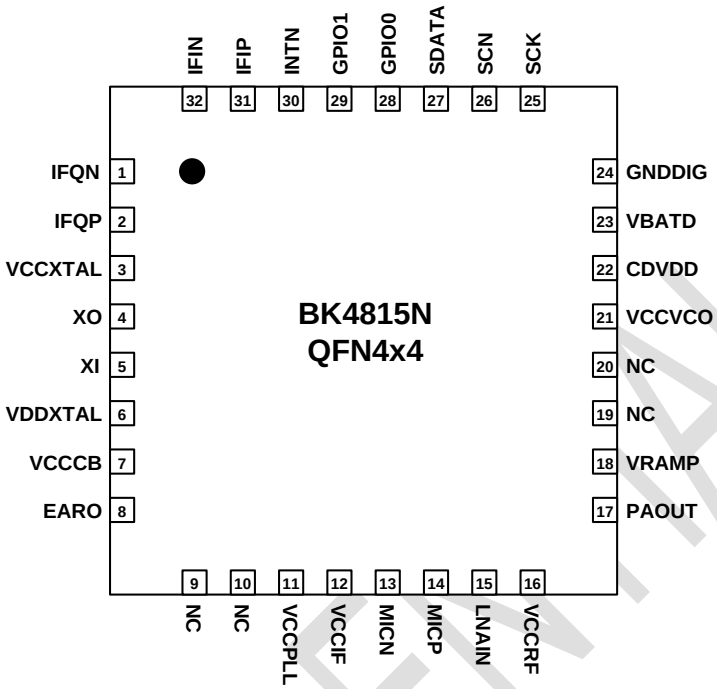

Figure 16. BK4815N Pin Assignment (Top View)

Table 12. BK4815N 4mmx4mm 32-Pin Definition

Pin #	Name	Direction	Function
1	IFQN	Output	Baseband analog ouput signal QN
2	IFQP	Output	Baseband analog ouput signal QP
3	VCCXTAL	Input	Power supply, 3.0 V to 3.6 V
4	XO	Input	Crystal oscillator port, output
5	XI	Output	Crystal oscillator port, input
6	VDDXTAL	Output	XTAL OSC regulator output
7	VCCCB	Input	Power supply, 3.0 V to 3.6 V
8	EARO	Output	Earpiece output
9	NC		
10	NC		
11	VCCPLL	Input	Power supply, 3.0 V to 3.6 V
12	VCCIF	Input	Power supply, 3.0 V to 3.6 V
13	MICN	Input	Microphone input, negative
14	MICP	Input	Microphone output, positive
15	LNAIN	Input	Input of low noise amplifier
16	VCCRF	Input	Power supply, 3.0 V to 3.6 V
17	PAOUT	Output	Output of power amplifier
18	VRAMP	Output	PA regulator output
19	NC		
20	NC		
21	VCCVCO	Input	Power Supply, 3.0 V~ 3.6 V
22	CDVDD	Output	Digital regulator output
23	VBATD	Input	Power Supply, 3.0 V~ 3.6 V

24	GNDDIG	Input	Ground
25	SCK	Input	SPI clock
26	SCN	Input	SPI enable
27	SDATA	I/O	SPI data
28	GPIO0	I/O	General purpose input/output. Can be used as DCS output
29	GPIO1	I/O	General purpose input/output
30	INTN	Output	Interrupt
31	IFIP	Output	Baseband analog ouput signal IP
32	IFIN	Output	Baseband analog ouput signal IN

5 Typical Application Schematic

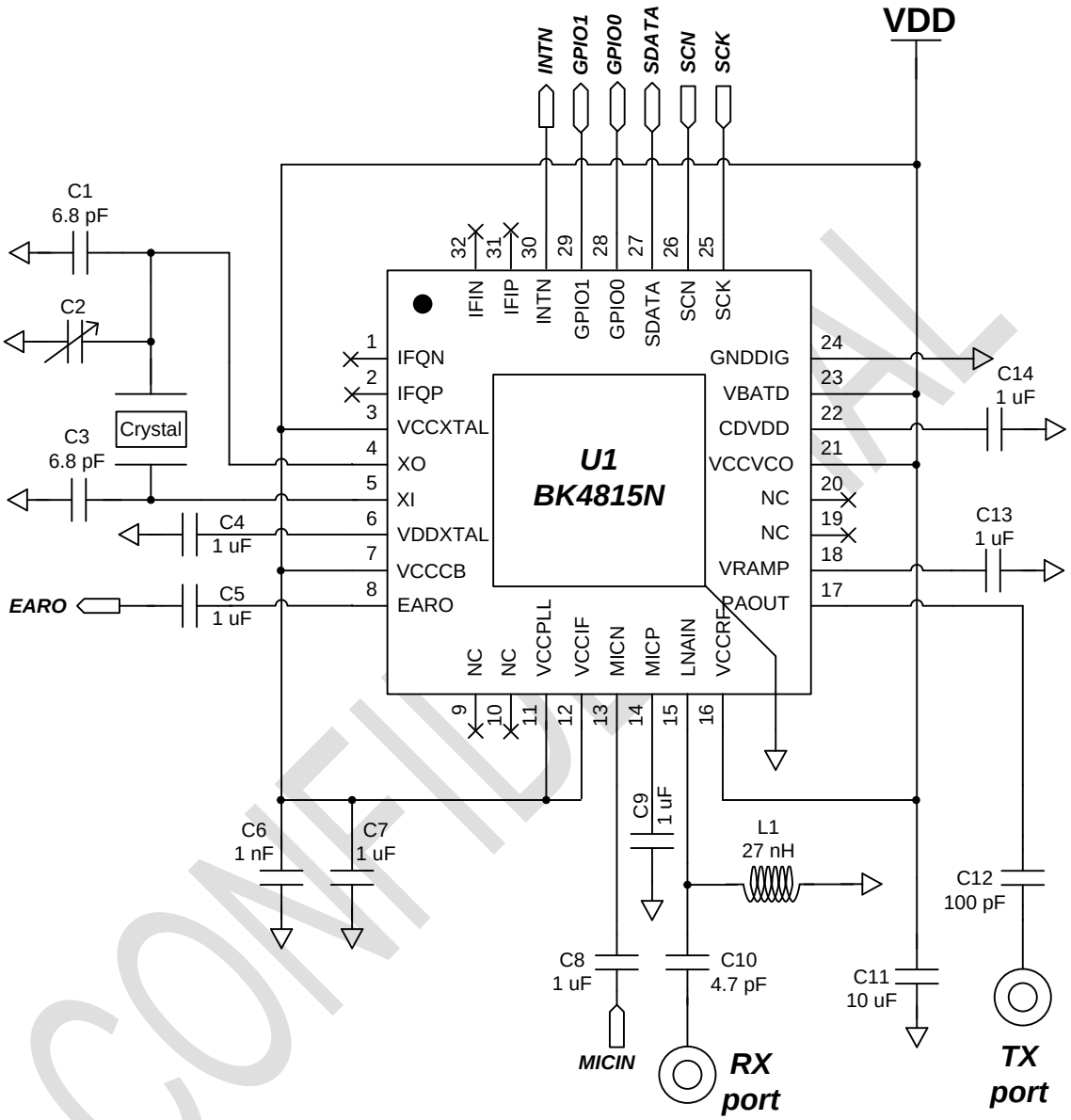

Figure 17. BK4815N Application

6 Package Information

QFN 4mmx4mm 32pin package is available for BK4815N. Detail information of the package is shown below:

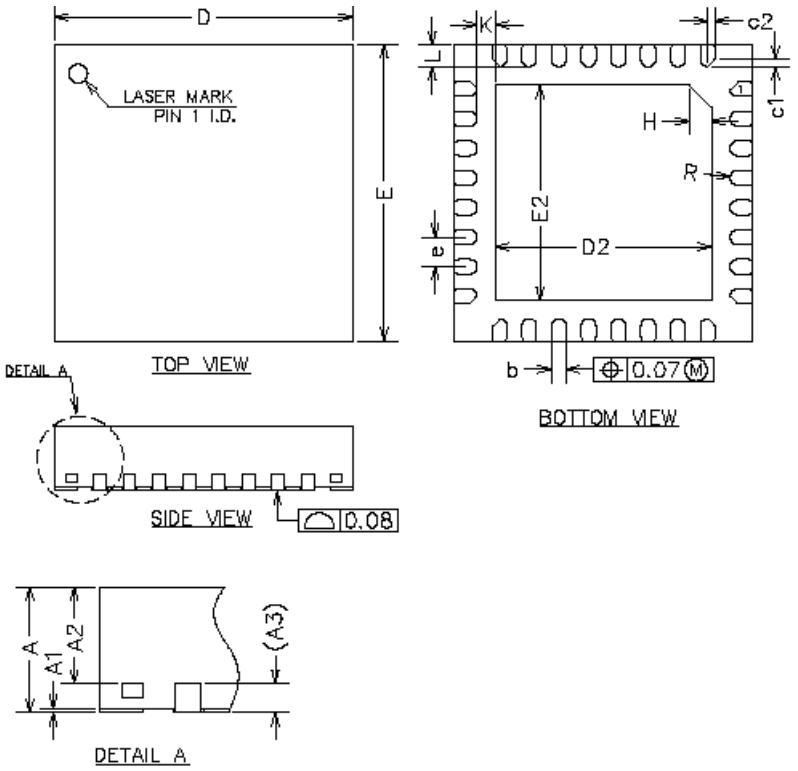

Figure 18. QFN 4x4 32 Pin Package diagram

Table 13. QFN 4x4 32 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.80	0.85	0.90	mm
A1	0.00	0.02	0.05	mm
A2	0.60	0.65	0.70	mm
A3		0.20 REF		mm
b	0.15	0.20	0.25	mm
D	3.90	4.00	4.10	mm
E	3.90	4.00	4.10	mm
D2	2.80	2.90	3.00	mm
E2	2.80	2.90	3.00	mm
e	0.30	0.40	0.50	mm
H		0.30 REF		mm
K		0.25 REF		mm
L	0.25	0.30	0.35	mm
R	0.09	–	–	mm
c1	–	0.10	–	mm
c2	–	0.10	–	mm

Soldering layer content

Content	width	unit
Ni	0.5-2.0	um
Pd	0.02-0.15	um
Au	0.003-0.015	um

Storage Caution

1. Calculated shelf life in vacuum sealed bag 12 months at<40℃ and 90% relative humidity (RH).
2. Peak package body temperature 260℃.
3. After vacuum sealed bag is opened ,devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory conditions<40℃/60%.
   b) Stored at 10% RH.

Package Markings(Top Marks)
QFN 32

N: Character N
V: Version Number
YWW: Y=Year, WW=Workweek
L: The last nubmer of Wafer
A: Assembly house number

7 Tape and Reel Information

All dimensions are in millimeters by default.

7.1 Tape Information

The figure below shows the dimensions of the tape for the BK4815N QFN.

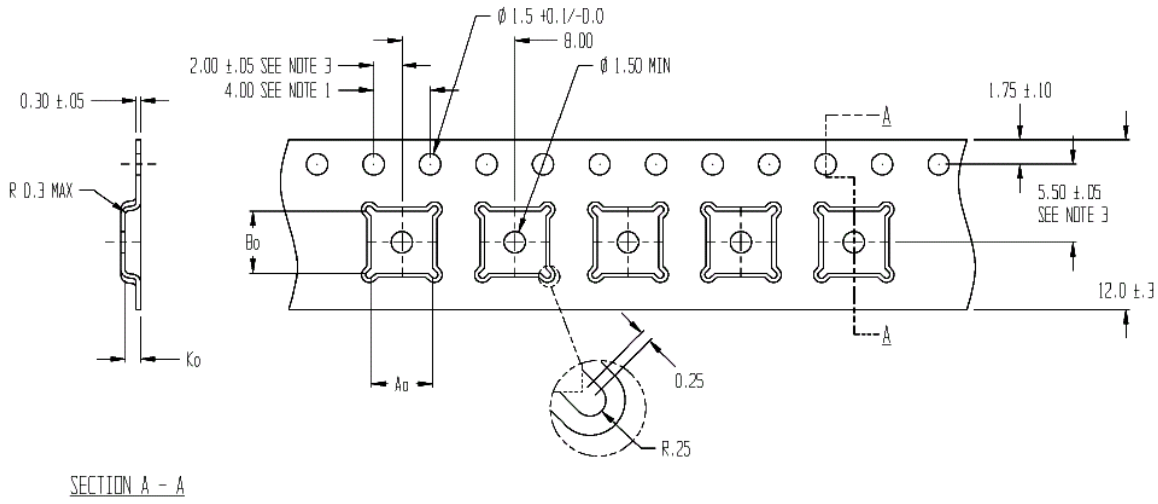

Figure 19. Tape Dimensions

A_0	B_0	K_0	Unit	Notes
4.35	4.35	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2. 2. Camber in compliance with EIA 481. 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

7.2 Cover Information

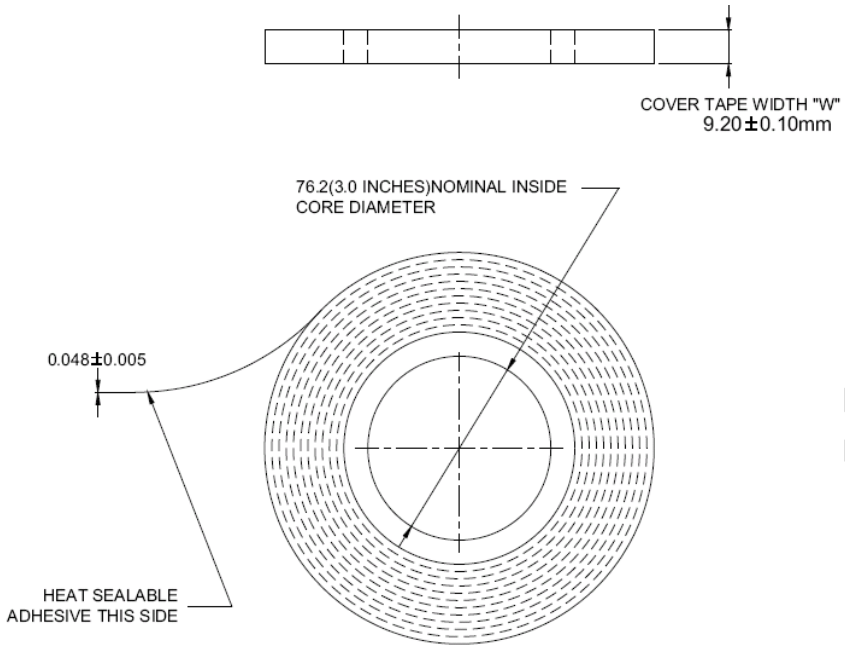

Figure 20. Cover Dimensions

Note:

1. Reel to contain 300 meters of splice free material.
2. Material: Polyester film with antistatic coating and adhesive coating.
3. Color: Transparent, natural

7.3 Reel Information

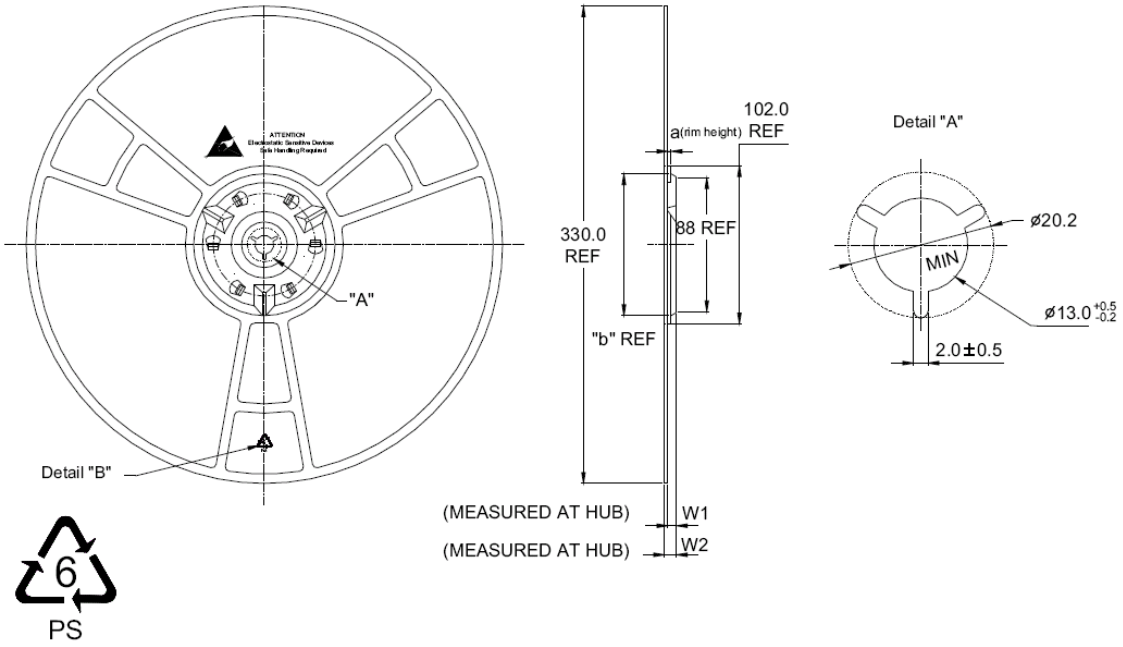

Figure 21. Reel Dimensions

Nominal Hub Width	W1 +0.6mm -0.4mm	W2 MAX	a	b	Unit
12	12.8	18.2	1.5	96.5	mm

8 Solder Reflow Profile

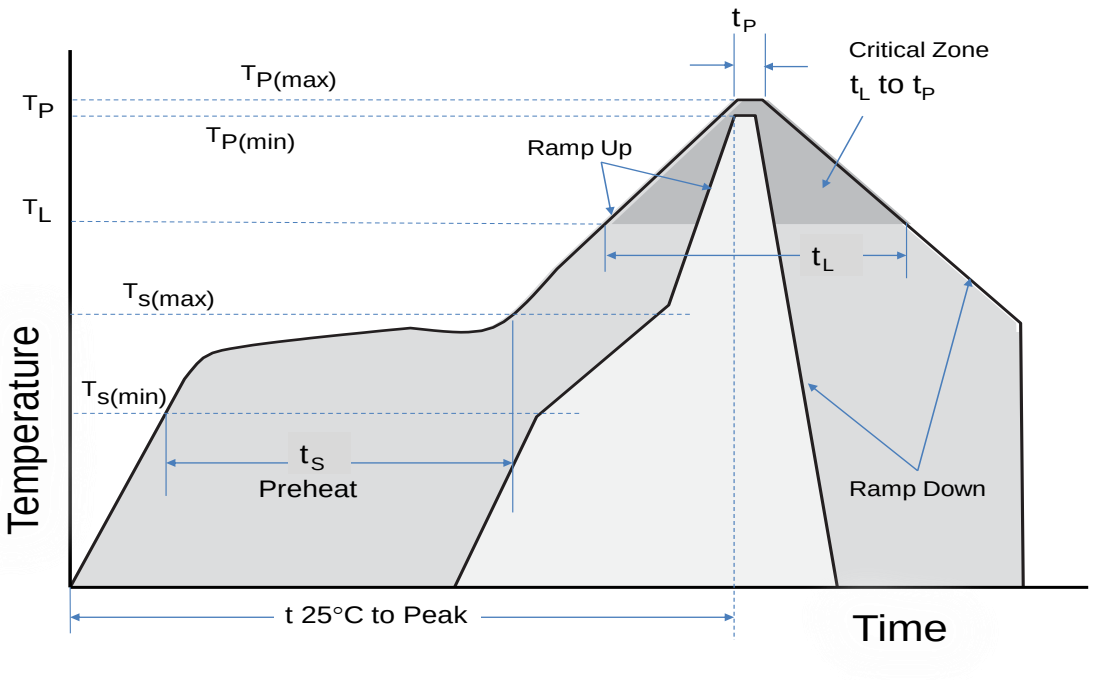

Figure 22. Classification Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate 6		6°C/second max.
Time 25°C to Peak Temperature 8		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

9 Order Information

Part number	Package	Packing	MOQ (ea)
BK4815NQB	QFN	Tape Reel	3 k

Remark:
MOQ: Minimum Order Quantity

10 Additional Reference Resources

- Application Notes
- Register Table
- Schematic & Layout
- Frequency Calculator

11 Revision History

Version	Change Summary	Date	Author
Rev.1.0	Initial Release	2016/09/01	PH

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